1.0 Key Features

Controller area network (CAN) is a serial communication protocol, which supports distributed real-time control and multiplexing with high safety level. Typical applications of CAN-based networks can be found in automotive and industrial environments.

The AMIS-42700 Dual-CAN transceiver is the interface between up to two physical bus lines and the protocol controller and will be used for serial data interchange between different electronic units at more than one bus line. It can be used for both 12V and 24V systems.

The circuit consists of following blocks:

- Two differential line transmitters
- Two differential line receivers
- Interface to the CAN protocol handler
- Interface to expand the number of CAN busses
- Logic block including repeater function and the feedback suppression
- Thermal shutdown circuit (TSD)
- Short to battery treatment circuit

Due to the wide common-mode voltage range of the receiver inputs, the AMIS-42700 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

2.0 Key Features

- Fully compatible with the ISO 11898-2 standard
- Certified "Authentication on CAN Transceiver Conformance (d1.1)"
- High speed (up to 1 Mbit/s)
- Ideally suited for 12V and 24V industrial and automotive applications
- Low EME common-mode-choke is no longer required
- Differential receiver with wide common-mode range (+/- 35V) for high EMS
- No disturbance of the bus lines with an un-powered node
- Transmit data (TxD) dominant time-out function
- Thermal protection
- Bus pins protected against transients in an automotive environment
- Power down mode in which the transmitter is disabled
- Short circuit proof to supply voltage and ground
- Logic level inputs compatible with 3.3V devices
- ESD protection guaranteed up to ±8KV

3.0 Technical Characteristics

Table 1: Technical Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
$V_{i(dif)(bus\_dom)}$	Differential bus output voltage in dominant state	$42.5\Omega < R_{LT} < 60\Omega$	1.5	3	V
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD	See Figure 7	70	245	ns
$t_{pd(dom-rec)}$	Propagation delay TxD to RxD	See Figure 7	100	245	ns
CM-range	Input common-mode range for comparator	Guaranteed differential receiver threshold and leakage current	-35	+35	V
$V_{CM-peak}$	Common-mode peak	See Figure 8 and 9 (note)	-500	500	mV
$V_{CM-step}$	Common-mode step	See Figure 8 and 9 (note)	-150	150	mV

Notes: The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low EME.

4.0 Ordering Information

Marketing Name	Package	Temp. Range
AMIS 42700FHA	SOIC-20 300 G	-40°C…125°C

5.0 Block Diagram

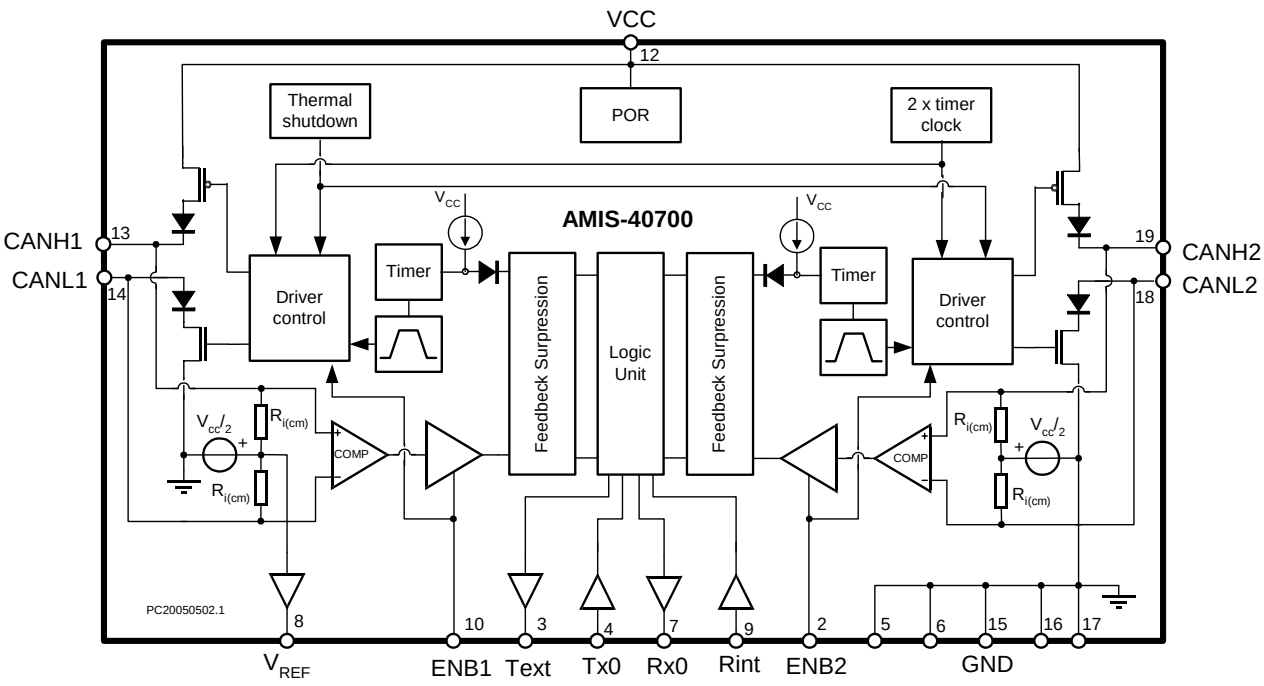


Figure 1: Block Diagram

6.0 Typical Application

6.1 Application Description

AMIS-42700 is especially designed to provide the link between a CAN controller (protocol ic) and two physical busses. It is able to operate in three different modes:

- Dual CAN
- A CAN bus extender
- A CAN bus repeater

6.2 Application Schematics

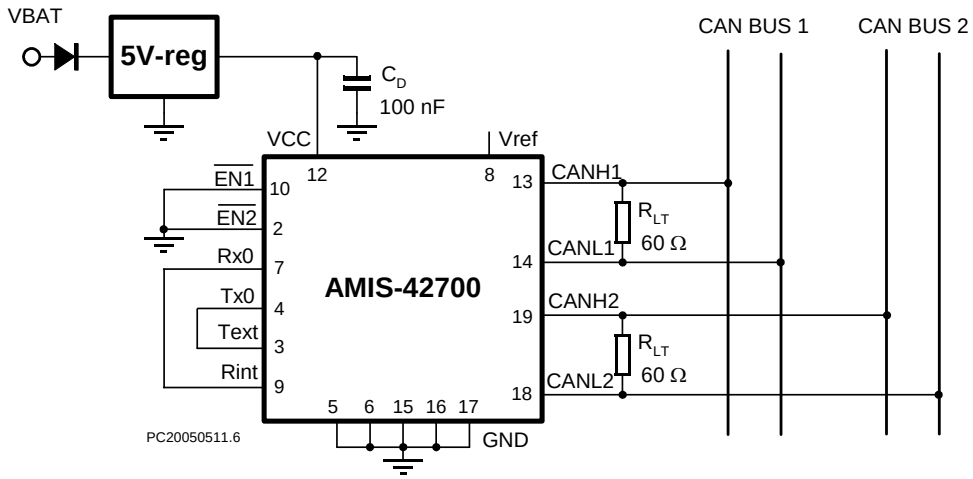


Figure 2: Application Diagram CAN-Bus Repeater

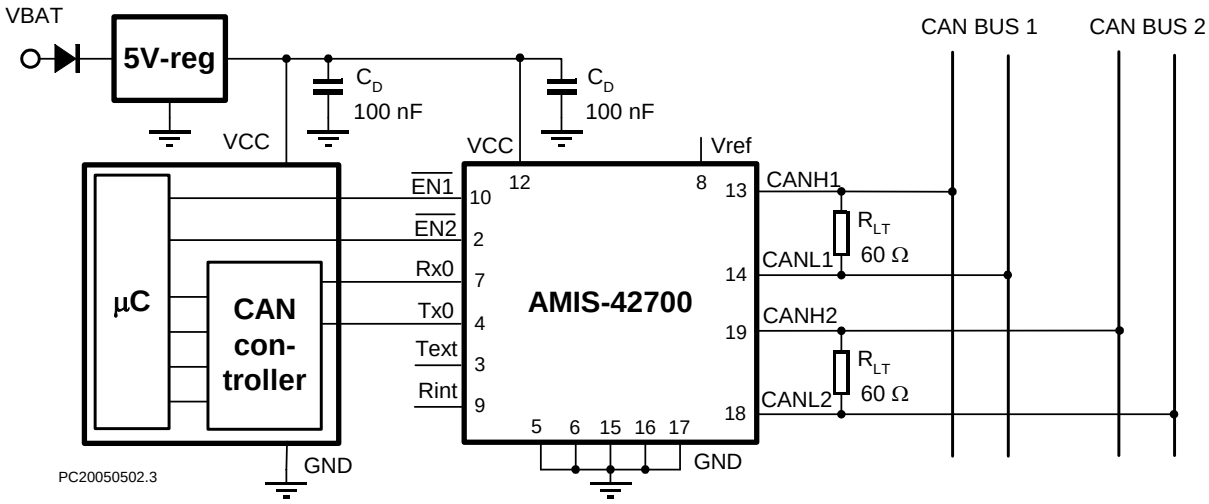


Figure 3: Application Diagram Dual-CAN

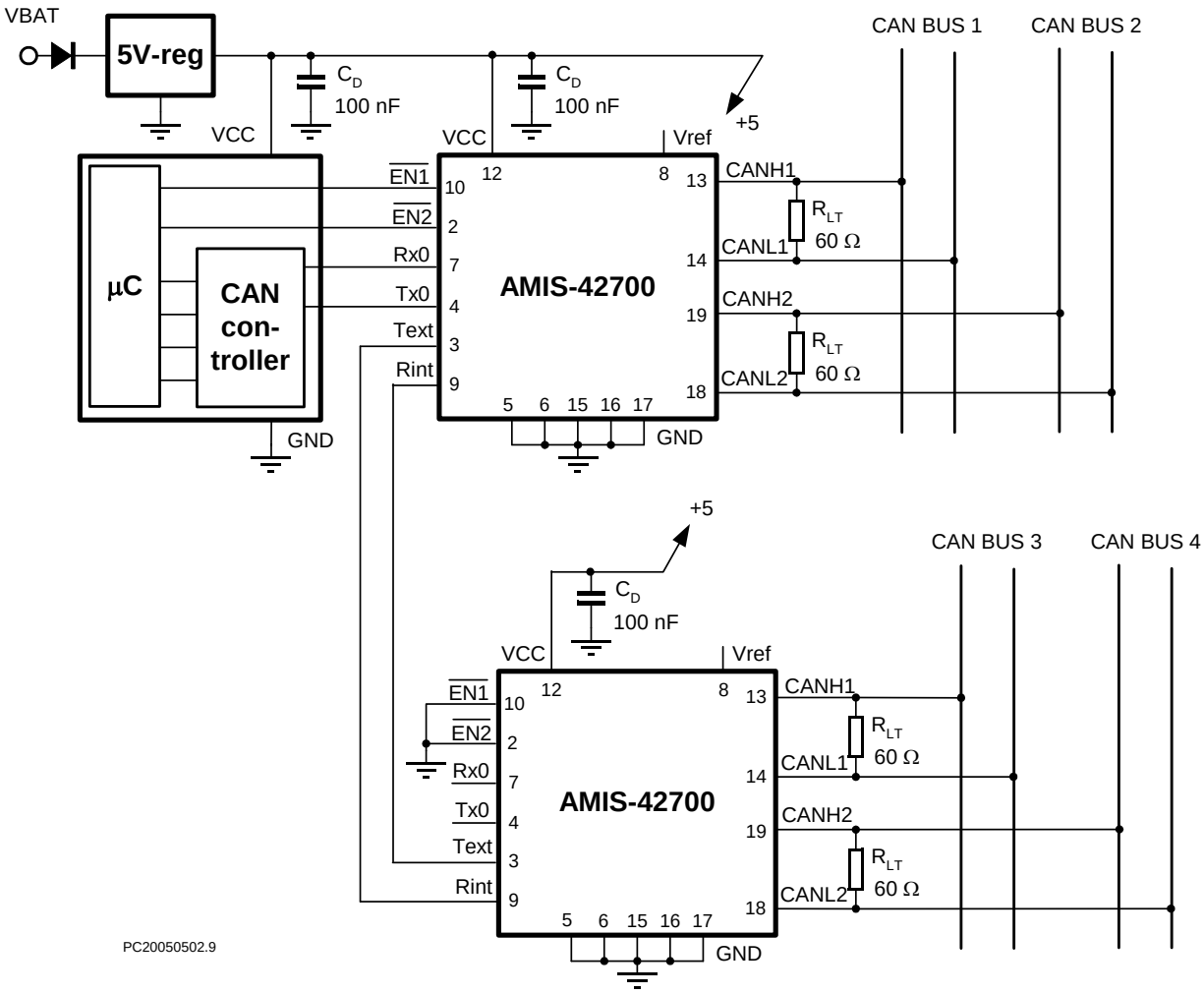


Figure 4: Application Diagram CAN Bus Extender

6.3 Pin Description

6.3.1 Pinout (top view)

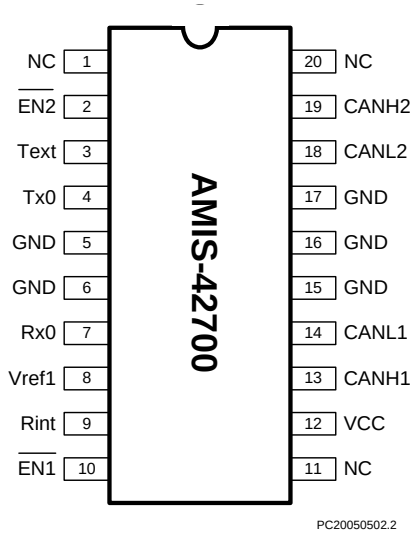


Figure 4: Pin Configuration

6.3.2 Pin Description

Table 2: Pinout

Pin	Name	Description
1	NC	Not connected
2	ENB2	Enable input, bus system 2
3	Text	Multi system transmitter input
4	Tx0	Transmitter input
5	GND	Ground connection, note 1
6	GND	Ground connection, note 1
7	Rx0	Receiver output
8	V_{REF1}	Reference voltage
9	Rint	Multi system receiver output
10	ENB1	Enable input, bus system 1
11	NC	Not connected
12	VCC	Positive supply voltage
13	CANH1	CANH transceiver I/O bus system 1
14	CANL1	CANL transceiver I/O bus system 1
15	GND	Ground connection, note 1
16	GND	Ground connection, note 1
17	GND	Ground connection, note 1
18	CANL2	CANL transceiver I/O bus system 2
19	CANH2	CANH transceiver I/O bus system 2
20	NC	Not connected

Notes:
1) In order to ensure the chip performance, these pins need to be connected to GND on the PCB.

7.0 Functional Description

7.1 Overall Functional Description

The CAN transceiver is specially designed to provide the link between the protocol IC (CAN controller) and two physical bus lines. Data interchange between those two bus lines is realized via the interface. Bitwise arbitration is extended on both buses. A fault like short circuit is limited to that bus line where it occurs. Data interchange from the protocol IC to the other bus system and on this bus system itself can be continued.

The transceiver can also be used for only one bus system. If the connections for the second bus system are simply left open it serves as a single transceiver for an electronic unit. For correct operation it is necessary to terminate an open bus. If not, the open bus will disturb the other one, e.g. in case of open load.

The bus lines can have two logical states, dominant or recessive. A bus is in the recessive state when the driving sections of all transceivers connected to the bus are passive. The differential voltage between the two wires is approximately zero. If at least one driver is active the bus changes into the dominant state. This state is represented by a differential voltage greater than a minimum threshold and therefore by a current flow through the terminating resistors of the bus line. The recessive state is overwritten by the dominant state.

To provide an independent switch-off of the transceiver units for both bus systems by a third device (e.g. the µC) enables inputs for the corresponding driving and receiving sections to be included.

7.2 Transmitter

The transceiver includes two transmitters, one for each bus line and a driver control circuit. Each transmitter is implemented as a push and a pull driver. The drivers will be active if the transmission of a dominant bit is required. During the transmission of a recessive bit all drivers are passive. The transmitters have a built-in current limiting circuit that protects the driver stages from damage caused by accidental short circuit to either positive supply voltage or to ground. Additionally a thermal protection circuit is integrated.

The driver control circuit ensures that the drivers are switched on and off with a controlled slope to limit EME. The driver control circuit will be controlled itself by the thermal protection circuit, the timer circuit, the ENBx inputs, and the logic unit.

The dominant time out timer circuit prevents the output drivers from driving a permanent dominant state (blocking all network communication) if pin Tx0 or the bus lines of the other bus are forced permanently dominant by a hardware and/or software failure (see tdom(TxD)).

The enable signal ENBx allows the transmitter to be switched off by a third device (e.g. the µC). In the disabled state (ENBx = high) the corresponding transmitter behaves as in the recessive state and does not depend on the input voltage at Tx0 nor on the state of the other bus system.

7.3 Receiver

Two bus receiving sections sense the states of the bus lines. Each receiver section consists of an input filter and a fast and accurate comparator. The aim of the input filter is to improve the immunity against high-frequency disturbances and also to convert the voltage at the bus lines CANHx and CANLx, which can vary from –12V to +12V, to voltages in the range 0 to 5V, which can be applied to the comparators.

The output signal of the comparators is gated by the ENBx signal. In the disabled state (ENBX = high) the output signal of the comparator will be replaced by a permanently recessive state and does not depend on the bus voltage. In the enabled state the receiver signal sent to the logic unit is identical to the comparator output signal.

7.4 Feedback Suppression

To provide proper function a feedback suppression must be included. This circuit replaces the reception of a dominant bit detected by the receiving section with a recessive bit if the corresponding transmitter is active.

The feedback suppression must be activated immediately after the transmitter is requested to drive, i.e. before the receiver detects the dominant state at the bus. After deactivating the transmitter, the feedback suppression must stay active long enough to guarantee that the corresponding receiver has sufficient time to change its state from dominant to recessive.

Including the feedback, suppression is possible because a transmitter becomes active if the other bus system or Tx0 is in the dominant state, so the reception of a dominant bit is already realized and need not be done additionally by this receiving section. Without feedback suppression the whole system would stay constantly in the dominant state after the occurrence of one dominant bit.

The logic is implemented in such a way that the suppression blocks in the two busses work independently of each other, and are identical so that both busses have the same priority. Furthermore the oscillation or single pulsing, that could occur at the dominant to recessive edge when the transceiver has received acknowledges from both busses, is avoided with this implementation.

If both buses are driven externally and go from dominant to recessive with some delay between each other, no spurious pulses are seen at RINT and Rx0. However, it is possible to have the driving section of one bus going active while that bus is still driven externally. To minimize the chance of this condition, an additional delay of typical 50ns is added that blocks the requirement to drive the driving section after the bus is forced externally from dominant to recessive.

7.5 Logic Unit and CAN Controller Interface

The central logic unit provides data transfer from/to the digital interface to/from the two busses and from one bus to the other bus.

Digital input stages convert the input voltage at Tx0 and TEXT into a logical value for the logic unit. All digital inputs, including ENBx, have an internal pull up resistor to ensure a recessive state when the input is not connected or is accidentally interrupted. Output stages convert the logical value provided by the logic unit into voltages corresponding to the input signal specification of the CAN controller at Rx0 and RINT. A dominant state on the bus line is represented by a low-level at the digital interface, a recessive state is represented by a high-level.

V_{ref} provides an analog voltage of $V_{cc}/2$ as a reference for CAN controller with analog inputs.

Input and output signals of the logic unit are related in such a way that a dominant state on any bus or Tx0 causes a dominant state on both buses, RINT and Rx0.

The output signal at Rx0 corresponds to the inputs Tx0 and TEXT, independent of the state of the two enable inputs. This is realized by an internal logical connection.

The pins TEXT and RINT are used for connecting the internal logics of several ICs to obtain versions with more than two bus outputs. If a dominant bit is received from at least one of the two bus systems (under the condition of feedback suppression) or from Tx0, RINT carries the low-level. Otherwise RINT is high. A low-level at TEXT activates both transmitters causing a dominant state on both busses and sets Rx0 to the low-level. A high-level at TEXT does not influence the transceiver.

7.6 Power-on-Reset (POR)

While Vcc voltage is below the POR level, the POR circuit makes sure that:

- The counter is kept in the reset mode and stable state without current consumption
- Inputs are disabled (don't care)
- Outputs are high impedant; only Rx0 = high-level
- Analog blocks are in power down
- Oscillator not running and in power down
- CANHx and CANLx are recessive
- VREF output high impedant for POR not released

7.7 Time Out Timer

The Tx0 dominant time out timer circuit prevents the output drivers from driving a permanent dominant state (blocking all network communication) if pin Tx0 or the bus lines of the other bus are forced permanently dominant by a hardware and/or software failure. The timer is triggered by a negative edge of the TIMERIN signal. If the duration of the low-level on TIMERIN exceeds the internal timer value TIMERDEL, the timer output TIMEROUT becomes high, disabling the transmitter (bus returns into the recessive state). The timer is reset by a positive edge of the TIMERIN signal.

7.8 Over Temperature Detection

A thermal protection circuit is integrated to prevent the transceiver from damage if the junction temperature exceeds thermal shutdown level. Because the transmitter dissipates most of the total power, the transmitter will be switched off only to reduce power dissipation and IC temperature. All other IC functions continue to operate.

7.9 Fault Behavior

A fault like a short circuit is limited to that bus line where it occurs, hence data interchange from the protocol IC to the other bus system is not affected.

When the voltage at the bus lines is going out of the normal operating range (-12V to +12V), the receiver is not allowed to erroneously detect a dominant state.

7.10 Short Circuits

As specified in the maximum ratings, short circuits of the bus wires CANHx and CANLx to the positive supply voltage Vbat or to ground must not destroy the transceiver. To provide sufficient safety for automotive applications the voltage range for permanent short circuits is extended to 50V dc. A short circuit between CANHx and CANLx must not destroy the IC as well.

The dedicated comparator (L2VBAT) on CANL pin detects the short to battery and after debounce time-out switches off the affected driver only.

The receiver of the affected driver has to operate normally.

7.11 Faulty Supply

In case of a faulty supply (missing connection of the electronic unit or the transceiver to ground, missing connection of the electronic unit to Vbat or missing connection of the transceiver to Vcc) the power supply module of the electronic unit will operate such that the transceiver is not supplied, i.e. the voltage Vcc is below the POR level. In this condition the bus connections of the transceiver must be in the POR state.

If the ground line of the electronic unit is interrupted, Vbat may be applied to the Vcc pin (measured relative to the original ground potential, to which the other units on the bus are connected).

7.12 Reverse Electronic Unit (ECU) Supply

If the connections for ground and supply voltage of an electronic unit (ECU) (max. 50V) which provides Vcc for the transceiver are exchanged, this transceiver has a ground potential which may be up to 50V higher than that of the other transceivers. In this case no transceiver must be destroyed even if several of them are connected via the bus system.

Any exchange among the six connections CANH1, CANH2, CANL1, CANL2, ground, and supply voltage of the electronic unit at the connector of the unit must never lead to the destruction of any transceiver of the bus system.

8.0 Electrical Characteristics

8.1 Definitions

All voltages are referenced to GND. Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

8.2 Absolute Maximum Ratings

Stresses above those listed in the following table may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage		-0.3	+7	V
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.25V$; no time limit	-45	+45	V
V_{TxD}	DC voltage at pin TxD		-0.3	V_{CC} + 0.3	V
V_{RxD}	DC voltage at pin RxD		-0.3	V_{CC} + 0.3	V
V_S	DC voltage at pin S		-0.3	V_{CC} + 0.3	V
V_{REF}	DC voltage at pin V_{REF}		-0.3	V_{CC} + 0.3	V
$V_{tran(CANH)}$	Transient voltage at pin CANH	Note 1	-150	+150	V
$V_{tran(CANL)}$	Transient voltage at pin CANL	Note 1	-150	+150	V
$V_{tran(VSPLIT)}$	Transient voltage at pin Vsplit	Note 1	-150	+150	V
$V_{esd(CANL/CANH)}$	ESD voltage at CANH and CANL pin	Note 2 Note 4	-8 -500	+8 +500	kV V
V_{esd}	ESD voltage at all other pins	Note 2 Note 4	-2 -250	+2 +250	kV V
Latch-up	Static latch-up at all pins	Note 3		100	mA
T_{stg}	Storage temperature		-55	+155	°C
T_{amb}	Ambient temperature		-40	+125	°C
T_{junc}	Maximum junction temperature		-40	+150	°C

Notes:
1) Applied transient waveforms in accordance with “ISO 7637 part 3”, test pulses 1, 2, 3a, and 3b (see Figure 4).
2) Standardized human body model (HBM) ESD pulses in accordance to MIL883 method 3015. Supply pin 8 is ±2 kV.
3) Static latch-up immunity: static latch-up protection level when tested according to EIA/JESD78.
4) Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3-1993.

8.3 Thermal Characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(vj-a)}$	Thermal resistance from junction to ambient in SO8 package	In free air	145	K/W
$R_{th(vj-s)}$	Thermal resistance from junction to substrate of bare die	In free air	45	K/W

8.4 DC Characteristics

V_{CC} = 4.75 to 5.25V; V_{33} = 2.9 to 3.6V; T_{junc} = -40 to +150°C; R_{LT} =60Ω unless specified otherwise.

Table 4: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply (pin V_{CC})						
I_{CC}	Supply current	Dominant; V_{TXD} =0V Recessive; V_{TXD} =V_{CC}		45 4	65 8	mA mA
Transmitter Data Input (pin TxD)						
V_{IH}	High-level input voltage	Output recessive	2.0	-	V_{CC}	V
V_{IL}	Low-level input voltage	Output dominant	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_{TXD} =V_{CC}	-1	0	+1	µA
I_{IL}	Low-level input current	V_{TXD} =0V	-75	-200	-350	µA
C_i	Input capacitance	Not tested	-	5	10	pF
Mode Select (pin S)						
V_{IH}	High-level input voltage	Silent mode	2.0	-	V_{CC}	V
V_{IL}	Low-level input voltage	High-speed mode	-0.3	-	+0.8	V
I_{IH}	High-level input current	V_S =2V	20	30	50	µA
I_{IL}	Low-level input current	V_{STB} =0.8V	15	30	45	µA
Receiver Data Output (pin RxD)						
V_{OH}	High-level output voltage	I_{RXD} = - 10mA	0.6 x V_{CC}	0.75 x V_{CC}		V
V_{OL}	Low-level output voltage	I_{RXD} = 6mA		0.25	0.45	V
I_{oh}	High-level output current	V_o=0.7 x V_{CC}	-5	-10	-15	mA
I_{ol}	Low-level output current	V_o=0.3 x V_{CC}	5	10	15	mA
Reference Voltage Output (pin V_{REF})						
V_{REF}	Reference output voltage	-50µA < I_{VREF} < +50µA	0.45 x V_{CC}	0.50 x V_{CC}	0.55 x V_{CC}	V
V_{REF_CM}	Reference output voltage for full common mode range	-35V <V_{CANH}< +35V; -35V <V_{CANL}< +35V	0.40 x V_{CC}	0.50 x V_{CC}	0.60 x V_{CC}	V
Bus Lines (pins CANH and CANL)						
$V_{o(reces)(CANH)}$	Recessive bus voltage at pin CANH	V_{TXD} =V_{CC}; no load	2.0	2.5	3.0	V
$V_{o(reces)(CANL)}$	Recessive bus voltage at pin CANL	V_{TXD} =V_{CC}; no load	2.0	2.5	3.0	V
$I_{o(reces)\ (CANH)}$	Recessive output current at pin CANH	-35V <V_{CANH}< +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive output current at pin CANL	-35V <V_{CANL} < +35V; 0V <V_{CC} < 5.25V	-2.5	-	+2.5	mA
$V_{o(dom)\ (CANH)}$	Dominant output voltage at pin CANH	V_{TXD} = 0V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant output voltage at pin CANL	V_{TXD} = 0V	0. 5	1.4	1.75	V
$V_{i(dif)\ (bus)}$	Differential bus input voltage (V_{CANH} - V_{CANL})	V_{TXD} = 0V; dominant; 42.5Ω < R_{LT} < 60Ω	1.5	2.25	3.0	V
		V_{TXD} =V_{CC}; recessive; no load	-120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short circuit output current at pin CANH	V_{CANH} =0V;V_{TXD} =0V	-45	-70	-95	mA
$I_{o(sc)\ (CANL)}$	Short circuit output current at pin CANL	V_{CANL} =36V; V_{TXD} =0V	45	70	120	mA
$V_{i(dif)(th)}$	Differential receiver threshold voltage	-5V <V_{CANL} < +12V; -5V <V_{CANH} < +12V; see Figure 5	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential receiver threshold voltage for high common-mode	-35V <V_{CANL} < +35V; -35V <V_{CANH} < +35V; see Figure 5	0.3	0.7	1.05	V
$V_{i(dif)\ (hys)}$	Differential receiver input voltage hysteresis	-35V <V_{CANL} < +35V; -35V <V_{CANH} < +35V; see Figure 5	50	70	100	mV
$R_{i(cm)(CANH)}$	Common-mode input resistance at pin CANH		15	26	37	KΩ
$R_{i(cm)\ (CANL)}$	Common-mode input resistance at pin CANL		15	26	37	KΩ
$R_{i(cm)(m)}$	Matching between pin CANH and pin CANL common-mode input resistance	V_{CANH} =V_{CANL}	-3	0	+3	%
$R_{i(dif)}$	Differential input resistance		25	50	75	KΩ
$C_{i(CANH)}$	Input capacitance at pin CANH	V_{TXD} =V_{CC}; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	V_{TXD} =V_{CC}; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	V_{TXD} =V_{CC}; not tested		3.75	10	pF
$I_{LI(CANH)}$	Input leakage current at pin CANH	V_{CC} =0V; V_{CANH} = 5V	10	170	250	µA

Table 4: DC Characteristics (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bus Lines (pins CANH and CANL)						
$I_{LI(CANL)}$	Input leakage current at pin CANL	V_{CC} =0V; V_{CANL} = 5V	10	170	250	µA
$V_{CM-peak}$	Common-mode peak during transition from dom → rec or rec → dom	See Figure 8 and 9	-500		500	mV
$V_{CM-step}$	Difference in common-mode between dominant and recessive state	See Figure 8 and 9	-150		150	mV
Power-on-Reset						
PORL	POR level	CANH, CANL, V_{ref} in tri-state below POR level	2.2	3.5	4.7	V
Thermal Shutdown						
$T_{j(sd)}$	Shutdown junction temperature		140	160	190	°C
Timing Characteristics (see Figure 6 and 7)						
$t_{d(TxD-BUSon)}$	Delay TxD to bus active	V_S = 0V	40	85	130	ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	V_S = 0V	30	60	105	ns
$t_{d(BUSon-RXD)}$	Delay bus active to RxD	V_S = 0V	25	55	105	ns
$t_{d(BUSoff-RXD)}$	Delay bus inactive to RxD	V_S = 0V	65	100	155	ns
$t_{pd(rec-dom)}$	Propagation delay TxD to RxD from recessive to dominant	V_S = 0V	70		230	ns
$t_{d(dom-rec)}$	Propagation delay TxD to RxD from dominant to recessive	V_S = 0V	100		245	ns
$t_{dom(TXD)}$	TXD dominant time for time out	V_{TxD} = 0V	250	450	750	µs

8.5 Measurement Setups and Definitions

Schematics are given for single CAN transceiver.

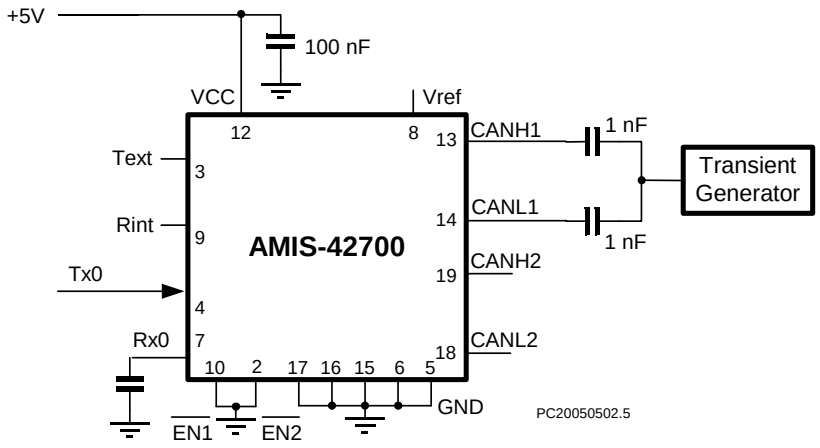


Figure 4: Test Circuit for Automotive Transients

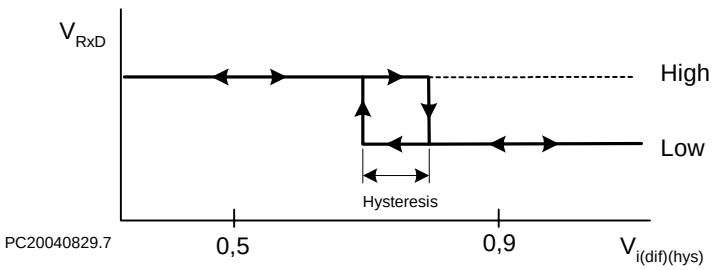


Figure 5: Hysteresis of the Receiver

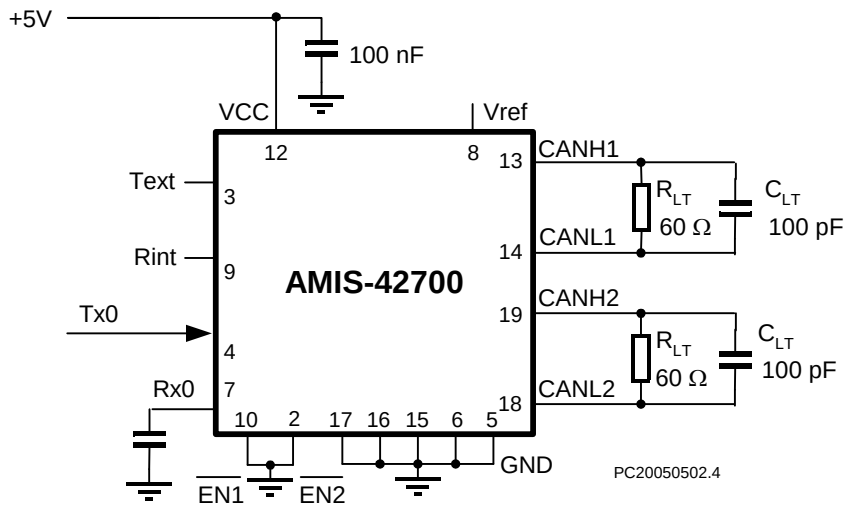


Figure 6: Test Circuit for Timing Characteristics

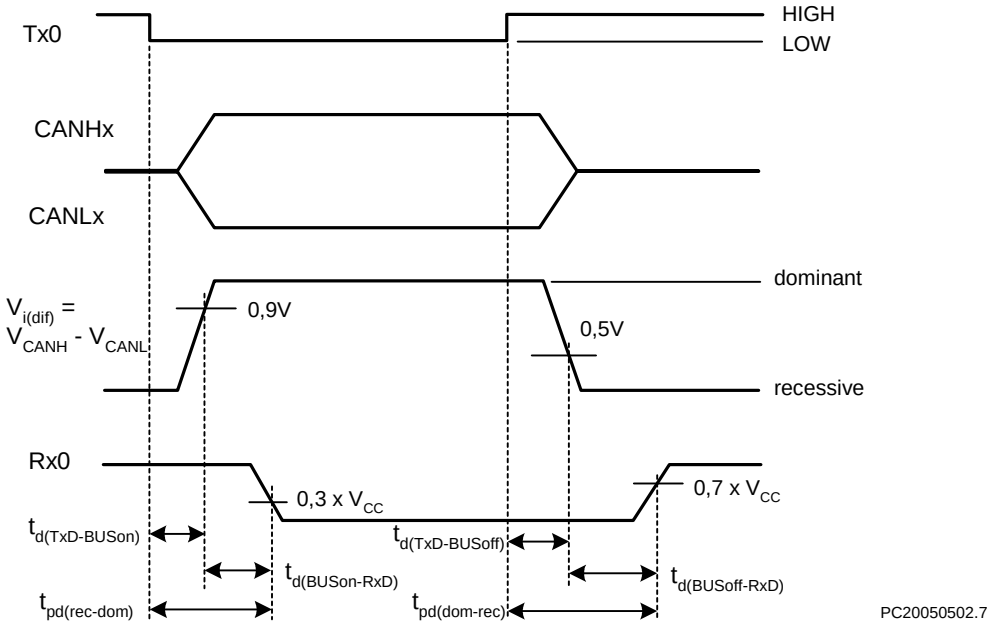


Figure 7: Timing Diagram for AC Characteristics

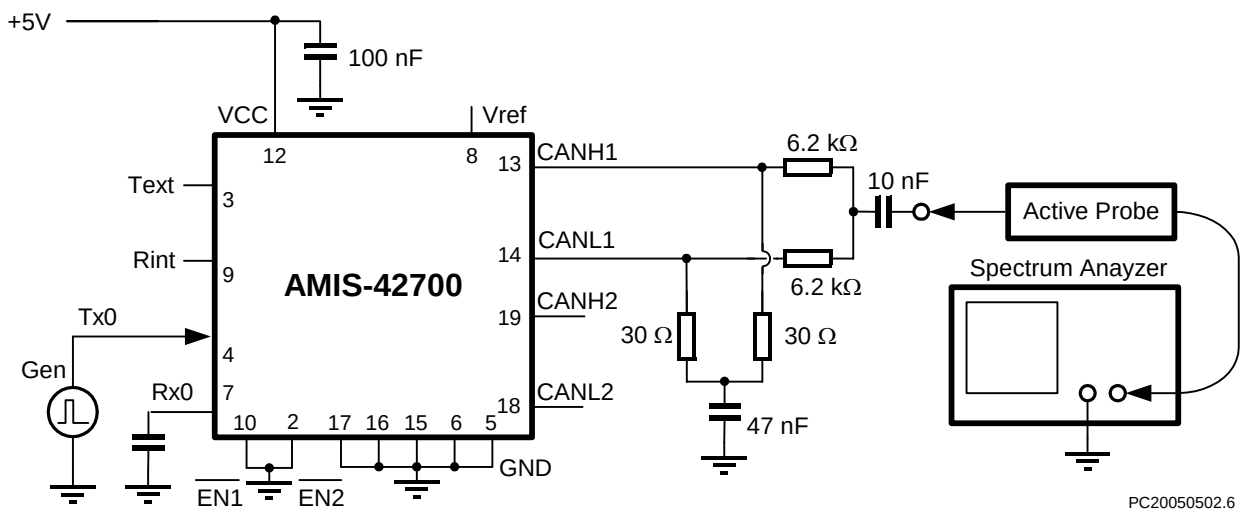


Figure 8: Basic Test Setup for Electromagnetic Measurement

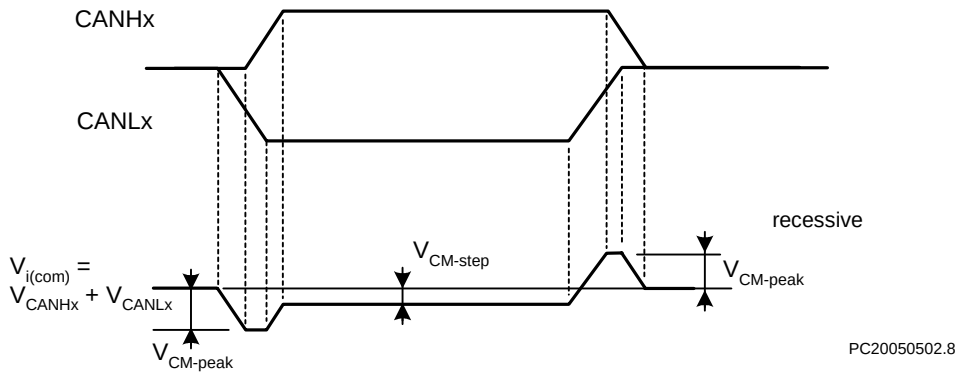
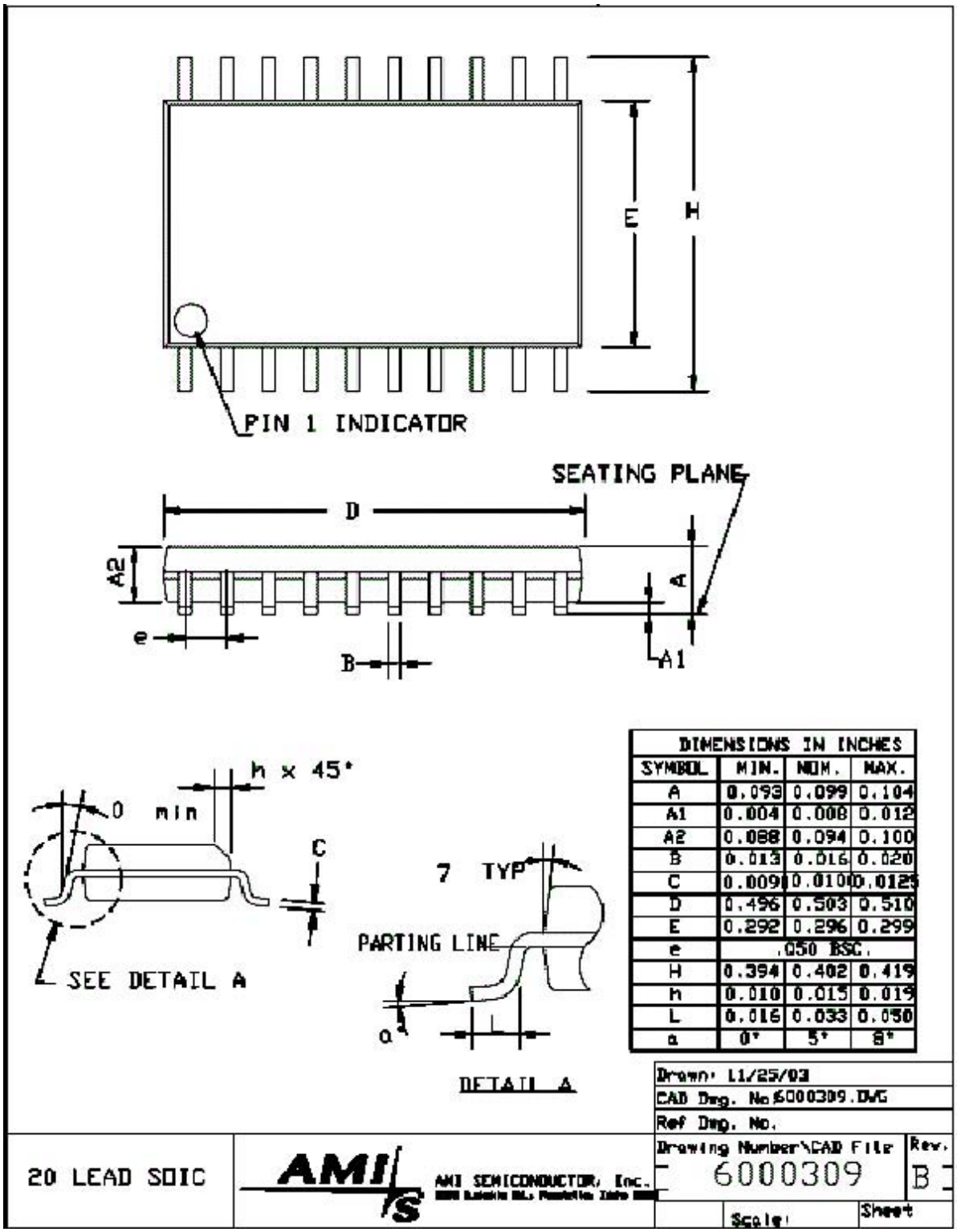


Figure 9: Common-mode Voltage Peaks (see measurement setup Figure 8)

9.0 Package Outline

SOIC-20: Plastic small outline; 20 leads; body width 300mil. AMIS reference: SOIC300 20 300 G



DIMENSIONS IN INCHES			
SYMBOL	MIN.	NOM.	MAX.
A	0.093	0.099	0.104
A1	0.004	0.008	0.012
A2	0.088	0.094	0.100
B	0.013	0.016	0.020
C	0.009	0.010	0.012
D	0.496	0.503	0.510
E	0.292	0.296	0.299
e	.050 BSC.		
H	0.394	0.402	0.419
h	0.010	0.015	0.019
L	0.016	0.033	0.050
α	0°	5°	8°

10.0 Soldering

10.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

10.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen-printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for re-flowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical re-flow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferably be kept below 230°C.

10.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems the double-wave soldering method was specifically developed. If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45º angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen-printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

10.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 11: Soldering Process

Package	Soldering Method	
	Wave	Re-flow(1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

11.0 Company or Product Inquiries

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