查询AM26C31CDBLE供应商

 Meets or Exceeds the Requirements of TIA/EIA-422-B and ITU Recommendation V.11

- Low Power, $I_{CC} = 100 \ \mu A Typ$
- Operates From a Single 5-V Supply
- High Speed, t_{PLH} = t_{PHL} = 7 ns Typ
- Low Pulse Distortion, t_{sk(p)} = 0.5 ns Typ
- High Output Impedance in Power-Off Conditions
- Improved Replacement for AM26LS31
- Available in Q-Temp Automotive
 - High-Reliability Automotive Applications
 - Configuration Control/Print Support
 - Qualification to Automotive Standards

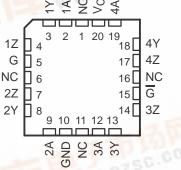
description/ordering information

The AM26C31 is a differential line driver with complementary outputs, designed to meet the requirements of TIA/EIA-422-B and ITU (formerly CCITT). The 3-state outputs have high-current capability for driving balanced lines, such as twisted-pair or parallel-wire transmission lines, and they provide the high-impedance state in the power-off condition. The enable functions are common to all four drivers and offer the choice of an active-high (G) or active-low (\overline{G}) enable input. BiCMOS circuitry reduces power consumption without sacrificing speed.

捷多邦,专业PCB打样工厂,24小时加急出货 AM26C31 QUADRUPLE DIFFERENTIAL LINE DRIVER

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AM26C31M J O AM26C31Q [AM26C31C D, DB, N AM26C31I D, DB, N, N	D PACKAGE I, OR NS PACKAGE						
(TOP VI	EW)						
1A [1 1Y [2 1Z [3 G [4 2Z [5 2Y [6 2A [7 GND [8	16 V _{CC} 15 4A 14 4Y 13 4Z 12 G 11 3Z 10 3Y 9 3A						
AM26C31M FK PACKAGE (TOP VIEW)							



NC – No internal connection

The AM26C31C is characterized for operation from 0° C to 70° C, the AM26C31I is characterized for operation from -40° C to 85° C, the AM26C31Q is characterized for operation over the automotive temperature range of -40° C to 125° C, and the AM26C31M is characterized for operation over the full military temperature range of -55° C to 125° C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



Copyright © 2004, Texas Instruments Incorporated On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

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description/ordering information (continued)

T _A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING				
	PDIP (N)	Tube of 25	AM26C31CN	AM26C31CN				
		Tube of 40	AM26C31CD					
0°C to 70°C	SOIC (D)	Reel of 2500	AM26C31CDR	AM26C31C				
	SOP (NS)	Reel of 2000	AM26C31CNSR	26C31				
	SSOP (DB)	Reel of 2000	AM26C31CDBR	26C31				
	PDIP (N)	Tube of 25	AM26C31IN	AM26C31IN				
		Tube of 40	AM26C31ID	444000040				
4000 1- 0500	SOIC (D)	Reel of 2500	AM26C31IDR	AM26C31C				
–40°C to 85°C	SOP (NS)	Reel of 2000	AM26C31INSR	26C31				
	SSOP (DB)	Reel of 2000	AM26C31IDBR	26C31				
	TSSOP (PW)	Tube of 90	AM26C31IPW	26C31I				
4000 1- 40500		Tube of 40	AM26C31QD	110000100				
–40°C to 125°C	SOIC (D)	Reel of 2500	AM26C31QDR	AM26C31QD				
	CDIP (J)	Tube of 25	AM26C31MJ	AM26C31MJ				
-55°C to 125°C	CFP (W)	Tube of 150	AM26C31MW	AM26C31MW				
	LCCC (FK)	Tube of 55	AM26C31MFK	AM26C31MFK				

ORDERING INFORMATION

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

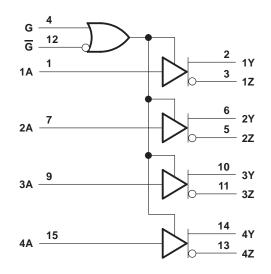
(each driver)								
INPUT	ENA	BLES	OUTPUTS					
Α	G	G	Y	Z				
Н	Н	Х	Н	L				
L	Н	Х	L	Н				
Н	Х	L	Н	L				
L	Х	L	L	Н				
Х	L	Н	Z	Z				

FUNCTION TABLE

H = High level, L = Low level, X = Irrelevant, Z = High impedance (off)



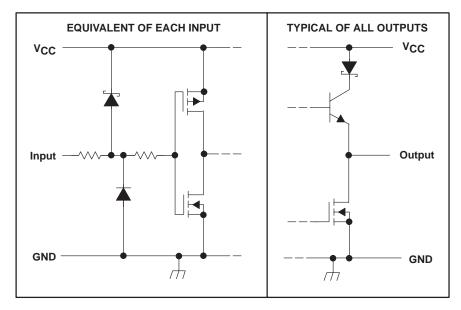
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logic diagram (positive logic)

Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

schematics of inputs and outputs





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC} (see Note 1) Input voltage range, V_1 Differential input voltage range, V_{ID} Output voltage range, V_O Input or output clamp current, I_{IK} or I_{OK} Output current, I_O V_{CC} current GND current Package thermal impedance, θ_{JA} (see Notes 2 and 3):	-0.5 V to V _{CC} + 0.5 V -14 V to 14 V -0.5 V to 7 V ±20 mA ±150 mA -200 mA
Operating virtual junction temperature, T _J Storage temperature range, T _{stg}	150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential output voltage (VOD), are with respect to the network ground terminal.
 - 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 - 3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		4.5	5	5.5	V
VID	Differential input voltage			±7		V
V_{IH}	High-level input voltage		2			V
VIL	VIL Low-level input voltage				0.8	V
IOH	IOH High-level output current				-20	mA
IOL	Low-level output current				20	mA
		AM26C31C	0		70	
	Operating free air temperature	AM26C31I	-40		85	°C
TA	Operating free-air temperature	AM26C31Q	-40		125	C
		AM26C31M	-55		125	



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		AM26C31C AM26C31I			UNIT
				MIN	TYP [†]	MAX	
VOH	High-level output voltage	I _O = -20 mA		2.4	3.4		V
VOL	Low-level output voltage	I _O = 20 mA			0.2	0.4	V
Vod	Differential output voltage magnitude	R _L = 100 Ω,	See Figure 1	2	3.1		V
$\Delta V_{OD} $	Change in magnitude of differential output voltage‡	R _L = 100 Ω,	See Figure 1			±0.4	V
Voc	Common-mode output voltage	R _L = 100 Ω,	See Figure 1			3	V
	Change in magnitude of common-mode output voltage [‡]	R _L = 100 Ω,	See Figure 1			±0.4	V
Ц	Input current	$V_I = V_{CC}$ or G	ND			±1	μA
			V _O = 6 V			100	
IO(off)	Driver output current with power off	Λ CC = 0	V _O = -0.25 V			-100	μA
los	Driver output short-circuit current	$V_{O} = 0$	•	-30		-150	mA
		V _O = 2.5 V				20	
IOZ	High-impedance off-state output current	V _O = 0.5 V				-20	μA
			$V_{I} = 0 V \text{ or } 5 V$			100	μA
ICC	Quiescent supply current	I _O = 0	V _I = 2.4 V or 0.5 V, See Note 4		1.5	3	mA
Ci	Input capacitance				6		pF

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C. [‡] Δ |V_{OD}| and Δ |V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

NOTE 4: This parameter is measured per input. All other inputs are at 0 or 5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		A A	UNIT		
				MIN	TYP†	MAX	
^t PLH	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2	3	7	12	ns
^t PHL	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2	3	7	12	ns
^t sk(p)	Pulse skew time (t _{PLH} – t _{PHL})	S1 is open,	See Figure 2		0.5	4	ns
^t r(OD), ^t f(OD)	Differential output rise and fall times	S1 is open,	See Figure 3		5	10	ns
^t PZH	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
tPZL	Output enable time to low level	S1 is closed,	See Figure 4		10	19	ns
^t PHZ	Output disable time from high level	S1 is closed,	See Figure 4		7	16	ns
^t PLZ	Output disable time from low level	S1 is closed,	See Figure 4		7	16	ns
C _{pd}	Power dissipation capacitance (each driver) (see Note 5)	S1 is open,	See Figure 2		170		pF

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C. NOTE 5: C_{pd} is used to estimate the switching losses according to P_D = C_{pd} × V_{CC}² × f, where f is the switching frequency.



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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		AM26C31Q AM26C31M			UNIT
				MIN	TYP†	MAX	
VOH	High-level output voltage	$I_{O} = -20 \text{ mA}$		2.2	3.4		V
VOL	Low-level output voltage	I _O = 20 mA			0.2	0.4	V
IVODI	Differential output voltage magnitude	R _L = 100 Ω,	See Figure 1	2	3.1		V
$\Delta V_{OD} $	Change in magnitude of differential output voltage‡	R _L = 100 Ω,	See Figure 1			±0.4	V
Voc	Common-mode output voltage	R _L = 100 Ω,	See Figure 1			3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage [‡]	R _L = 100 Ω,	See Figure 1			±0.4	V
Ц	Input current	$V_I = V_{CC}$ or G	ND			±1	μA
		V _O :	V _O = 6 V			100	
lO(off)	Driver output current with power off	$V_{CC} = 0 \qquad \qquad V_{O} = -0.25 \text{ V}$				-100	μA
IOS	Driver output short-circuit current	VO = 0				-170	mA
		V _O = 2.5 V		20		20	
loz	High-impedance off-state output current	V _O = 0.5 V				-20	μA
		I _O = 0	$V_{I} = 0 V \text{ or } 5 V$			100	μA
ICC	Quiescent supply current	I ^O = 0	V _I = 2.4 V or 0.5 V, See Note 4			3.2	mA
Ci	Input capacitance				6		pF

[†] All typical values are at $V_{CC} = 5$ V and $T_A = 25^{\circ}$ C. [‡] $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level.

NOTE 4: This parameter is measured per input. All other inputs are at 0 V or 5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

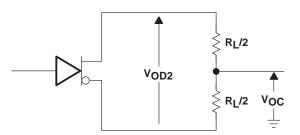
PARAMETER		TEST C	TEST CONDITIONS		AM26C31Q AM26C31M		
				MIN	TYP†	MAX	
^t PLH	Propagation delay time, low- to high-level output	S1 is open,	See Figure 2		7	12	ns
^t PHL	Propagation delay time, high- to low-level output	S1 is open,	See Figure 2		6.5	12	ns
^t sk(p)	Pulse skew time (tPLH - tPHL)	S1 is open,	See Figure 2		0.5	4	ns
^t r(OD), ^t f(OD)	Differential output rise and fall times	S1 is open,	See Figure 3		5	12	ns
^t PZH	Output enable time to high level	S1 is closed,	See Figure 4		10	19	ns
^t PZL	Output enable time to low level	S1 is closed,	See Figure 4		10	19	ns
^t PHZ	Output disable time from high level	S1 is closed,	See Figure 4		7	16	ns
^t PLZ	Output disable time from low level	S1 is closed,	See Figure 4		7	16	ns
C _{pd}	Power dissipation capacitance (each driver) (see Note 5)	S1 is open,	See Figure 2		100		pF

[†] All typical values are at V_{CC} = 5 V and T_A = 25°C. NOTE 5: C_{pd} is used to estimate the switching losses according to P_D = C_{pd} × V_{CC}² × f, where f is the switching frequency.

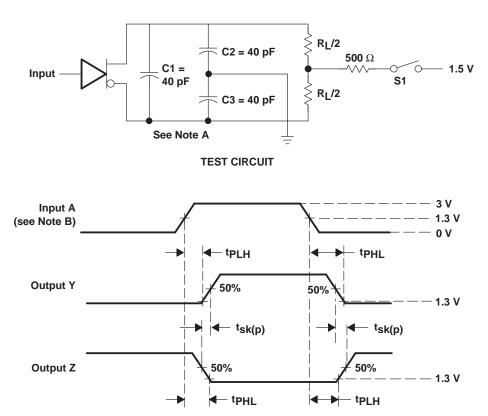


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PARAMETER MEASUREMENT INFORMATION





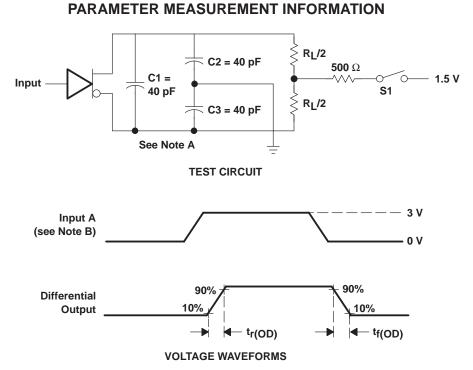


NOTES: A. C1, C2, and C3 include probe and jig capacitance. B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, and t_r, t_f \leq 6 ns.

Figure 2. Propagation Delay Time and Skew Waveforms and Test Circuit



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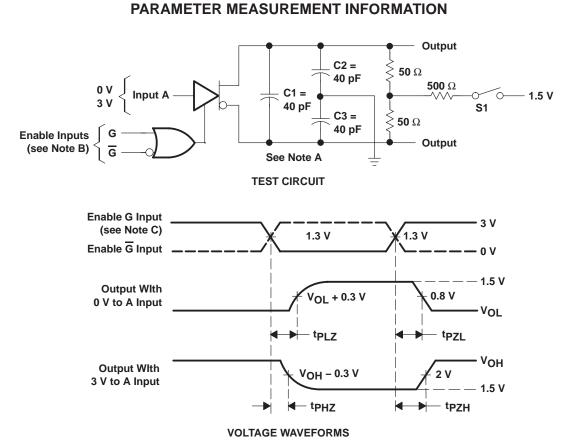
NOTES: A. C1, C2, and C3 include probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: $PRR \le 1$ MHz, duty cycle $\le 50\%$, and t_r , $t_f \le 6$ ns.

Figure 3. Differential-Output Rise- and Fall-Time Waveforms and Test Circuit



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- NOTES: A. C1, C2, and C3 includes probe and jig capacitance.
 - B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, duty cycle \leq 50%, t_r < 6 ns, and t_f < 6 ns.
 - C. Each enable is tested separately.

Figure 4. Output Enable- and Disable-Time Waveforms and Test Circuit



SLLS103K – DECEMBER 1990 – REVISED SEPTEMBER 2004

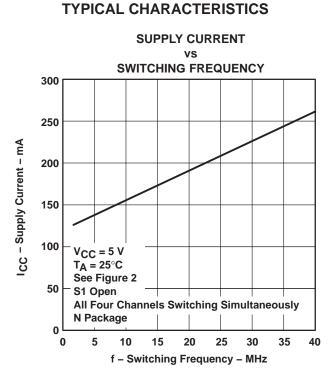


Figure 5





PACKAGE OPTION ADDENDUM

11-Feb-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9163901Q2A	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
5962-9163901QEA	ACTIVE	CDIP	J	16	1	None	A42 SNPB	Level-NC-NC-NC
5962-9163901QFA	ACTIVE	CFP	W	16	1	None	A42 SNPB	Level-NC-NC-NC
AM26C31CD	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
AM26C31CDBLE	OBSOLETE	SSOP	DB	16		None	Call TI	Call TI
AM26C31CDBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26C31CDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
AM26C31CN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
AM26C31CNSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26C31ID	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
AM26C31IDBLE	OBSOLETE	SSOP	DB	16		None	Call TI	Call TI
AM26C31IDBR	ACTIVE	SSOP	DB	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26C31IDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR
AM26C31IN	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
AM26C31INSR	ACTIVE	SO	NS	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
AM26C31IPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
AM26C31MFKB	ACTIVE	LCCC	FK	20	1	None	POST-PLATE	Level-NC-NC-NC
AM26C31MJB	ACTIVE	CDIP	J	16	1	None	A42 SNPB	Level-NC-NC-NC
AM26C31MWB	ACTIVE	CFP	W	16	1	None	A42 SNPB	Level-NC-NC-NC
AM26C31QD	ACTIVE	SOIC	D	16	40	None	CU NIPDAU	Level-1-220C-UNLIM
AM26C31QDR	ACTIVE	SOIC	D	16	2500	None	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens,

including bromine (Br) or antimony (Sb) above 0.1% of total product weight.



PACKAGE OPTION ADDENDUM

11-Feb-2005

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

J (R-GDIP-T**) 14 LEADS SHOWN

PINS ** 14 16 20 18 DIM 0.300 0.300 0.300 0.300 В Α (7,62) (7,62) (7,62) (7,62) BSC BSC BSC BSC 14 8 0.785 .840 0.960 1.060 B MAX (19, 94)(21, 34)(24, 38)(26, 92)B MIN С 0.300 0.300 0.310 0.300 C MAX (7, 62)(7, 62)(7, 87)(7, 62)7 0.245 0.245 0.220 0.245 0.065 (1,65) C MIN (6, 22)(6,22) (5, 59)(6,22) 0.045 (1,14) 0.060 (1,52) ← 0.005 (0,13) MIN Α 0.015 (0,38) 0.200 (5,08) MAX Seating Plane 0.130 (3,30) MIN 0.026 (0,66) 0.014 (0,36) 0'-15' 0.100 (2,54) 0.014 (0,36) 0.008 (0,20) 4040083/F 03/03

CERAMIC DUAL IN-LINE PACKAGE

NOTES: A. All linear dimensions are in inches (millimeters).

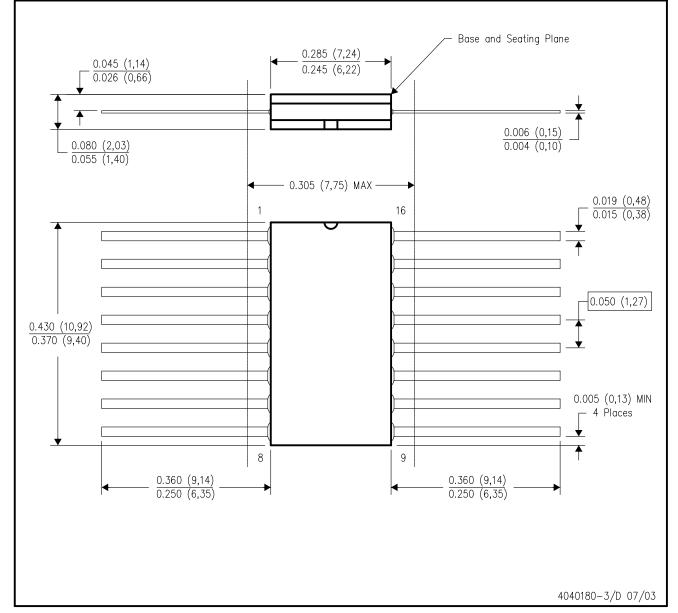
B. This drawing is subject to change without notice.

- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



NOTES:

: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

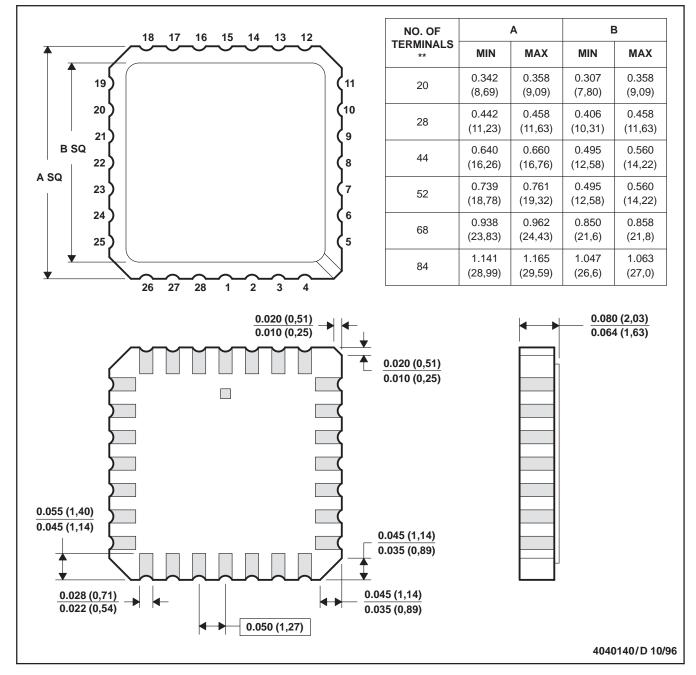


MECHANICAL DATA

MLCC006B - OCTOBER 1996

LEADLESS CERAMIC CHIP CARRIER

FK (S-CQCC-N**) 28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

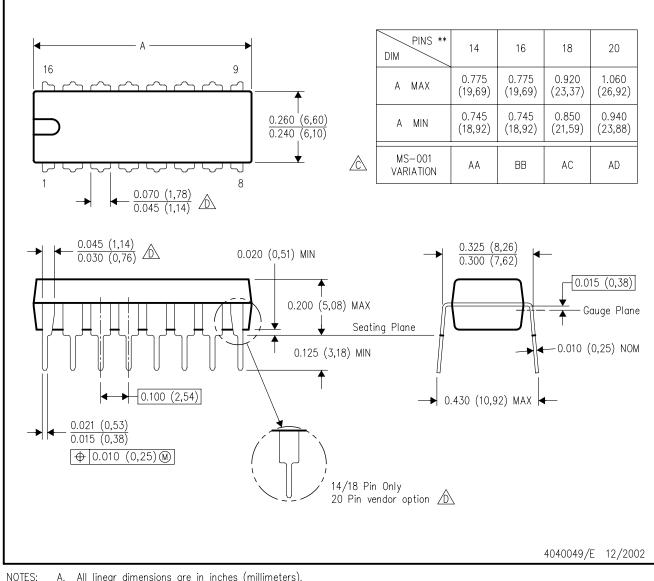
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

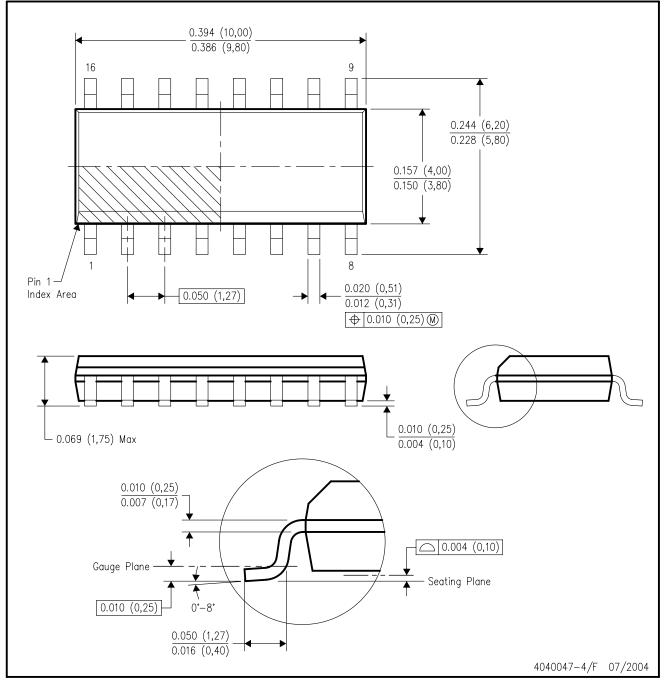
🖄 Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



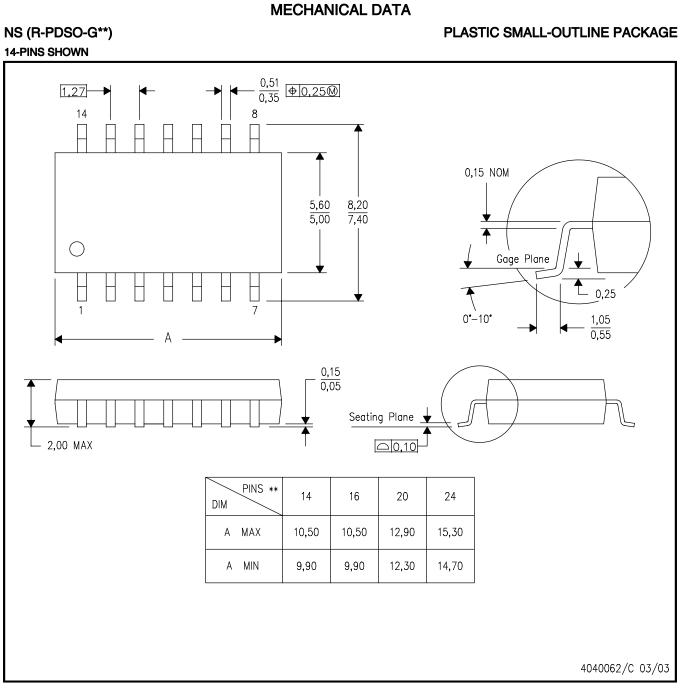
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

D. Falls within JEDEC MS-012 variation AC.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

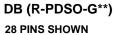
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

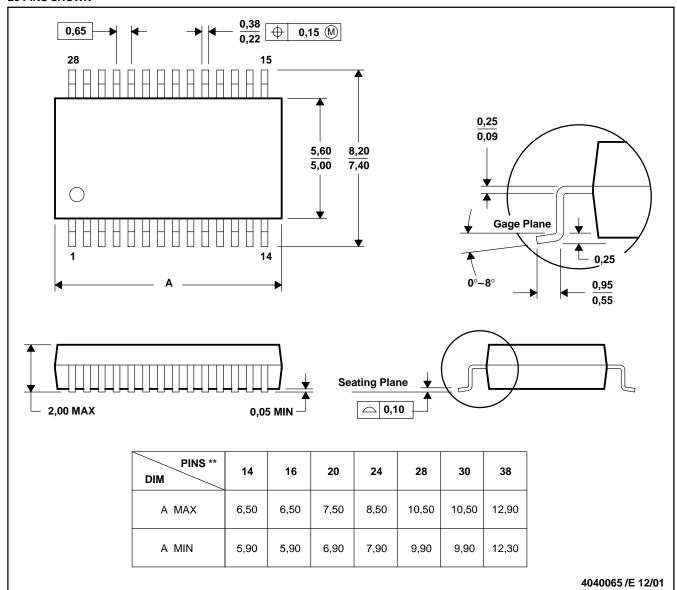


MECHANICAL DATA

MSSO002E - JANUARY 1995 - REVISED DECEMBER 2001

PLASTIC SMALL-OUTLINE





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150



MECHANICAL DATA

MTSS001C - JANUARY 1995 - REVISED FEBRUARY 1999

PLASTIC SMALL-OUTLINE PACKAGE





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



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