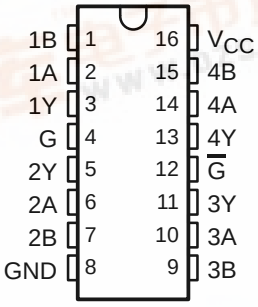
AM26LS32AC, AM26LS32AI, AM26LS33AC, AM26LS32AM, AM26LS33AM QUADRUPLE DIFFERENTIAL LINE RECEIVERS

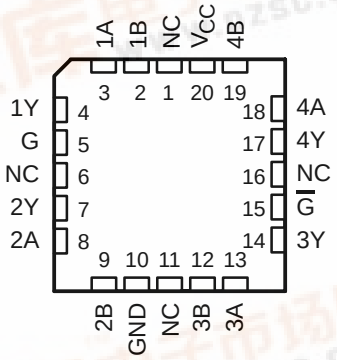
SLLS115D – OCTOBER 1980 – REVISED MARCH 2002

- **AM26LS32A Devices Meet or Exceed the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Devices Have ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS33A Devices Have ±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operate From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 kΩ Min**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

AM26LS32AC . . . D, N, OR NS PACKAGE
AM26LS32AI, AM26LS33AC . . . D OR N PACKAGE
AM26LS32AM, AM26LS33AM . . . J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The AM26LS32A and AM26LS33A devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AI is characterized for operation from –40°C to 85°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of –55°C to 125°C.

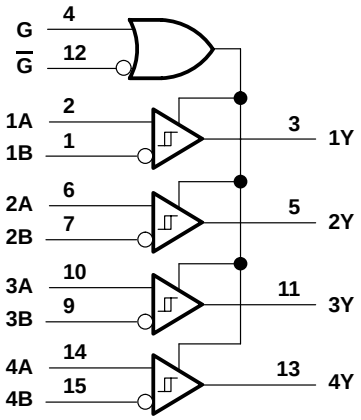
AM26LS32 and AM26LS33 are trademarks of Advanced Micro Devices, Inc.

FUNCTION TABLE
(each receiver)

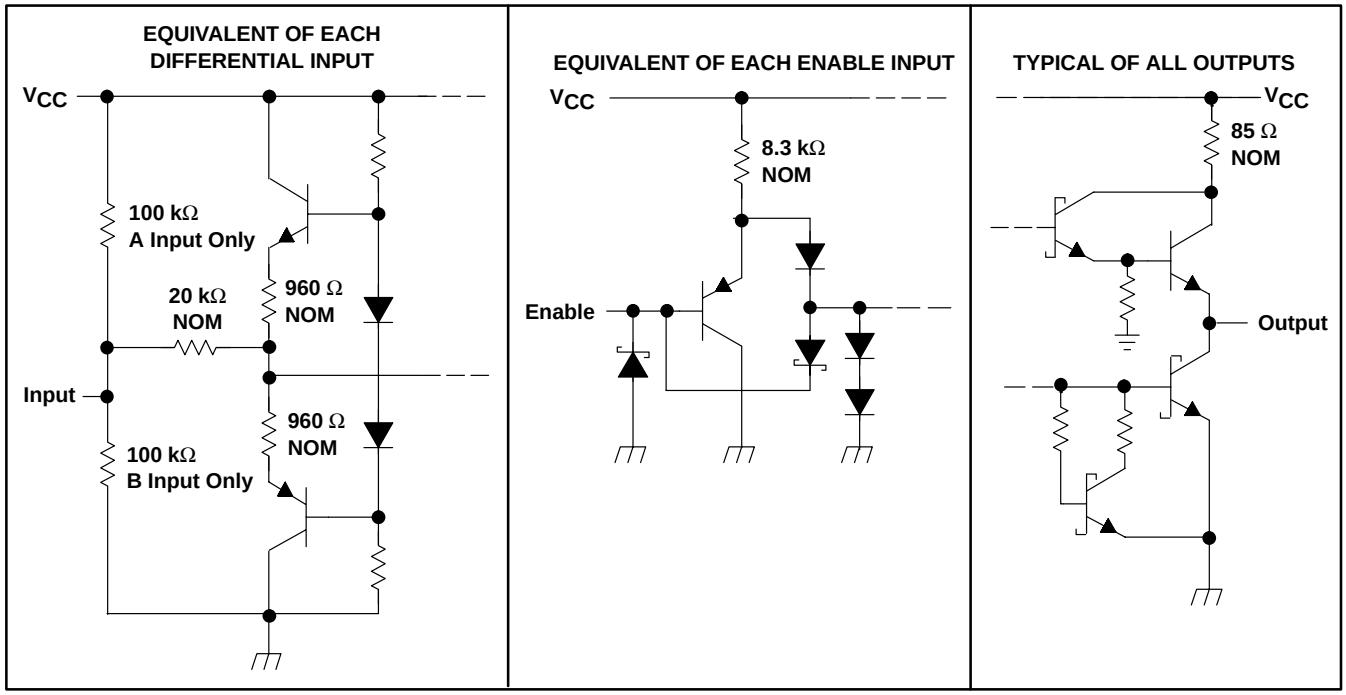
DIFFERENTIAL A – B	ENABLES		OUTPUT Y
	G	$\overline{G}$	
$V_{ID} \geq V_{IT+}$	H	X	H
	X	L	H
$V_{IT-} \leq V_{ID} \leq V_{IT+}$	H	X	?
	X	L	?
$V_{ID} \leq V_{IT-}$	H	X	L
	X	L	L
X	L	H	Z
Open	H	X	H
	X	L	H

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I: Any differential input . . . . . ±25 V
Other inputs . . . . . 7 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±25 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Package thermal impedance, θ_{JA} (see Note 3): D package . . . . . 73°C/W
N package . . . . . 67°C/W
NS package . . . . . 64°C/W
Case temperature for 60 seconds, T_C: FK package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or N package . . . . . 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package . . . . . 300°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting (A) input terminals with respect to the inverting (B) input terminals.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	275 mW

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	AM26LS32AC, AM26LS32AI, AM26LS33AC	4.75	5	5.25	V
		AM26LS32AM, AM26LS33AM	4.5	5	5.5	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Common-mode input voltage	AM26LS32A			±7	V
		AM26LS33A			±15	
I_{OH}	High-level output current				–440	μA
I_{OL}	Low-level output current				8	mA
T_A	Operating free-air temperature	AM26LS32AC, AM26LS33AC	0		70	°C
		AM26LS32AI	–40		85	
		AM26LS32AM, AM26LS33AM	–55		125	

electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

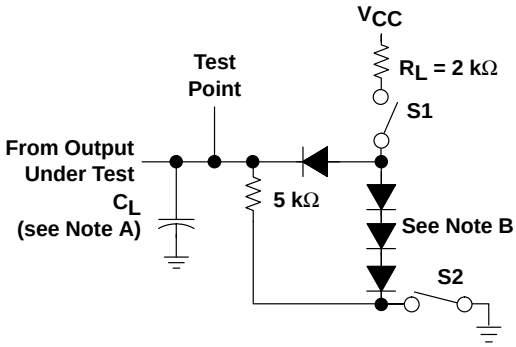
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going input threshhold voltage	$V_O = V_{OH}$min, I_{OH} = –440 μA	AM26LS32A			0.2	V
			AM26LS33A			0.5	
$V_{IT–}$	Negative-going input threshhold voltage	V_O = 0.45 V, I_{OL} = 8 mA	AM26LS32A	–0.2‡			V
			AM26LS33A	–0.5‡			
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT–}$)				50		mV
V_{IK}	Enable-input clamp voltage	V_{CC} = MIN,	I_I = –18 mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} =MIN, V_{ID} = 1 V, $V_{I(G)}$ = 0.8 V, I_{OH} = –440 μA	AM26LS32AC AM26LS33AC	2.7			V
			AM26LS32AM, AM26LS32AI, AM26LS33AM	2.5			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = –1 V, $V_{I(G)}$ = 0.8 V	I_{OL} = 4 mA			0.4	V
			I_{OL} = 8 mA			0.45	
I_{OZ}	Off-state (high-impedance state) output current	V_{CC} = MAX	V_O = 2.4 V			20	μA
			V_O = 0.4 V			–20	
I_I	Line input current	V_I = 15 V,	Other input at –10 V to 15 V			1.2	mA
		V_I = –15 V,	Other input at –15 V to 10 V			–1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V				100	μA
I_{IH}	High-level enable current	V_I = 2.7 V				20	μA
I_{IL}	Low-level enable current	V_I = 0.4 V				–0.36	mA
r_I	Input resistance	V_{IC} = –15 V to 15 V,	One input to ac ground	12	15		kΩ
I_{OS}	Short-circuit output current§	V_{CC} = MAX		–15		–85	mA
I_{CC}	Supply current	V_{CC} = MAX,	All outputs disabled		52	70	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
‡ The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
§ Not more than one output should be shorted to ground at a time, and duration of the short circuit should not exceed one second.

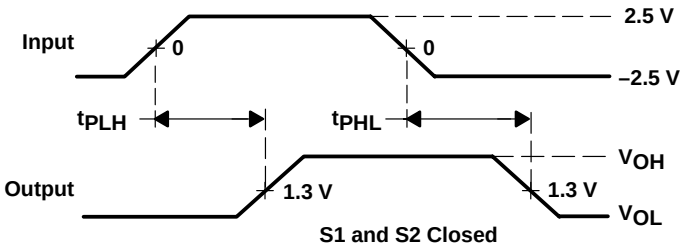
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level				20	25	
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level				30	40	

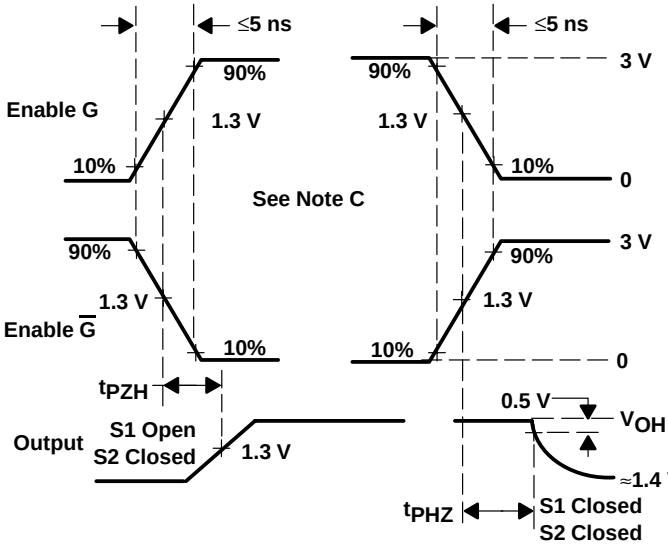
PARAMETER MEASUREMENT INFORMATION



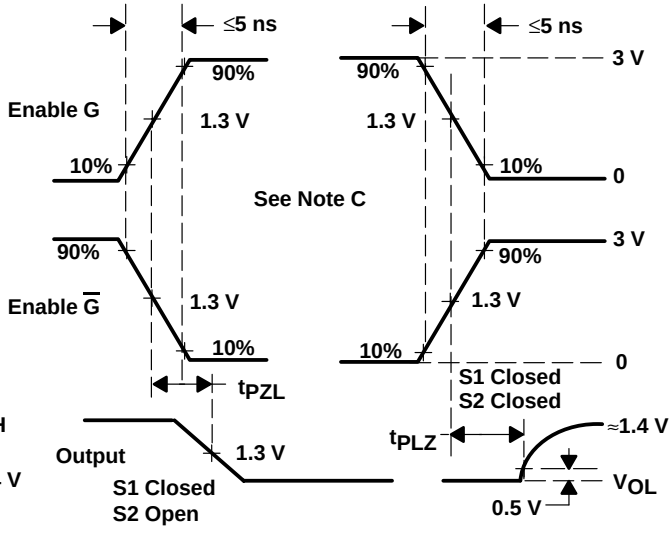
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



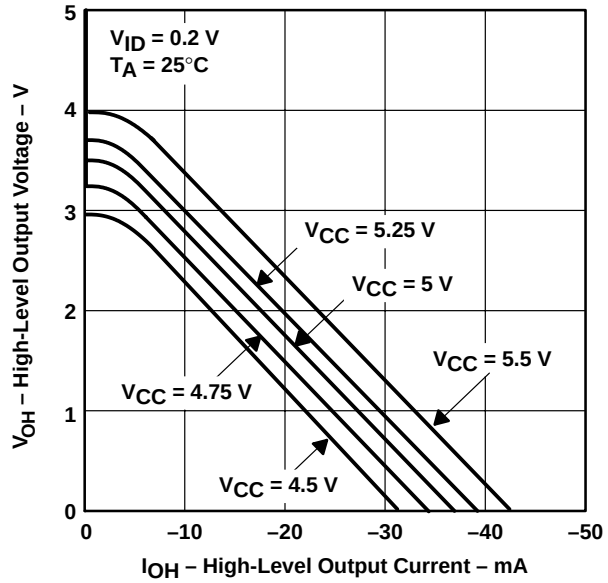
VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

Figure 1

TYPICAL CHARACTERISTICS

**HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT†**



† V_{CC} = 5.5 V and V_{CC} = 4.5 V applies to M-suffix devices only.

Figure 2

**HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

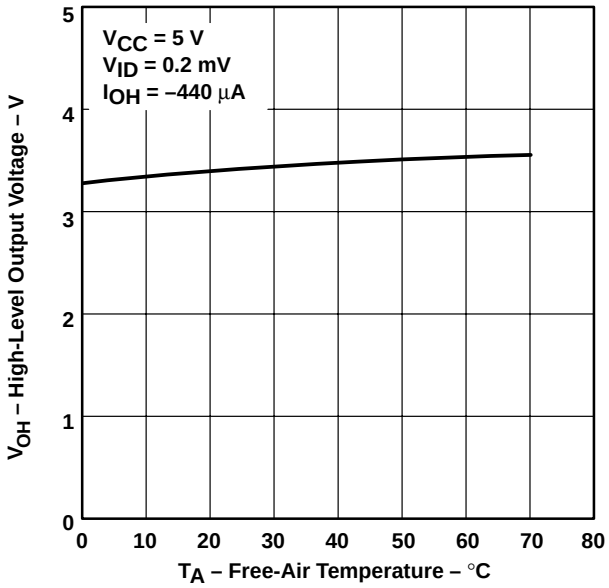


Figure 3

**LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT**

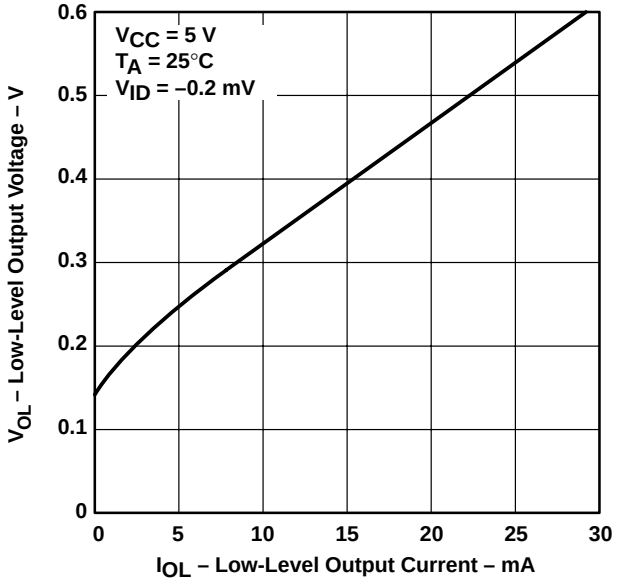


Figure 4

**LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE**

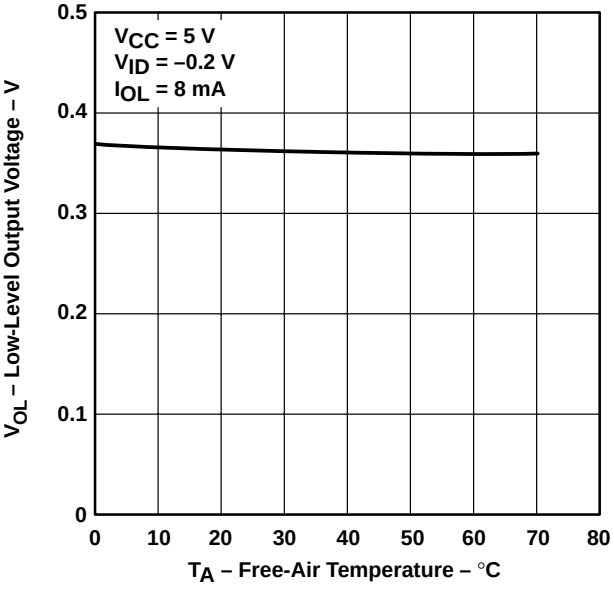


Figure 5

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

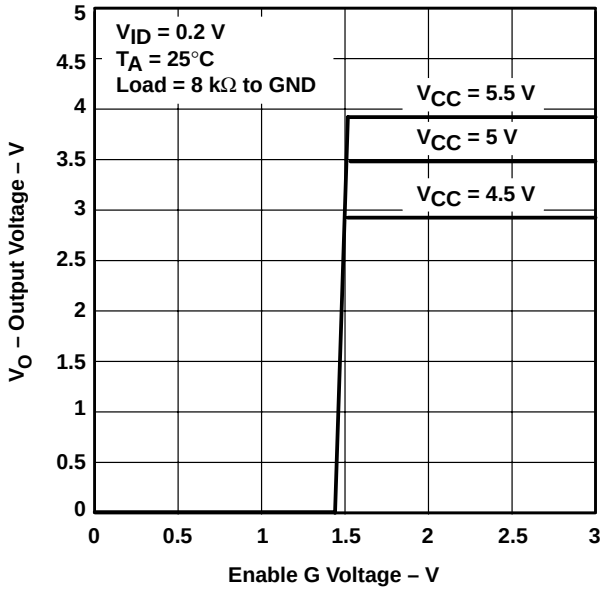


Figure 6

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

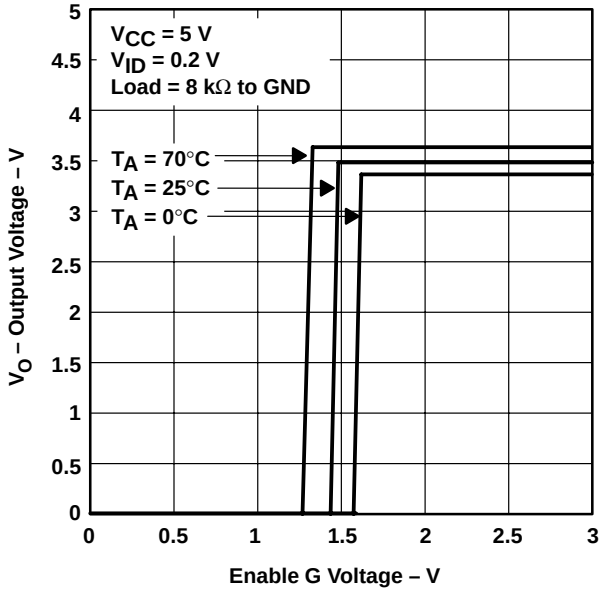


Figure 7

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

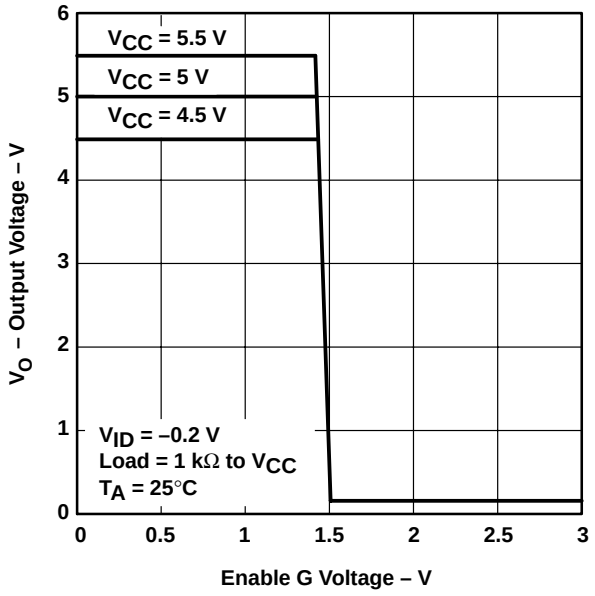


Figure 8

OUTPUT VOLTAGE vs ENABLE G VOLTAGE

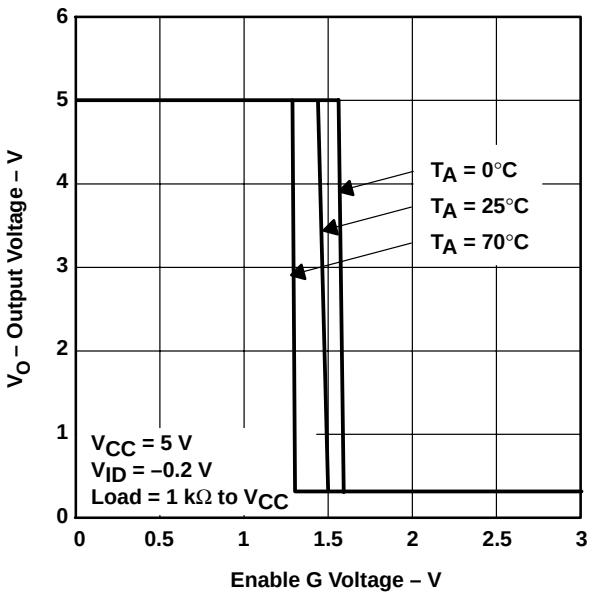


Figure 9

TYPICAL CHARACTERISTICS

AM26LS32A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

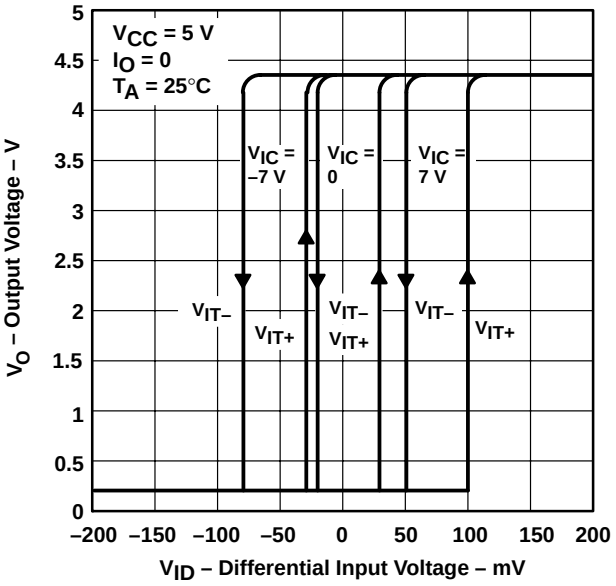


Figure 10

AM26LS33A
OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

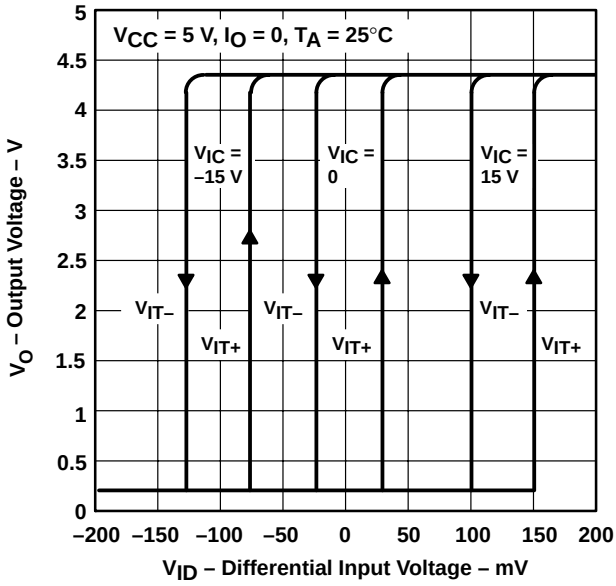
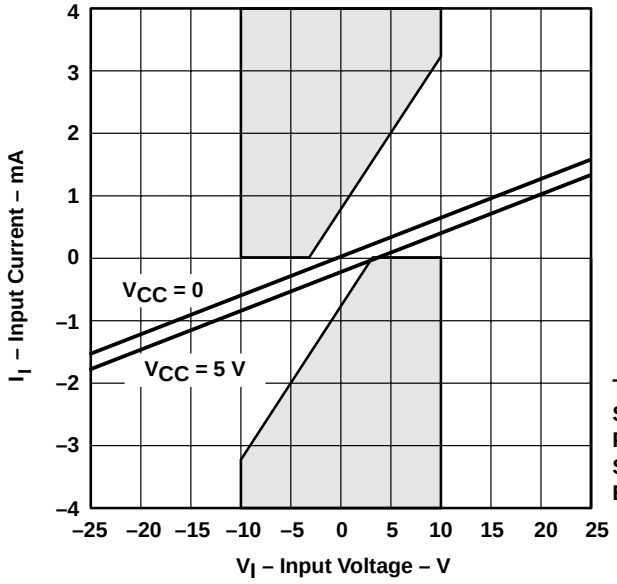


Figure 11

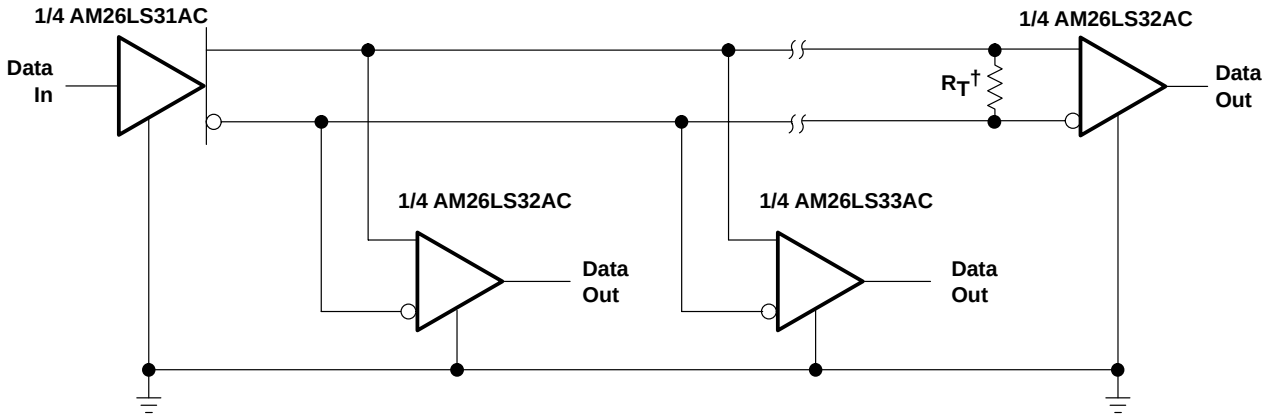
INPUT CURRENT
vs
INPUT VOLTAGE



The Unshaded Area Shows Requirements of Paragraph 4.2.1 of ANSI Standards EIA/TIA-422-B and EIA/TIA-423-B.

Figure 12

APPLICATION INFORMATION



† R_T equals the characteristic impedance of the line.

Figure 13. Circuit With Multiple Receivers

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
5962-7802003M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-7802003MEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7802003MFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7802004M2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-7802004MEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7802004MFA	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS32ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32ACNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32ACNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS32AIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32AINE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS32AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
AM26LS32AMJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS32AMJB	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS32AMWB	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS33ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACDRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AM26LS33ACDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
AM26LS33ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS33ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
AM26LS33AMFKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
AM26LS33AMJ	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS33AMJB	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
AM26LS33AMWB	ACTIVE	CFP	W	16	1	TBD	A42 SNPB	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

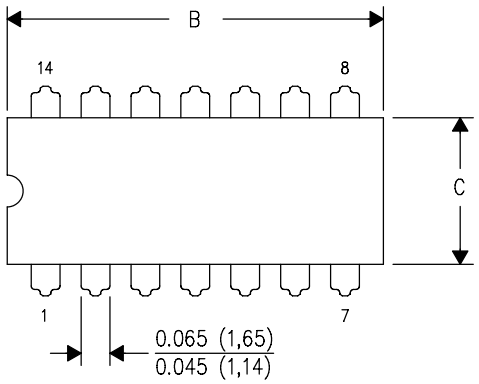
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

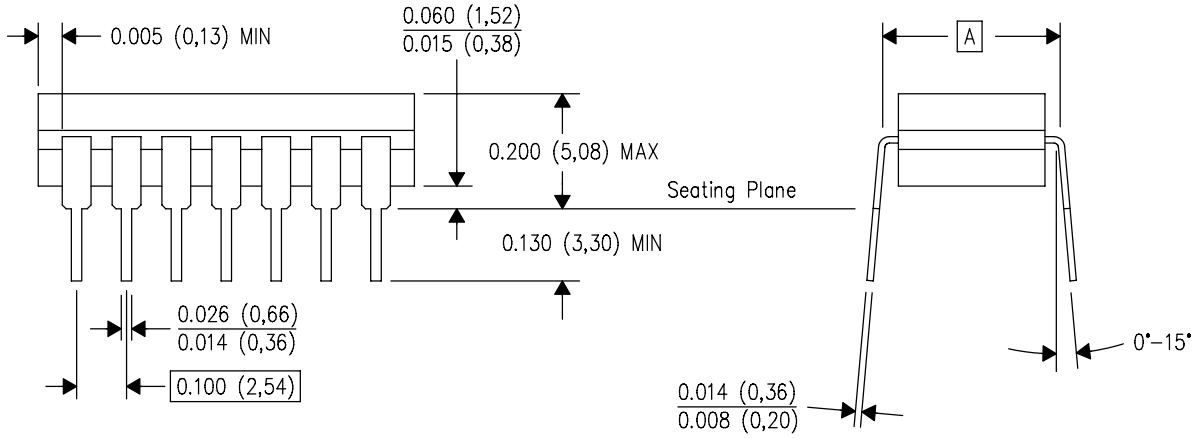
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



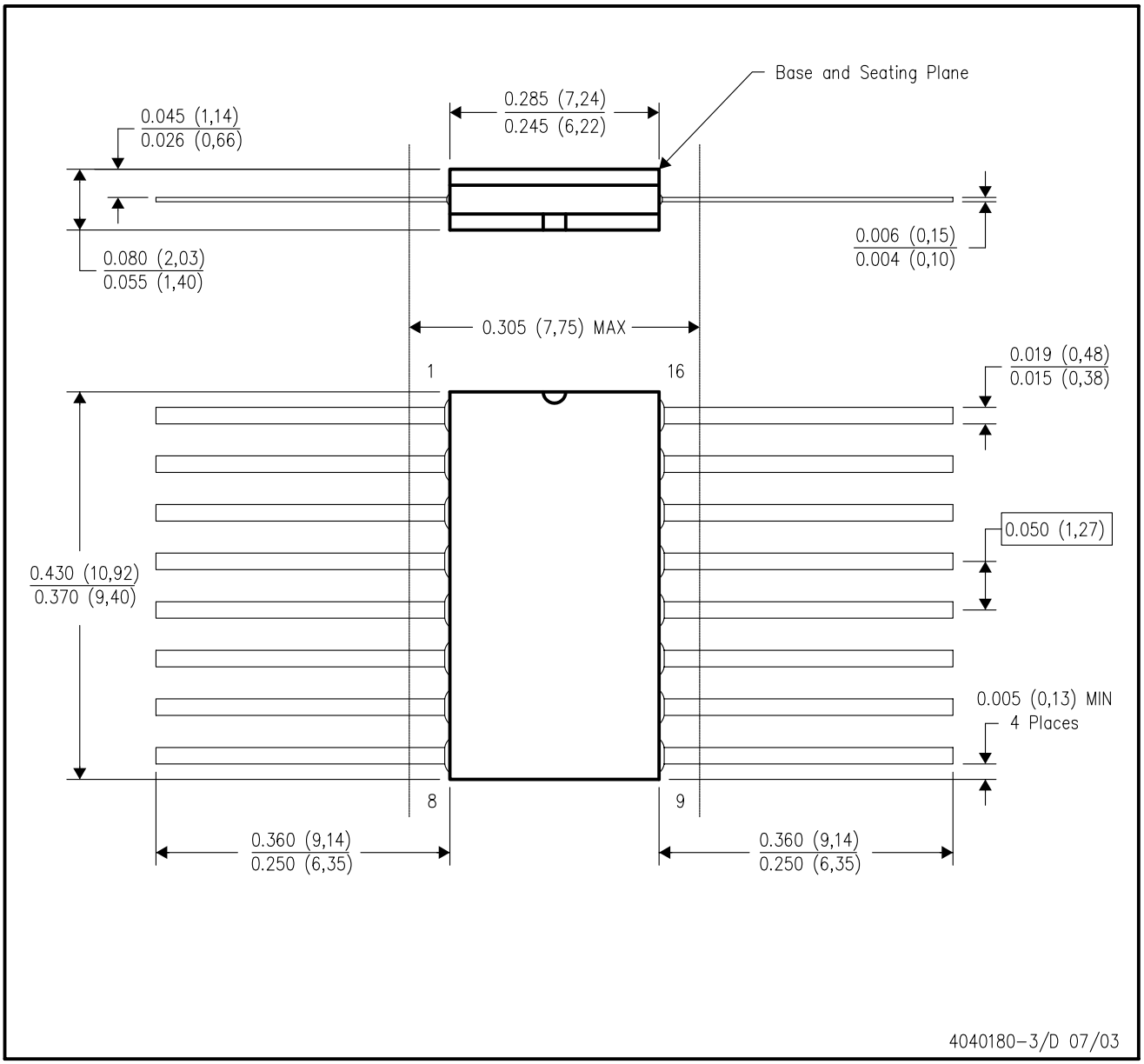
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

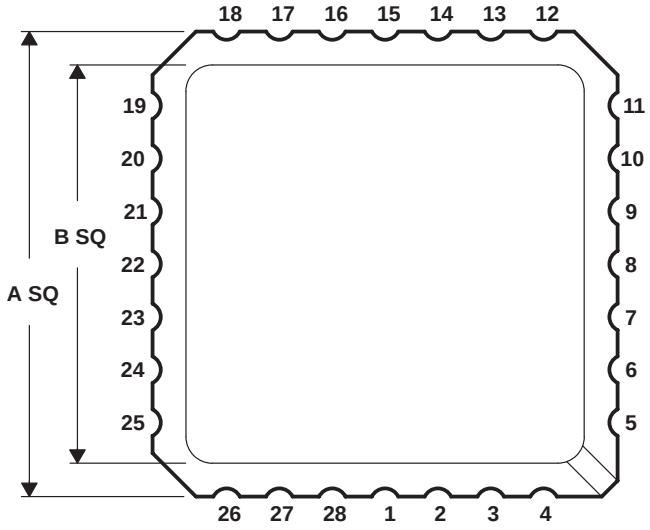
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



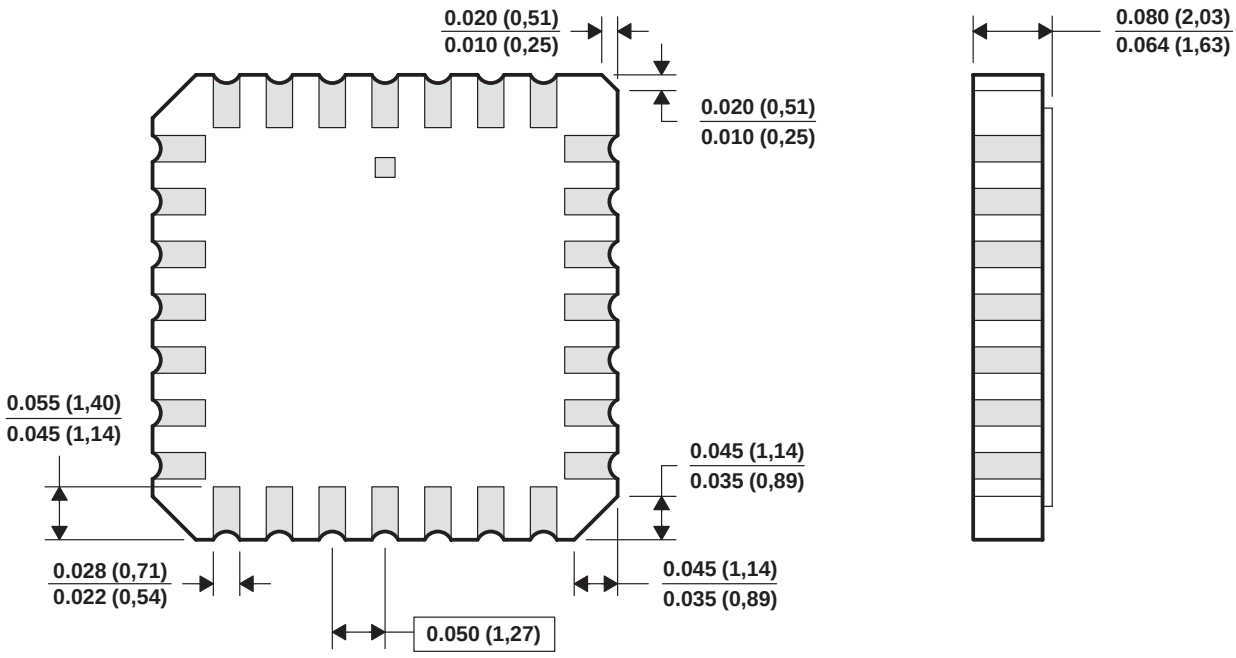
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F16 and JEDEC MO–092AC

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



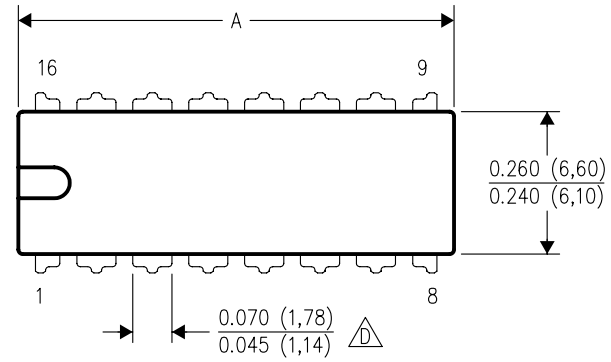
4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

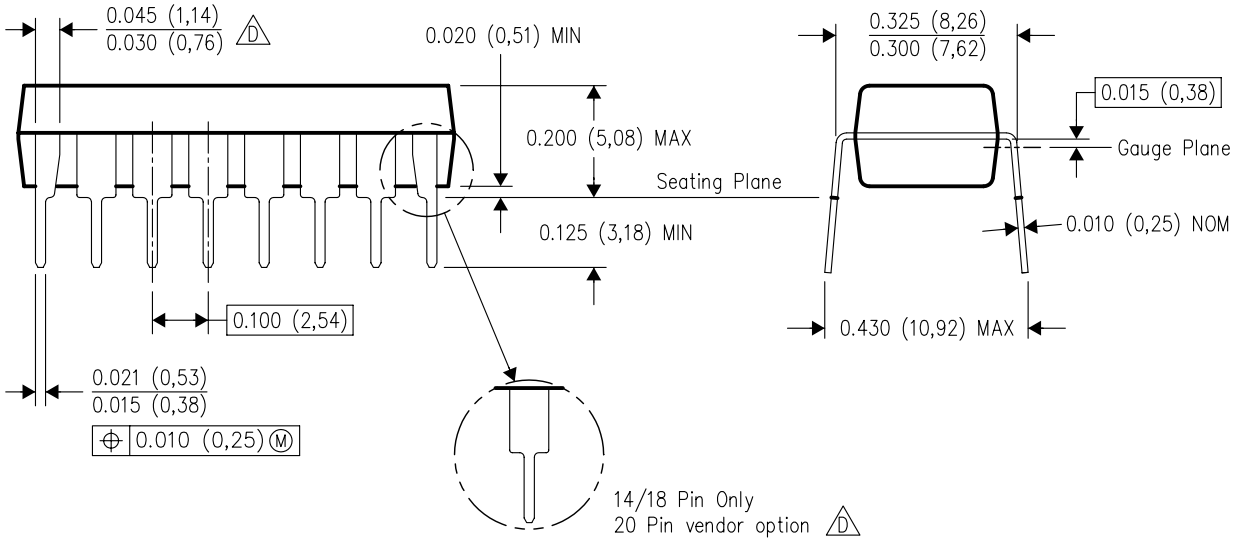
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



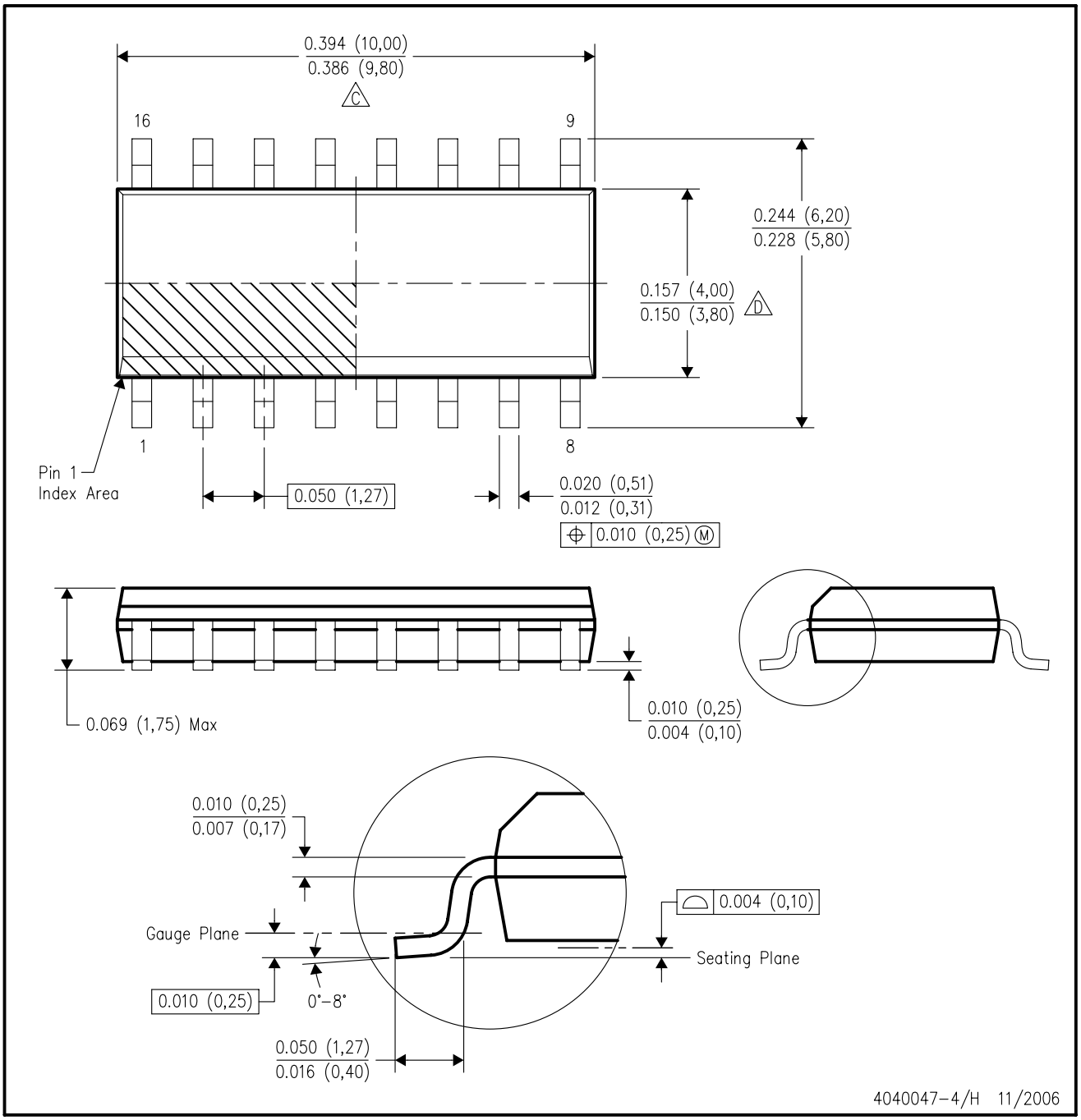
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE

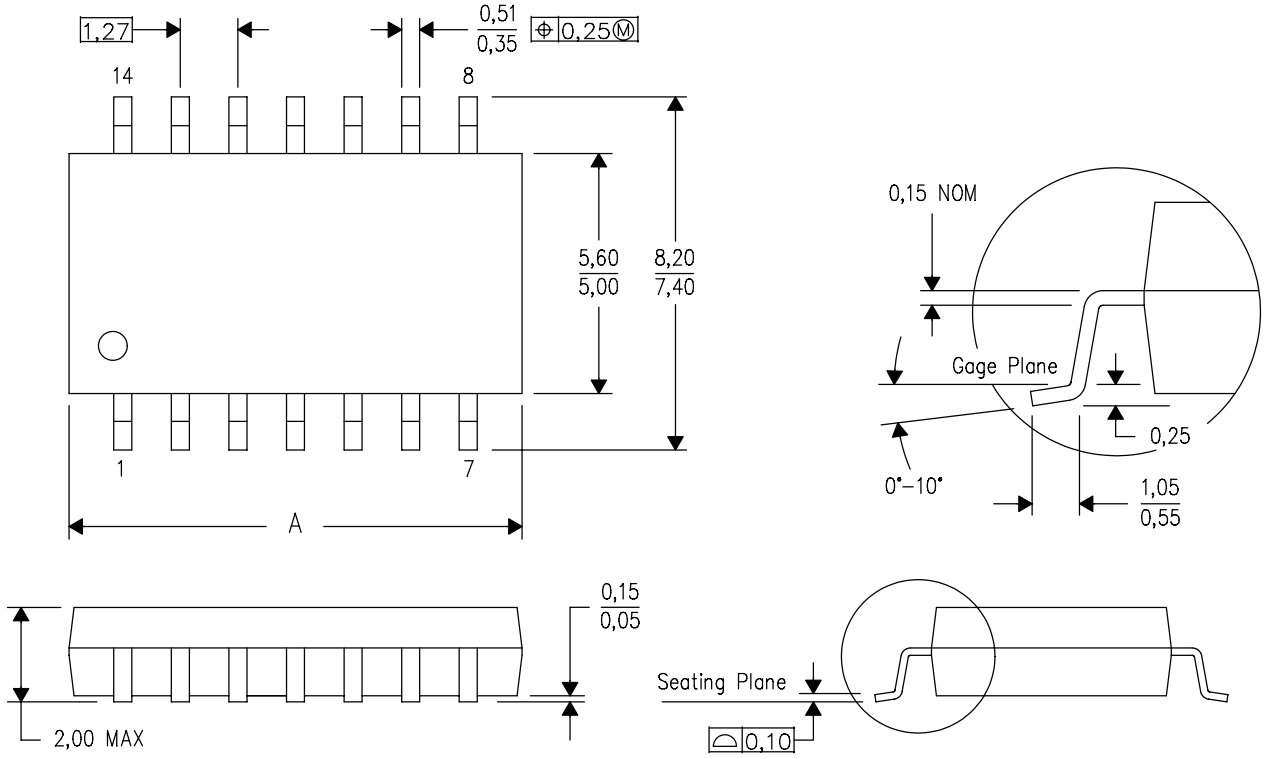


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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