

## 250 mW Linear Power Amplifier and T/R Switch

1.8 - 2.0 GHz

**AM55-0004**  
**V2**

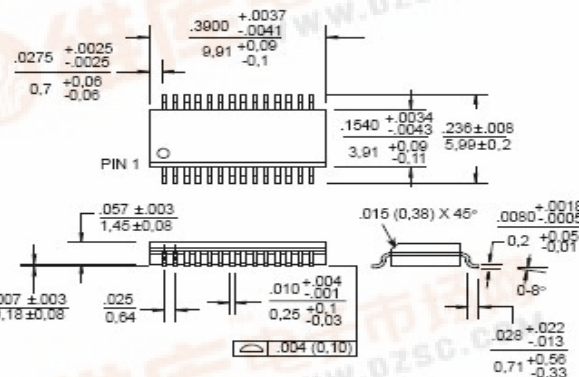
### Features

- Operates Over Full PCN/PCS/PHS Bands
- Operates Over +3 V to +5 V Supply Voltage
- +24 dBm P<sub>1dB</sub> Typical at PA Out
- 35% PAE @ P<sub>1dB</sub> for Linear Operation
- On-Chip T/R Switch, Linear Operation to +30 dBm
- Low Cost SSOP-28 Plastic Package

### Description

M/A-COM's AM55-0004 power amplifier/switch integrates a power amplifier and transmit/receive switch in a low cost SSOP package. The power amplifier delivers +24 dBm of linear power with high efficiency and can be operated at supply voltages as low as 2.7 V. It is ideally suited for QPSK or other linearly modulated systems in the 1.8 to 2.0 GHz frequency band. The power amplifier/switch is fully monolithic and requires only one output capacitor for power match. The T/R switch achieves good insertion loss and isolation without degrading the overall linearity. The AM55-0004 is ideally suited for final stage power amplification in linear TDD systems. The integrated switch is convenient for duplexing. The AM55-0004 can also be used as a driver stage for high power systems. Typical applications include Japanese PHS systems or PCN/PCS transmit chains. M/A-COM's AM55-0004 is fabricated using a mature 0.5-micron gate length GaAs process. The process features full passivation for increased performance and reliability.

### SSOP-28



### Ordering Information

| Part Number  | Package                        |
|--------------|--------------------------------|
| AM55-0004    | SSOP-28-Lead Plastic Packaging |
| AM55-0004TR  | Forward Tape and Reel*         |
| AM55-0004RTR | Reverse Tape and Reel*         |
| AM55-0004SMB | Designer's Kit                 |

\* If specific reel size is required, consult factory for part number assignment.

### Electrical Specifications

**Test conditions: Frequency: 1.9 GHz, VDD1 = VDD2 = 4.8 V ±10%, VG1 adjusted for 30 mA quiescent bias on VDD1, VG2 adjusted for 65 mA quiescent bias on VDD2, TA= +25°C**

| Parameter                                       | Units | Min. | Typ.  | Max. |
|---|-------|------|-------|------|
| <b>Power Amplifier</b>                          |       |      |       |      |
| Linear Gain                                     | dB    | 22   | 24    |      |
| Power Output @ P <sub>1dB</sub> at PA OUT port  | dBm   | 22.5 | 24    |      |
| Current From Positive Supply @ P <sub>1dB</sub> | mA    | 75   | 175   | 275  |
| Input VSWR                                      |       |      | 2.0:1 |      |
| <b>T/R Switch</b>                               |       |      |       |      |
| Insertion Loss                                  | dB    |      | 0.6   | 1.0  |
| Input Match                                     |       |      | 1.5:1 |      |
| Isolation                                       | dB    | 15   | 20    |      |

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### Pin Configuration

| Pin No. | Pin Name         | Description  |
|---------|------------------|--|
| 1       | GND              | RF and DC Ground   |
| 2       | VSW              | Complimentary T/R Switch Control, -4 V Tx model/0 V Rx mode  |
| 3       | GND              | RF and DC Ground   |
| 4       | Tx IN            | Transmit side of T/R switch  |
| 5       | GND              | RD and DC Ground   |
| 6       | GND              | RF and DC Ground   |
| 7       | ANT IN/OUT       | Common port of T/R switch which is connected to the antenna  |
| 8       | GND              | RF and DC Ground   |
| 9       | Rx OUT           | Receive side of T/R switch   |
| 10      | GND              | RF and DC Ground   |
| 11      | GND              | RF and DC Ground   |
| 12      | V <sub>DD1</sub> | Positive bias for the first stage of PA, +2.7 to +6.0 volts  |
| 13      | SAVE Tx          | Sleep mode control of first stage of PA ONLY<br>0 V—first PA stage on<br>-4 V—first PA stage off   |
| 14      | GND              | RF and DC Ground   |
| 15      | GND              | RF and DC Ground   |
| 16      | PA IN            | RF input of the Power Amplifier  |
| 17      | GND              | RF and DC Ground   |
| 18      | V <sub>G1</sub>  | Negative bias control for the first PA stage, voltage divider is on the MMIC, adjusted to set V <sub>DD1</sub> quiescent bias current, which is typically 30 mA. Input impedance : 10 k $\Omega$ |
| 19      | GND              | RF and DC Ground   |
| 20      | V <sub>G2</sub>  | Negative bias control for the second PA stage, adjusted to set V <sub>DD2</sub> quiescent bias current, which is typically 65 mA. Input impedance : > 1 M $\Omega$                               |
| 21      | GND              | Second Stage RF and DC Ground  |
| 22      | GND              | Second Stage RF and DC Ground  |
| 23      | GND              | Second Stage RF and DC Ground  |
| 24      | GND              | Second Stage RF and DC Ground  |
| 25      | PA OUT           | RF output of the Power Amplifier   |
| 26      | V <sub>DD2</sub> | Positive bias for the second stage of the PA, +2.7 to +6.0 volts   |
| 27      | VSW              | T/R Switch Control, 0 V Tx model/ -4 V Rx mode   |
| 28      | GND              | RF and DC Ground   |

### Absolute Maximum Ratings <sup>1</sup>

| Parameter                       | Absolute Maximum   |
|---------------------------------|--|
| Max. Input Power <sup>2</sup>   | +10 VDC  |
| Operating Voltages <sup>2</sup> | V <sub>DD</sub> = 7V<br>V <sub>GG</sub> = -5 V<br>V <sub>DD</sub> - V <sub>GG</sub> = 8V |
| Operating Temperature           | -40°C to +85°C   |
| Storage Temperature             | -65°C to +150°C  |

1. Exceeding any one or combination of these limits may cause permanent damage to this device.

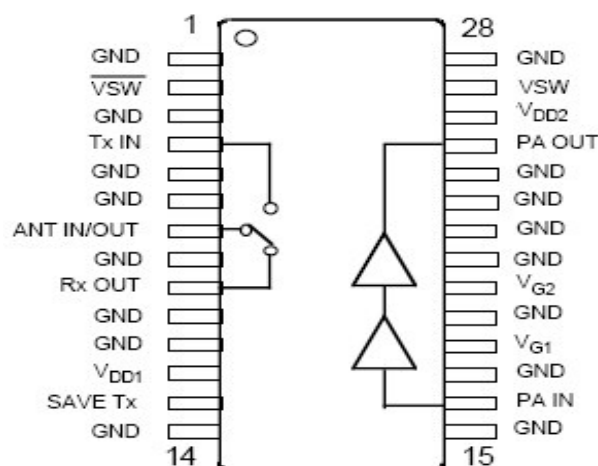
2. Ambient temperature (T<sub>A</sub>) = +25°C.

### Truth Table

| Operating Mode | VSW        | VSW        | SAVE Tx    |
|----------------|------------|------------|------------|
| PA Tx          | X          | X          | 0 V        |
| PA Sleep       | X          | X          | -4.0 Volts |
| T/R Switch TX  | 0 Volts    | -4.0 Volts | X          |
| T/R Switch Rx  | -4.0 Volts | 0 Volts    | X          |

X = Don't Care

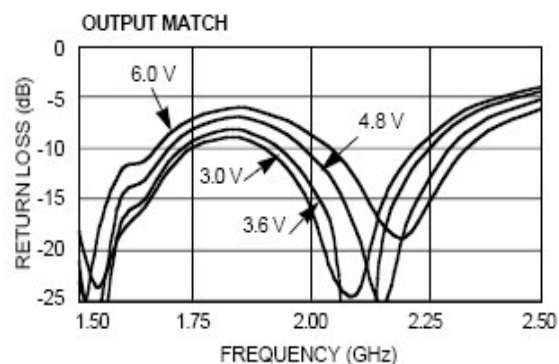
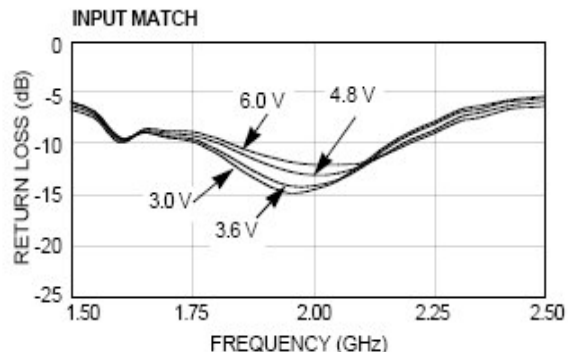
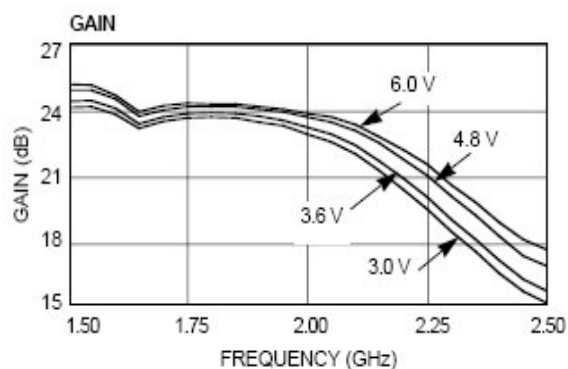
### Functional Diagram and Pin Configuration



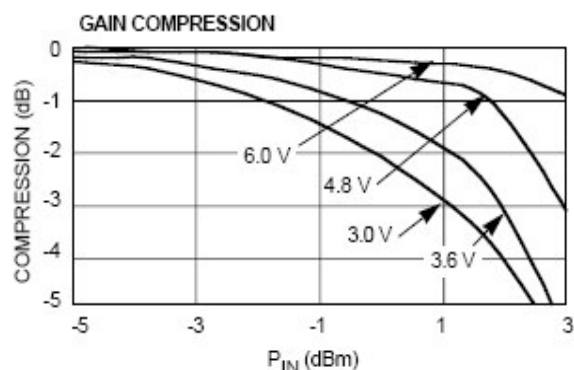
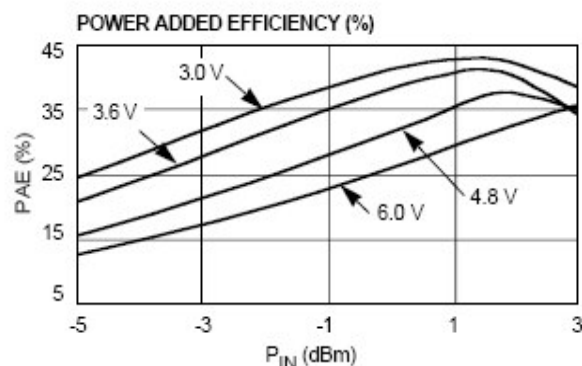
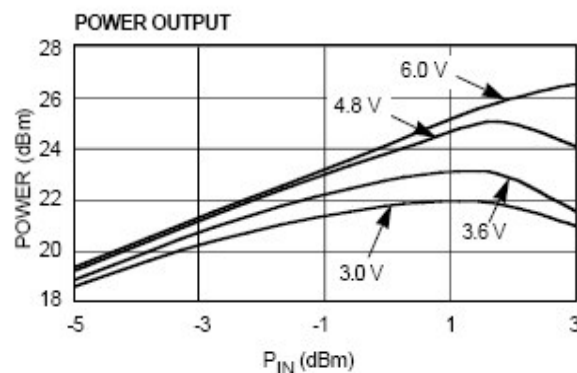
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**Power Amplifier Small Signal**  
**Performance<sup>1</sup>**



**Power Amplifier CW Performance**  
**at 1.9 GHz<sup>1</sup>**

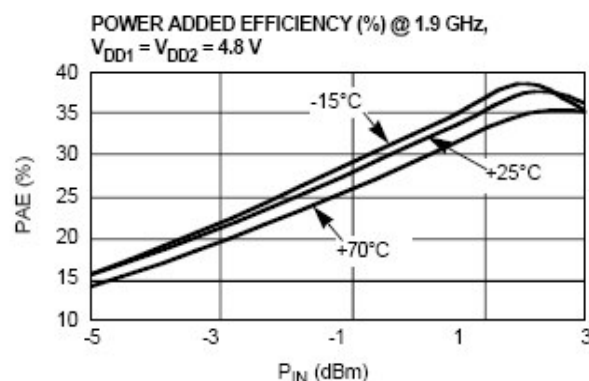
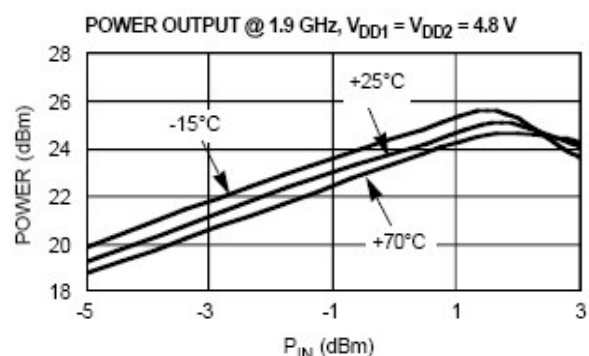
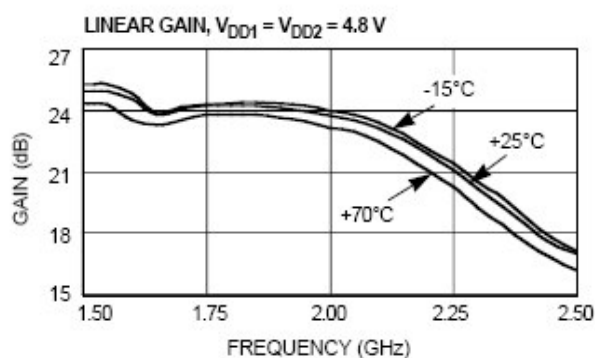


1. All data measured at  $T_A = +25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  adjusted for first stage quiescent current of 30 mA and second stage current of 65 mA, respectively.

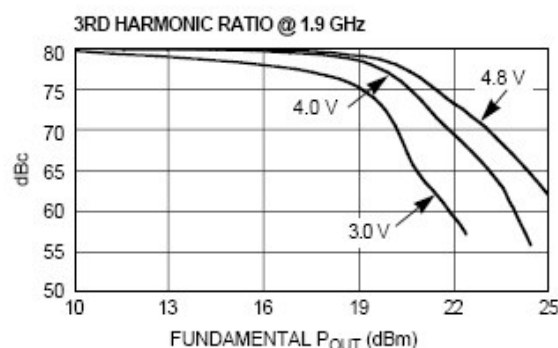
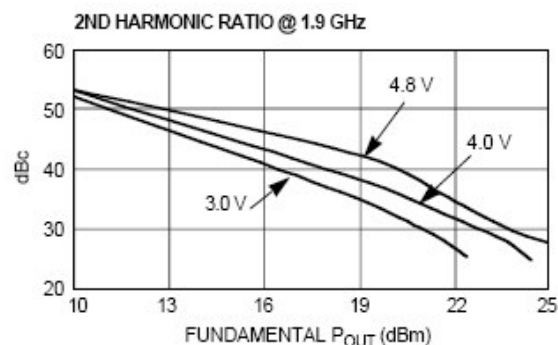
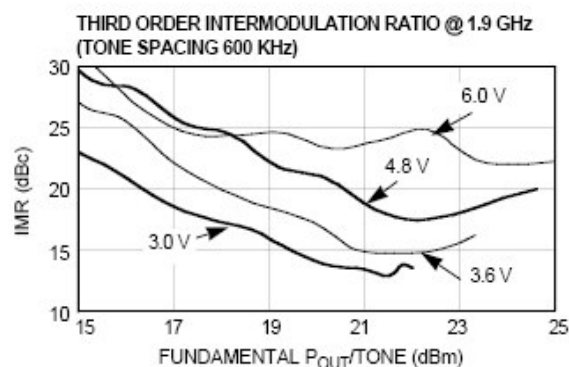
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**Power Amplifier Temperature Performance<sup>1</sup>**



**Power Amplifier Spurious Response at Various Supply Voltages<sup>1</sup>**

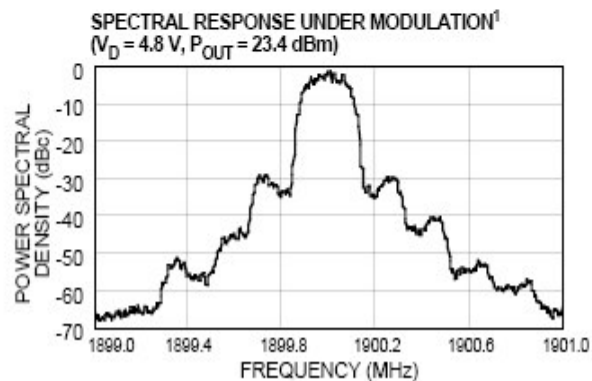
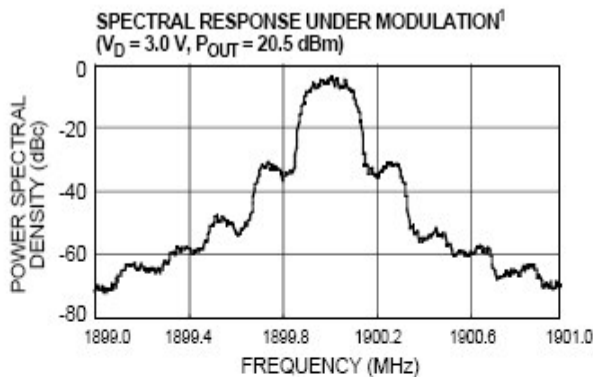


1. All data measured at  $T_A = +25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  adjusted for first stage quiescent current of 30 mA and second stage current of 65 mA, respectively.

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**Power Amplifier Spectral Response Under Modulation Drive ( $\neq$ 4 DQPSK,  $a = 0.5$ , 384 kB/sec, 9-bit PN code)**



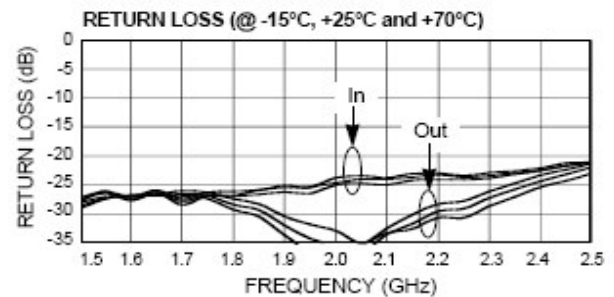
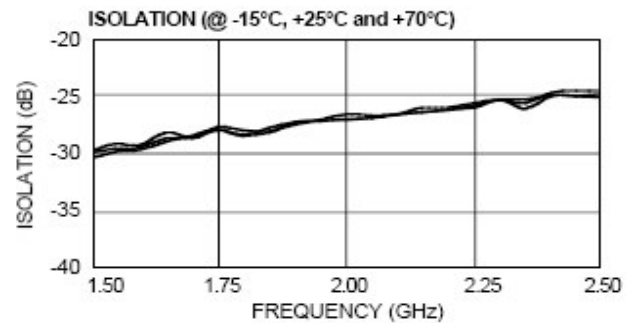
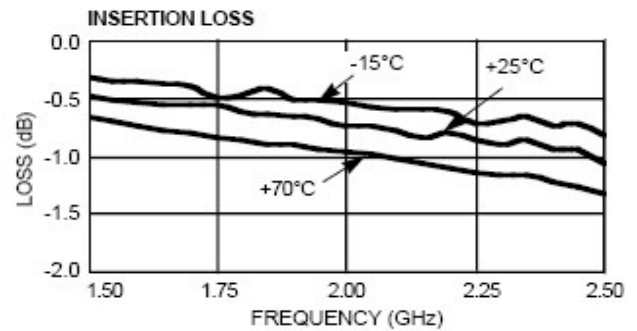
**Output Power Under Modulation<sup>2</sup>**

| $V_D$ (volts) | $P_{OUT}$ (dBm) |
|---------------|-----------------|
| 3             | 20.5            |
| 3.6           | 21.4            |
| 4             | 22.2            |
| 4.8           | 23.4            |
| 6             | 23.7            |

1. Spectral output is tested under the following conditions:  
Modulation scheme is  $\neq$ 4 DQPSK with a bit transfer rate of 384 kB/sec and a root Nyquist filter with  $a = 0.5$  per RCR STD-28.  
The spectrum analyzer settings are as follows:  
Resolution bandwidth: 10 kHz  
Video bandwidth: 100 kHz  
Sweep time: 5 seconds

2. This chart documents the modulated output power delivered for a fixed adjacent channel interference (ACI) rejection of 55

**Transmit/Receive Switch Performance**

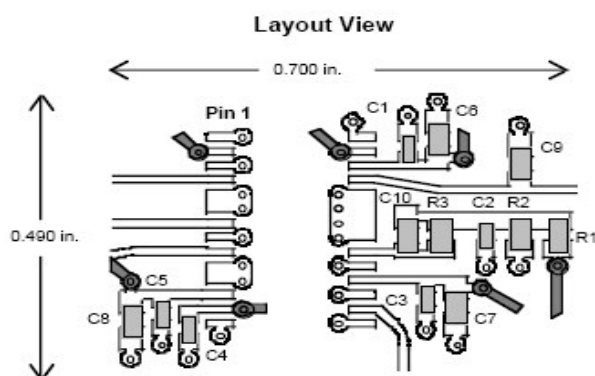


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### Recommended PCB Configuration



### Cross-Section View



The PCB dielectric between RF traces and RF ground layers should be chosen to reduce RF discontinuities between 50- $\Omega$  lines and package pins. M/A-COM recommends an FR-4 dielectric thickness of 0.008 in. (0.2 mm), yielding a 50- $\Omega$  line width of 0.015 in. (0.38 mm). The recommended metalization thickness is 1 oz. copper. Shaded traces are vias to DC routing layer and traces on DC routing layer.

### External Circuitry Parts List

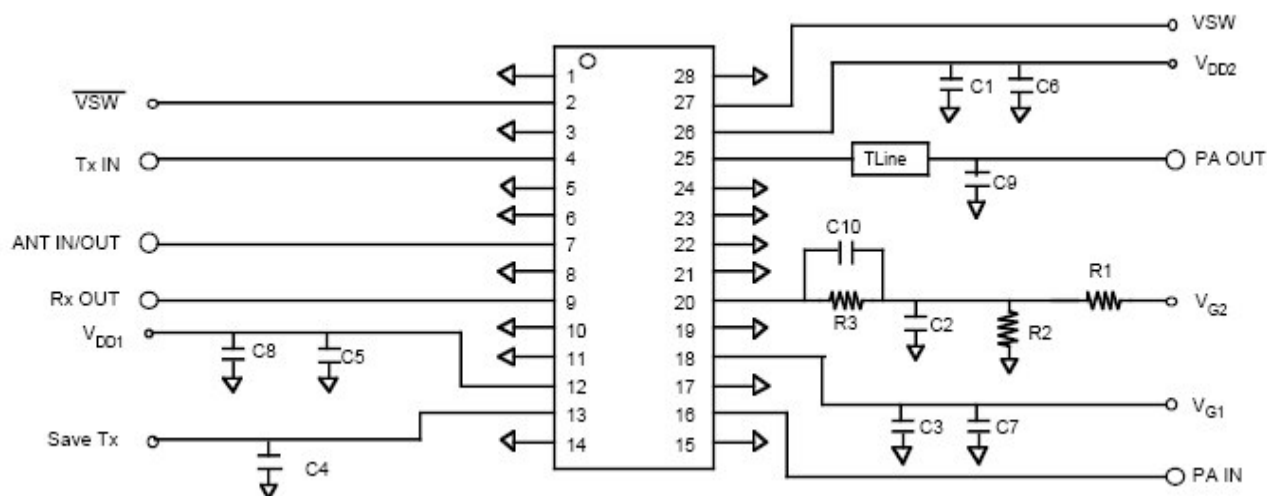
| Label   | Value          | Purpose                     |
|---------|----------------|-----------------------------|
| C1 - C5 | 1000 pF        | Low Frequency bypass        |
| C6 - C8 | 68 pF          | RF bypass                   |
| C9      | 1.5 pF         | Output power tuning         |
| C10     | 15 pF          | Reduces low frequency gain  |
| R1      | 2.7 k $\Omega$ | Voltage divider to $V_{G2}$ |
| R2      | 1.5 k $\Omega$ | Voltage divider to $V_{G2}$ |
| R3      | 150 $\Omega$   | Reduces low frequency gain  |
| Tline   | 0.250 in. long | Power match                 |

All off-chip components are low-cost surface mount components obtainable from multiple sources. (0.020 in. x 0.040 in. or 0.030 in. x 0.050 in.)

### Biasing Procedure

The AM55-0004 requires that  $V_{GG}$  bias be applied prior to *any*  $V_{DD}$  bias. Permanent damage may occur if this procedure is not followed. All FETs in the PA will draw excessive current and damage internal circuitry.

### External Circuitry



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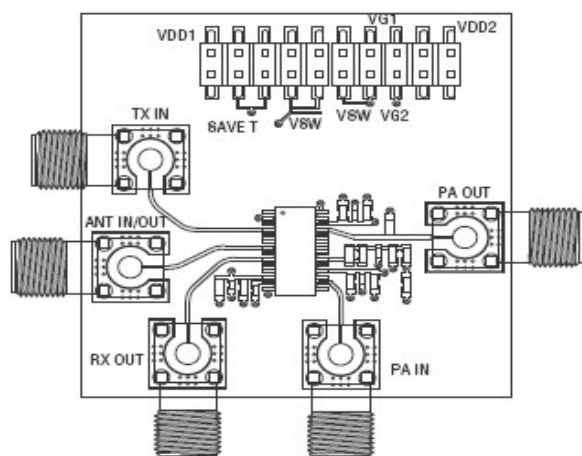
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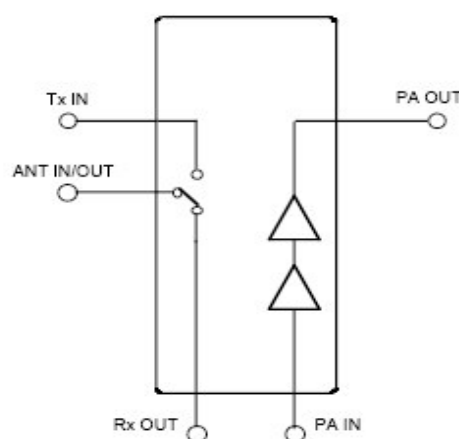
### Designer's Kit (AM55-0004SMB)

The AM55-0004SMB Designer's Kit allows for immediate evaluation of M/A-COM's AM55-0004 integrated Power Amplifier and T/R Switch. The evaluation board consists of an AM55-0004, recommended external surface mount circuitry, RF connectors and a DC multipin connector, all mounted to a multi-layer FR-4 PCB. Other items included in the Designer's Kit: a floppy disk (with typical performance data and a .DXF file of the recommended PCB layout) and any additional Application Notes. The AM55-0004SMB PA/Switch evaluation PCB and block diagram are illustrated below with all functional ports labeled.

### P/A Switch Sample Board



### Functional Block Diagram



### DC Connector Pinout

| PCB DC Connector | Function           | Device Pin Number |
|------------------|--------------------|-------------------|
| 1                | N/C                | N/C               |
| 2                | VDD1 (+ 4.8 V)     | 12                |
| 3                | SAVE Tx (0 V/-4 V) | 13                |
| 4                | GND                | N/C               |
| 5                | SAVE Tx (0 V/-4 V) | 13                |
| 6                | VG1                | 18                |
| 7                | VSW                | 2                 |
| 8                | GND                | N/C               |
| 9                | VSW                | 2                 |
| 10               | VG1                | 18                |

| PCB DC Connector | Function       | Device Pin Number |
|------------------|----------------|-------------------|
| 11               | VSW            | 27                |
| 12               | VG1            | 18                |
| 13               | VSW            | 27                |
| 14               | GND            | N/C               |
| 15               | VG2            | 20                |
| 16               | VG1            | 18                |
| 17               | N/C            | N/C               |
| 18               | VG2            | 20                |
| 19               | N/C            | N/C               |
| 20               | VDD2 (+ 4.8 V) | 26                |

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### AM55-0004SMB Biasing Procedure

In order to prevent transients which may damage the MMIC, please adhere to the following procedure.

- Turn on all power supplies and set all voltages to 0 volts BEFORE connecting the power supplies to the DC connector.
  - Apply -4.0 volt supply or GND to DC connector pin 9 (VSW, see truth table for desired mode).
  - Apply -4.0 volt supply or GND to DC connector pin 13 (VSW, see truth table for desired mode).
  - Apply a -4.0 volt supply to the DC connector pin 16 (VG1).
  - Apply a -4.0 volt supply to the DC connector pin 18 (VG2).
  - Apply a +4.8 volt supply to the DC connector pin 2 (VDD1).
  - Apply a +4.8 volt supply to the DC connector pin 20 (VDD2).
  - Apply GND to DC connector pin 5 (Save Tx).
  - Adjust VG1 supply for desired VDD1 quiescent current (typically 30 mA).
  - Adjust VG2 supply for desired VDD2 quiescent current (typically 65 mA).
  - Change voltage on DC connector pin 5 as required (Save Tx, see truth table for desired mode).
  - Apply RF power and test.
  - To power off, reverse above procedure
1. Set VG1 & VG2 to -4 V.
  2. Set VDD1 & VDD2 to 0 V.
  3. Set control voltage supplies to 0 V.
  4. Disconnect bias lines from DC connector.
  5. Turn off power supplies.

### Evaluation PCB and RF Connector Losses

| Port Reference | Estimated Loss (dB) |
|----------------|---------------------|
| PA IN          | 0.15                |
| PA OUT         | 0.20                |
| Tx IN          | 0.20                |
| ANT IN/OUT     | 0.20                |
| Rx OUT         | 0.20                |

The DC connector on the Designer's Kit PCB allows selection of all the device's operating modes.

It is accomplished by one or more of the following methods:

1. A mating female multi-pin connector (Newark Electronics Stock # 46F-4658, not included)
2. Wires soldered to the necessary pins (not included)
3. Clip leads (not included)
4. A combination of clip leads or wires and jumpers (jumpers included as required)