Am6071
Companding D-to-A Converter for Control Systems

Distinctive Characteristics

- Tested to A-law tracking specification
- Absolute accuracy specified – includes all errors over temperature range
- Settling time 300ns typical
- Ideal for multiplexed PCM, audio, and 8-bit μ-P systems
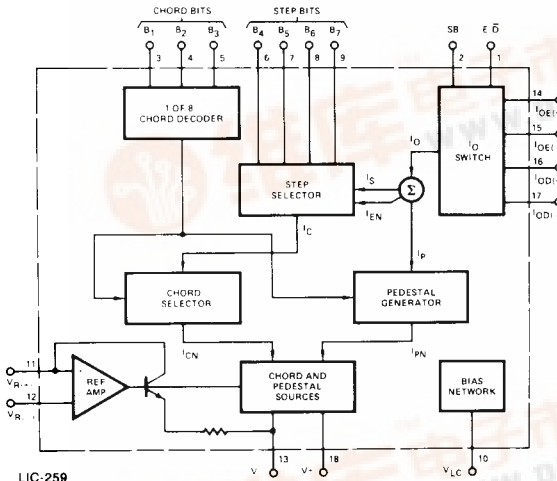
- Output dynamic range of 62 dB
- Microprocessor controlled operations
- Multiplying operation
- Negligible output noise
- Monotonicity guaranteed over entire dynamic range
- Wide output voltage compliance
- Low power consumption

GENERAL DESCRIPTION

The Am6071 is a monolithic 8-bit, companding digital-to-analog (D/A) converter with true current outputs and large output voltage compliance for fast driving a variety of loads. The transfer function of the Am6071 consists of 13 linear segments or chords. A particular chord is identified with the sign bit input, (SB) and three chord select input bits. Each chord contains 16 uniformly spaced linear steps which are determined by four step select input bits. The resulting dynamic range achieved with this format is 62 dB. Accuracy
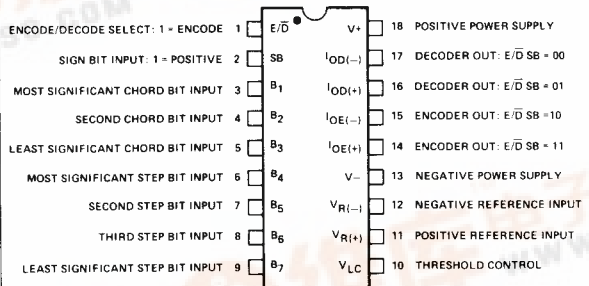
and monotonicity are assured by the internal circuit design and are guaranteed over the full temperature range. The Am6071 is tested to the A-law tracking specification. Applications for the Am6071 include digital audio recording, servo motor controls, electro-mechanical positioning, voice synthesis, secure communications, microprocessor controlled sound and voice systems, log sweep generators, and various data acquisition systems.

FUNCTIONAL BLOCK DIAGRAM


LIC-259

CONNECTION DIAGRAM
Am6072

Pin	Name	Pin	Name
ENCODE/DECODE SELECT: 1 = ENCODE 1	E/D̄	18	V+ POSITIVE POWER SUPPLY
SIGN BIT INPUT: 1 = POSITIVE 2	SB	17	$I_{OD(-)}$ DECODER OUT: E/D̄ SB = 00
MOST SIGNIFICANT CHORD BIT INPUT 3	B₁	16	$I_{OD(+)}$ DECODER OUT: E/D̄ SB = 01
SECOND CHORD BIT INPUT 4	B₂	15	$I_{OE(-)}$ ENCODER OUT: E/D̄ SB =10
LEAST SIGNIFICANT CHORD BIT INPUT 5	B₃	14	$I_{OE(+)}$ ENCODER OUT: E/D̄ SB = 11
MOST SIGNIFICANT STEP BIT INPUT 6	B₄	13	V– NEGATIVE POWER SUPPLY
SECOND STEP BIT INPUT 7	B₅	12	$V_{R(-)}$ NEGATIVE REFERENCE INPUT
THIRD STEP BIT INPUT 8	B₆	11	$V_{R(+)}$ POSITIVE REFERENCE INPUT
LEAST SIGNIFICANT STEP BIT INPUT 9	B₇	10	V_{LC} THRESHOLD CONTROL

Top View
Pin 1 is marked for orientation.   LIC-260

ORDERING INFORMATION

Part Number	Temperature	Accuracy
Am6071ADM	−55°C to +125°C	±1/2 step
Am6071DM	−55°C to +125°C	±1 step
Am6071ADC	0°C to +70°C	±1/2 step
Am6071DC	0°C to +70°C	±1 step

SIMPLIFIED CONVERSION TRANSFER FUNCTIONS

Decoder Characteristic

Encoder Characteristic
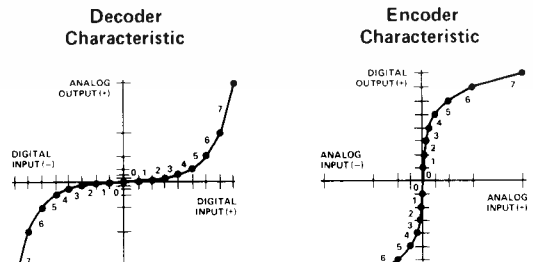
Am6071

MAXIMUM RATINGS above which useful life may be impaired

V+ Supply to V− Supply	36V	Operating Temperature	
V_{LC} Swing	V− plus 8V to V+	MIL Grade	−55°C to +125°C
Output Voltage Swing	V− plus 8V to V− plus 36V	COM'L Grade	0°C to +70°C
Reference Inputs	V− to V+	Storage Temperature	−65°C to +150°C
Reference Input Differential Voltage	±18V	Power Dissipation $T_A \leqslant 100°C$	500mW
Reference Input Current	1.25mA	For $T_A > 100°C$ derate at	10mW/°C
Logic Inputs	V− plus 8V to V− plus 36V	Lead Soldering Temperature	300°C (60 sec)

GUARANTEED FUNCTIONAL SPECIFICATIONS

Resolution	±128 Steps
Monotonicity	For both groups of 128 steps and over full operating temperature range
Dynamic Range	62dB, $(20 \log (I_{7, 15}/I_{0, 1}))$

ELECTRICAL CHARACTERISTICS

These specifications apply for V+ = +15V, V− = −15V, I_{REF} = 512µA, 0°C ≤ T_A ≤ +70°C, for the commercial grade, −55°C ≤ T_A ≤ +125C, for the military grade, and for all 4 outputs unless otherwise specified.

Parameter	Description		Test Conditions	Am6071ADM / Am6071ADC Min.	Typ.	Max.	Am6071DM / Am6071DC Min.	Typ.	Max.	Units
t_s	Settling Time		To within ±1/2 step at T_A = 25°C output switched from I_{ZS} to I_{FS}		300	500		300	500	ns
	Chord Endpoint Accuracy		Guaranteed by output current error specified below.		±1/2			±1		Step
	Step Nonlinearity				±1/2			±1		Step
$I_{FS(D)}$	Full Scale Current Deviation				±1/2			±1		
$I_{FS(E)}$	From Ideal				±1/2			±1		
ΔI_O	Output Current Error		V_{REF} = 10.000V, R_{REF+} = 19.53k, R_{REF-} = 20kΩ, −5.0V ≤ V_{OUT} ≤ +18V, Error referred to nominal values in Table 1.		±1/2			±1		Step
$I_{O(+)} - I_{O(-)}$	Full Scale Symmetry Error		V_{REF} = 10.000V, R_{REF-} = 19.53k, R_{REF} = 20kΩ, −5.0V ≤ V_{OUT} ≤ +18V, Error referred to nominal values in Table 1	1/40	1/8		1/20	1/4		Step
				1/40	1/8		1/20	1/4		Step
I_{EN}	Encode Current		Additional output Encode/Decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
I_{ZS}	Zero Scale Current		Measured at selected output with 000 0000 input		1/40	1/4		1/20	1/2	Step
ΔI_{FS}	Full Scale Drift		Operating temperature range		±1/20	±1/4		±1/10	±1/2	Step
V_{OC}	Output Voltage Compliance		Full scale current change ≤1/2 step	−5.0		+18	−5.0		+18	Volts
I_{DIS}	Disable Current		Output leakage Output disabled by E/D̄ and SB		5.0	50		5.0	50	nA
I_{FSR}	Output Current Range			0	2.0	4.2	0	2.0	4.2	mA
V_{IL}	Logic Input Levels	Logic "0"	V_{LC} = 0V			0.8			0.8	Volts
V_{IH}		Logic "1"		2.0			2.0			
I_{IN}	Logic Input Current		V_{IN} = −5.0V to +18V			40			40	µA
V_{IS}	Logic Input Swing		V− = −15V	−5.0		+18	−5.0		+18	Volts
$I_{B \ REF-}$	Reference Bias Current				−1.0	−4.0		−1.0	−4.0	µA
di/dt	Reference Input Slew Rate			0.12	0.25		0.12	0.25		mA/µs
$PSSI_{FS+}$	Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)		V+ = 4.5 to 18V, V− = −15V	±1/20	±1/2		±1/20	±1/2		Step
$PSSI_{FS-}$			V− = −10.8 to −18V, V+ = 15V	±1/10	±1/2		±1/10	±1/2		Step
I+	Power Supply Current		V+ = +5.0 to +15V, V− = −15V		2.7	4.0		2.7	4.0	mA
I−			I_{FS} = 2.0mA		−6.7	−8.8		−6.7	−8.8	
P	Power Dissipation		V− = −15V, V_{OUT} = 0 V+ = 5.0V		114	152		114	152	mW

ELECTRICAL CHARACTERISTICS (Cont.)

TABLE I
NOMINAL DECODER OUTPUT CURRENT LEVELS IN μA

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	.500	16.500	33.000	66.000	132.00	264.00	528.00	1056.00
1	1.500	17.500	35.000	70.000	140.00	280.00	560.00	1120.00
2	2.500	18.500	37.000	74.000	148.00	296.00	592.00	1184.00
3	3.500	19.500	39.000	78.000	156.00	312.00	624.00	1248.00
4	4.500	20.500	41.000	82.000	164.00	328.00	656.00	1312.00
5	5.500	21.500	43.000	86.000	172.00	344.00	688.00	1376.00
6	6.500	22.500	45.000	90.000	180.00	360.00	720.00	1440.00
7	7.500	23.500	47.000	94.000	188.00	376.00	752.00	1504.00
8	8.500	24.500	49.000	98.000	196.00	392.00	784.00	1568.00
9	9.500	25.500	51.000	102.000	204.00	408.00	816.00	1632.00
10	10.500	26.500	53.000	106.000	212.00	424.00	848.00	1696.00
11	11.500	27.500	55.000	110.000	220.00	440.00	880.00	1760.00
12	12.500	28.500	57.000	114.000	228.00	456.00	912.00	1824.00
13	13.500	29.500	59.000	118.000	236.00	472.00	944.00	1888.00
14	14.500	30.500	61.000	122.000	244.00	488.00	976.00	1952.00
15	15.500	31.500	63.000	126.000	252.00	504.00	1008.00	2016.00
STEP SIZE	1	1	2	4	8	16	32	64

TABLE 2
IDEAL DECODER OUTPUT VALUES EXPRESSED IN dB DOWN FROM OVERLOAD LEVEL (+ 3dBmo)

STEP	CHORD							
	0	1	2	3	4	5	6	7
0	72.11	41.74	35.72	29.70	23.68	17.66	11.64	5.62
1	62.57	41.23	35.21	29.19	23.17	17.15	11.13	5.11
2	58.13	40.75	34.73	28.71	22.68	16.66	10.64	4.62
3	55.21	40.29	34.27	28.25	22.23	16.21	10.19	4.17
4	53.03	39.85	33.83	27.81	21.79	15.77	9.75	3.73
5	51.28	39.44	33.42	27.40	21.38	15.36	9.34	3.32
6	49.83	39.05	33.03	27.00	20.98	14.96	8.94	2.92
7	48.59	38.67	32.65	26.63	20.61	14.59	8.57	2.54
8	47.50	38.31	32.29	26.27	20.24	14.22	8.20	2.18
9	46.54	37.96	31.94	25.92	19.90	13.88	7.86	1.84
10	45.67	37.62	31.60	25.58	19.56	13.54	7.52	1.50
11	44.88	37.30	31.28	25.26	19.24	13.22	7.20	1.18
12	44.15	36.99	30.97	24.95	18.93	12.91	6.89	0.87
13	43.48	36.69	30.67	24.65	18.63	12.61	6.59	0.57
14	42.86	36.40	30.38	24.38	18.34	12.32	6.30	0.28
15	42.28	36.12	30.10	24.08	18.06	12.04	6.02	0.00

3

THEORY OF OPERATION

Functional Description

The Am6071 is an 8-bit, nonlinear, digital-to-analog converter with high impedance current outputs. The output current value is proportional to the product of the digital inputs and the input reference current. The full scale output current, I_{FS}, is specified by the input binary code 111 1111, and is a linear function of the reference current, I_{REF}. There are two operating modes, encode and decode, which are controlled by the Encode/Decode, ($E/\overline{D}$), input signal. A logic 1 applied to the $E/\overline{D}$ input places the Am6073 in the encode mode and current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output, depending on the state of the Sign Bit (SB) input. A logic 0 at the $E/\overline{D}$ input places the Am6073 in the decode mode.

The transfer characteristic is a piece-wise linear approximation to the CCITT A-87.6 logarithmic law which can be written as follows:

$$Y = 0.18 \, (1 + \ln (A\,|X|\,)) \, sgn\,(X), \quad 1/A \leqslant |X| \leqslant 1$$
$$Y = 0.18 \, (A\,|X|\,) \, sgn\,(X), \quad\quad\quad 0 \leqslant |X| \leqslant 1/A$$

where: X = analog signal level normalized to unity
(encoder input or decoder output)
Y = digital signal level normalized to unity
(encoder output or decoder input)
$A = 87.6$

The current flows from the external circuit into one of four possible analog outputs determined by the SB and $E/\overline{D}$ inputs. The output current transfer function can be represented by a total of 16 segments or chords addressable through the SB input and three chord select bits. The two chords closest to the origin of the transfer function, chord 0 and chord 1, are made colinear and contiguous. The beginning of chord 0, specified by the input binary code 000 0000, is offset by $+0.5\mu A$. Each chord can be further divided into 16 steps, all of the same size. The step size changes from one chord to another, with the smallest step of $1.0\mu A$ found in the first two chords near zero output current, and the largest step of $64\mu A$ found in the last chord near full scale output current. This nonlinear feature provides exceptional accuracy for small signal levels. The accuracy for signal amplitudes corresponding to chords 0 and 1 is very close to that of an 11-bit linear, binary D/A converter. The ratio (in dB) between the chord endpoint current, (Step 15), and the current which corresponds to the preceding step, (Step 14), is maintained at about 0.3dB over the entire dynamic range, with the exception of chord 0. The difference between the ratios of full scale current to chord endpoint currents of adjacent chords is similarly maintained at 6dB over the entire dynamic range. Resulting signal-to-quantizing distortions due to non-uniform quantizing levels maintain an acceptably low value over a 40dB range of input speech signals. Note that the 62dB output dynamic range for the Am6071 is very close to the dynamic range of a sign plus 11-bit linear, binary D/A converter.

In order to achieve a smoother transition between adjacent chords, the step size between these chord end points is equal to 1.5 times the step size of the lower chord. Note that this does not apply to chord 0 and chord 1 where adjacent end points differ by only one step, because these two chords are colinear and have the same step sizes. Monotonic operation is guaranteed by the internal device design over the entire output dynamic range by specifying and maintaining the chord end points and step size deviations within the allowable limits.

Operating Modes

The basic converter function is conversion of digital input data into a corresponding analog current signal, i.e., the basic function is digital-to-analog decoding. The basic decoder connection for a sign plus 7-bit input configuration is shown in Figure 1. The corresponding dynamic range is 62dB, and input-output characteristics conform to the standard decoder transfer function with output current values specified in Table 1. The $E/\overline{D}$ input enables switching between the encode, $I_{OE(+)}$ or $I_{OE(-)}$, and the decode, $I_{OD(+)}$ or $I_{OD(-)}$, outputs. A typical encode/decode test circuit is shown in Figure 2. This circuit is used for output current measurements. When the $E/\overline{D}$ input is high, (a logic 1), the converter will assume the encode mode operating mode and the output current will flow into one of the I_{OE} outputs (as determined by the SB input). When operating in the encode mode as shown
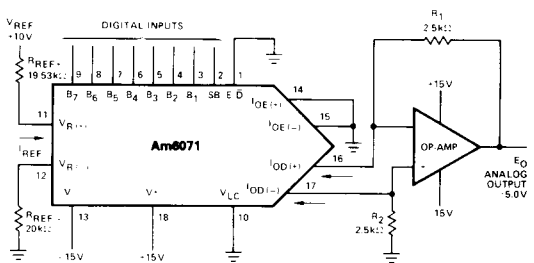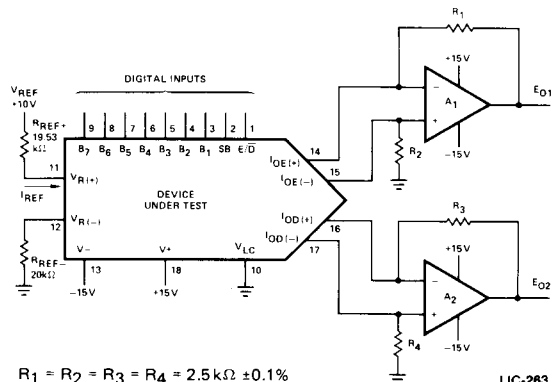

$I_{REF} = V_{REF}/R_{REF}$
IDEAL VALUES: $I_{REF} = 512\mu A$, $I_{FS} = 2016\mu A$

LIC-262

	E/D̄	SB	B₁	B₂	B₃	B₄	B₅	B₆	B₇	E_O
POSITIVE FULL SCALE	0	1	1	1	1	1	1	1	1	5.040V
(+) ZERO SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.004V
(+) ZERO SCALE	0	1	0	0	0	0	0	0	0	0.0012V
(-) ZERO SCALE	0	0	0	0	0	0	0	0	0	-0.0012V
(-) ZERO SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.004V
NEGATIVE FULL SCALE	0	0	1	1	1	1	1	1	1	-5.040V

Figure 1. Detailed Decoder Connections

$R_1 = R_2 = R_3 = R_4 = 2.5k\Omega \pm 0.1\%$

LIC-263

LINE SELECTION TABLE

TEST GROUP	E/D̄	SB	OUTPUT MEASUREMENT	
1	1	1	I_OE (+)	(E_O1/R_1)
2	1	0	I_OE (-)	(E_O1/R_2)
3	0	1	I_OD (+)	(E_O2/R_3)
4	0	0	I_OD (-)	(E_O2/R_4)

in Figure 3, an offset current equal to a half step in each chord is required to obtain the correct encoder transfer characteristic. Since the size of this step varies from one chord to another, it cannot easily be added externally. As indicated in the block diagram this required half step of encode current, I_{EN}, is automatically added to the I_{OE} output through the internal chip design. This additional current will, for example, make the ideal full scale current in the encode mode larger than the same current in the decode mode by $32\mu A$. Similarly, the current levels in the first chord near the origin will be offset by $0.5\mu A$, which will bring the ideal encode current value for step 0 on chord 0 to $1.0\mu A$ with respect to the corresponding decode current value of $0.5\mu A$. This additional encode half step of current can be used for extension of the output dynamic range from 62dB to 66dB, when the converter is performing only the decode function. The corresponding decoder connection utilizes the $E/\overline{D}$ input as a ninth digital input and has the outputs $I_{OD(+)}$ and $I_{OE(+)}$ and the outputs $I_{OD(-)}$ and $I_{OE(-)}$ tied together, respectively.

When encoding or compression of an analog signal is required, the Am6071 can be used together with a Successive Approximation Register (SAR), comparator, and additional SSI logic elements to perform the A/D data conversion, as shown in Figure 3. The encoder transfer function, shown on page 1, characterizes this A/D converter system. The first task of this system is to determine the polarity of the incoming analog signal and to generate a corresponding SB input value. When the proper $\overline{START}$, $(\overline{S})$, and $\overline{CONVERSION\ COMPLETE}$, $(\overline{CC})$, signal levels are set, the first clock pulse sets the MSB output of the SAR, Am2502, to a logic 0 and sets all other parallel digital outputs to logic 1 levels. At the same time, the flip-flop is triggered, and its output provides the $E/\overline{D}$ input with a logic 0 level. No current flows into the I_{OE} outputs. This disconnects the converter from the comparator inputs, and the incoming analog signal can be compared with the ground applied to the opposite comparator input. The resulting comparator output is fed to the Am2502 serial data input, D, through an exclusive-or gate. At the same time, the second input to the same exclusive-or gate is held at a logic 0 level by the additional successive approximation logic shown in Figure 3. This exclusive-or gate inverts the comparator's outputs whenever a negative signal polarity is detected. This maintains the proper output current coding, i.e., all ones for full scale and all zeros for zero scale.

The second clock pulse changes the $E/\overline{D}$ input back to a logic 1 level because the $\overline{CC}$ signal changed. It also clocks the D input signal of the Am2502 to its MSB output, and transfers it to the SB input of the Am6071. Depending upon the SB input level, current will flow into the $I_{OE(+)}$ or $I_{OE(-)}$ output of the Am6071.

Nine clock pulses are required to obtain a digital binary representation of the incoming analog signal at the eight Am2502 digital outputs. The resulting Am6071 analog output signal is compared with the analog input signal after each of the nine successive clock pulses. The analog signal should not be allowed to change its value during the data conversion time. In high speed systems, fast changes of the analog signals at the A/D system input are usually prevented by using sample and hold circuitry.

Additional Considerations and Recommendations

In Figure 1, an optional operational amplifier converts the Am6071 output current to a bipolar voltage output. When the SB input is a logic 1, sink current appears at the amplifier's negative input, and the amplifier acts as a current to voltage converter, yielding a positive voltage output. With the SB value at a logic 0, sink current appears at the amplifier's positive input. The amplifier behaves as a voltage follower, and the true current outputs will swing below ground with essentially no change in output current. The SB input steers current into the appropriate (+) or (−) output of the Am6071. The resulting operational amplifier's output in Figure 1 should ideally be symmetrical with resistors R1 and R2 matched.

In Figure 2, two operational amplifiers measure the currents of each of the four Am6071 analog outputs. Resistor tolerances of 0.1% give 0.1% output measurement error (approximately $2\mu A$ at full scale). The input offset currents of the A1 and A2 devices also increase output measurement error and this error is most significant near zero scale. The Am101A and 308 devices, for example, may be used for A1 and A2 since their maximum offset currents, which would add directly to the measurement error, are only 10nA and 1nA respectively. The input offset voltages of the A1 and A2 devices, with output resistor values of $2.5k\Omega$, also contribute to the output measurement error by a factor of 400nA for
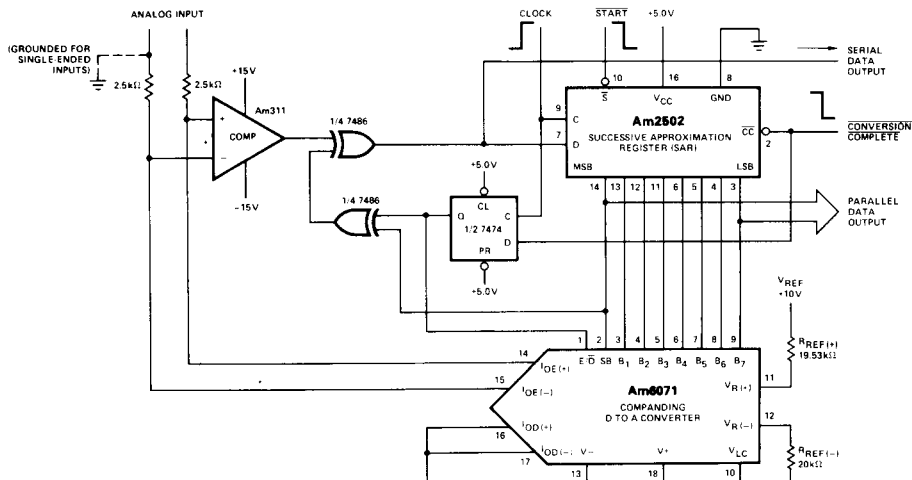
every mV of offset. Therefore, to minimize error, the offset voltages of A1 and A2 should be nulled.

The recommended operating range for the reference current I_{REF} is from 0.1mA to 1.0mA. The full scale output current, I_{FS}, is a linear function of the reference current, and may be calculated from the equation $I_{FS} = 3.94\ I_{REF}$. This tight relationship between I_{REF} and I_{FS} alleviates the requirement for trimming the I_{REF} current if the R_{REF} resistor values are within ±1% of the calculated value. Lower values of I_{REF} will reduce the negative power supply current, $(I-)$, and will increase the reference amplifier negative common mode input voltage range.

The ideal value for the reference current $I_{REF} = V_{REF}/R_{REF}$ is $512\mu A$. The corresponding ideal full scale decode and encode current values are $2016\mu A$ and $2048\mu A$, respectively. A percentage change from the ideal I_{REF} value produced by changes in V_{REF} or R_{REF} values produces the same percentage change in decode and encode output current values. The positive voltage supply, $V+$, may be used, with certain precautions, for the positive reference voltage V_{REF}. In this case, the reference resistor $R_{REF(+)}$ should be split into two resistors and their junction bypassed to ground with a capacitor of $0.01\mu F$. The total resistor value should provide the reference current $I_{REF} = 512\mu A$. The resistor $R_{REF(-)}$ value should be approximately equal to the $R_{REF(+)}$ value in order to compensate for the errors caused by the reference amplifier's input offset current.

An alternative to the positive reference voltage applications shown in Figures 1, 2 and 3 is the application of a negative voltage to the $V_{R(-)}$ terminal through the resistor $R_{REF(-)}$ with the $R_{REF(+)}$ resistor tied to ground. The advantage of this arrangement is the presence of very high impedance at the $V_{R(-)}$ terminal while the reference current flows from ground through $R_{REF(+)}$ into the $V_{R(+)}$ terminal.

The Am6071 has a wide output voltage compliance suitable for driving a variety of loads. With $I_{REF} = 512\mu A$ and $V- = -15V$, positive voltage compliance is +18V and negative

voltage compliance is $-5.0V$. For other values of I_{REF} and $V-$, the negative voltage compliance, $V_{OC(-)}$, may be calculated as follows:

$$V_{OC(-)} = (V-) + 2(I_{REF} \cdot 1.55k\Omega) + 8.4V,$$

where $1.55k\Omega$ and $8.4V$ are equivalent worst case values for the Am6071.

The following table contains $V_{OC(-)}$ values for some specific $V-$, I_{REF}, and I_{FS} values.

Negative Output Voltage Compliance $V_{OC(-)}$

$V-$	I_{REF} (I_{FS})		
	$256\mu A$ (1mA)	$512\mu A$ (2mA)	$1024\mu A$ (4mA)
$-12V$	$-2.8V$	$-2.0V$	$-0.4V$
$-15V$	$-5.8V$	$-5.0V$	$-3.4V$
$-18V$	$-8.8V$	$-8.0V$	$-6.4V$

The V_{LC} input can accommodate various logic input switching threshold voltages allowing the Am6071 to interface with various logic families. This input should be placed at a potential which is 1.4V below the desired logic input switching threshold. Two external discrete circuits which provide this function for non-TTL driven inputs are shown in Figure 4. For TTL-driven logic inputs, the V_{LC} input should be grounded. If negative voltages are applied at the digital logic inputs, they must have a value which is more positive than the sum of the chosen $V-$ value and +10V.

With a $V-$ value chosen between $-15V$ and $-11V$, the $V_{OC(-)}$, the input reference common mode voltage range, and the logic input negative voltage range are reduced by an amount equivalent to the difference between $-15V$ and the $V-$ value chosen.

With a $V+$ value chosen between +5V and +15V, the reference amplifier common mode positive voltage range and the V_{LC} input values are reduced by an amount equivalent to the difference between +15V and the $V+$ value chosen.
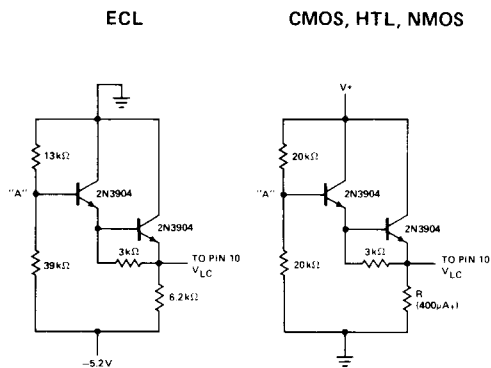
Figure 4. Interfacing Circuits for ECL, CMOS, HTL, and NMOS Logic Inputs.

(See Notes 2 and 3)
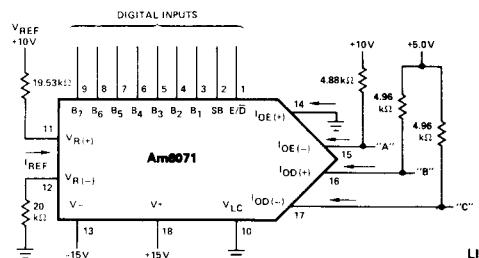
LIC-265

LIC-266

INPUT CODE (E/D̄, SB, B₁, . . ., B₇)	OUTPUT VOLTAGE (V)			
	"A"	"B"	"C"	DIFF
10 111 1111	0	N/A	N/A	N/A
10 110 1111	+5.00			
10 000 0000	+10.00			
01 111 1111	N/A	−5.00	+5.00	−10.00
01 110 1111		+0.00	+5.00	−5.00
01 000 0000		+5.00	+5.00	0
00 000 0000		+5.00	+5.00	0
00 110 1111		+5.00	+0.00	+5.00
00 111 1111		+5.00	−5.00	+10.00

Figure 5. Resistive Output Connections

ADDITIONAL DECODE OUTPUT CURRENT TABLES

Table 3
Normalized Decoder Output (Sign Bit Excluded)

STEP (S)		CHORD (C)							
		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	1	33	66	132	264	528	1056	2112
1	0001	3	35	70	140	280	560	1120	2240
2	0010	5	37	74	148	296	592	1184	2368
3	0011	7	39	78	156	312	624	1248	2496
4	0100	9	41	82	164	328	656	1312	2624
5	0101	11	43	86	172	344	688	1376	2752
6	0110	13	45	90	180	360	720	1440	2880
7	0111	15	47	94	188	376	752	1504	3008
8	1000	17	49	98	196	392	784	1568	3136
9	1001	19	51	102	204	408	816	1632	3264
10	1010	21	53	106	212	424	848	1696	3392
11	1011	23	55	110	220	440	880	1760	3520
12	1100	25	57	114	228	456	912	1824	3648
13	1101	27	59	118	236	462	944	1888	3776
14	1110	29	61	122	244	488	976	1952	3904
15	1111	31	63	126	252	504	1008	2016	4032
STEP SIZE		2	2	4	8	16	32	64	128

The normalized decode current, $(I_{C,S})$, where C is chord number and S is step number, is calculated using: $I_{CS} = 2^C(S + 16.5)$ for $C \geq 1$, and $I_{C,S} = 2S + 1$ for $C = 0$. The ideal decode current, (I_{OD}), in μA is calculated using: $I_{OD} = (I_{C,S}/I_{7,15(norm.)}) \cdot I_{FS}(\mu A)$, where $I_{C,S}$ is the corresponding normalized current.

Table 4
Normalized Encoder Output (Sign Bit Excluded)

STEP (S)		CHORD (C)							
		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	2	34	68	136	272	544	1088	2176
1	0001	4	36	72	144	288	576	1152	2304
2	0010	6	38	76	152	304	608	1216	2432
3	0011	8	40	80	160	320	640	1280	2560
4	0100	10	42	84	168	336	672	1344	2688
5	0101	12	44	88	176	352	704	1408	2816
6	0110	14	46	92	184	368	736	1472	2944
7	0111	16	48	96	192	384	768	1536	3072
8	1000	18	50	100	200	400	800	1600	3200
9	1001	20	52	104	208	416	832	1664	3328
10	1010	22	54	108	216	432	864	1728	3456
11	1011	24	56	112	224	448	896	1792	3584
12	1100	26	58	116	232	464	928	1856	3712
13	1101	28	60	120	240	480	960	1920	3840
14	1110	30	62	124	248	496	992	1984	3968
15	1111	32	64	128	256	512	1024	2048	4096
STEP SIZE		2	2	4	8	16	32	64	128

ADDITIONAL DECODE OUTPUT CURRENT TABLES (Cont.)

Table 5
Decoder Step Size Summary

Chord	Step Size Normalized to Full Scale	Step Size in μA with 2016μA F. S.	Step Size as a % of Full Scale	Step Size in dB at Chord Endpoints	Step Size as a % of Reading at Chord Endpoints	Resolution & Accuracy of Equivalent Binary DAC
0	2	1.0	0.05%	0.58	6.45%	Sign + 11 Bits
1	2	1.0	0.05%	0.28	3.17%	Sign + 11 Bits
2	4	2.0	0.1%	0.28	3.17%	Sign + 10 Bits
3	8	4.0	0.2%	0.28	3.17%	Sign + 9 Bits
4	16	8.0	0.4%	0.28	3.17%	Sign + 8 Bits
5	32	16.0	0.8%	0.28	3.17%	Sign + 7 Bits
6	64	32.0	1.6%	0.28	3.17%	Sign + 6 Bits
7	128	64.0	3.2%	0.28	3.17%	Sign + 5 Bits

Table 6
Decoder Chord Size Summary

| Chord	Chord Endpoints Normalized to Full Scale	Chord Endpoints in μA with 2016μA F. S.	Chord Endpoints as a % of Full Scale	Chord Endpoints in dB Down from Full Scale
0	31	15.5	0.77%	−42.28
1	63	31.5	1.56%	−36.12
2	126	63.0	3.13%	−30.10
3	252	126.0	6.25%	−24.08
4	504	252.0	12.5%	−18.06
5	1008	504.0	25.0%	−12.04
6	2016	1008.0	50.0%	−6.02
7	4032	2016.0	100%	0

BASIC CIRCUIT CONNECTIONS

±10V RANGE ENCODER/DECODER CONNECTIONS
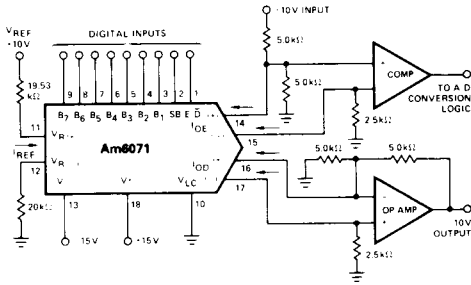
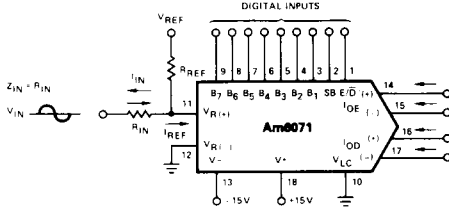LIC-267

COMPLIANCE EXTENSION USING AC COUPLED OUTPUT
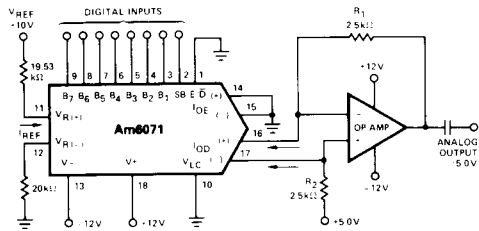
IDEAL VALUES:

$I_{REF} = 512\mu A$

$I_{FS} = 2016\mu A$
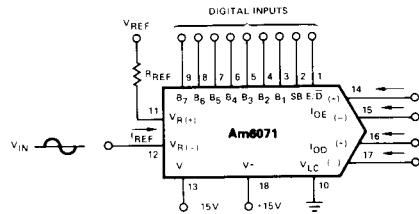
LIC-268

LOW INPUT IMPEDANCE CONNECTION

$I_{REF} = V_{IN}/R_{IN} + V_{REF}/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$
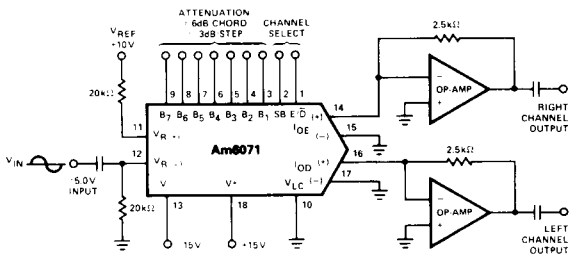
LIC-269

HIGH INPUT IMPEDANCE CONNECTION

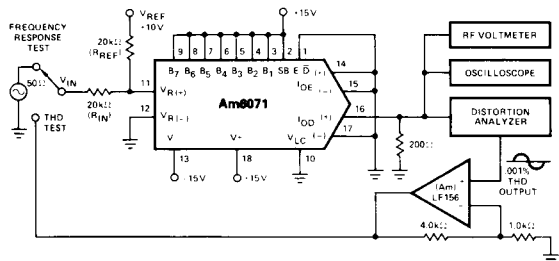$I_{REF} = (V_{REF} - V_{IN})/R_{REF}$

$I_{FS} \approx 4 \cdot I_{REF}$

LIC-270

LOGARITHMIC DIGITAL GAIN CONTROL
(Notes 4 & 5)

LIC-271

REFERENCE AMPLIFIER DYNAMIC TEST CIRCUIT

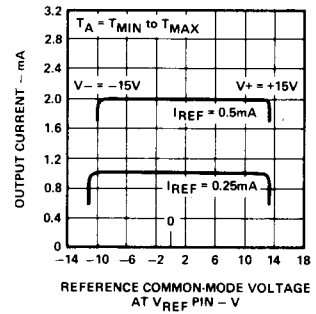LIC-272

3

TYPICAL PERFORMANCE CURVES

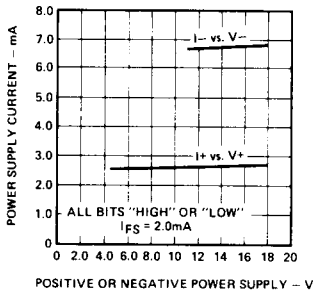**Reference Amplifier Total Harmonic Distortion Versus Frequency (80kHz Filter) (Notes 6, 7, 8)**
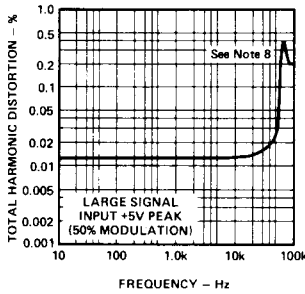
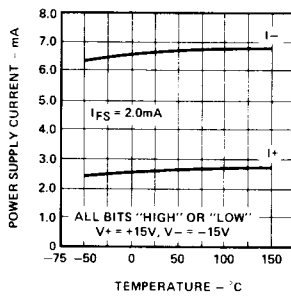**Reference Amplifier Input Frequency Response**
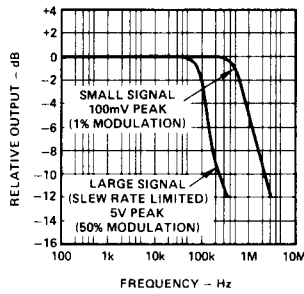
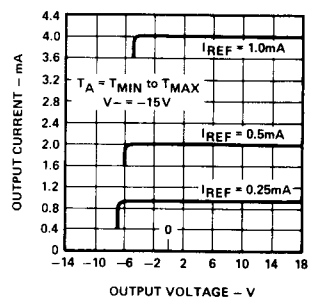**Reference Amplifier Input Common-Mode Range (Note 9)**

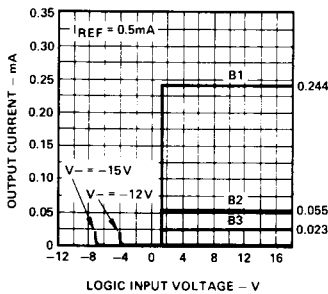**Power Supply Currents Versus Power Supply Voltages**
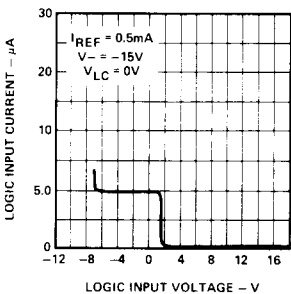
Power Supply Currents Versus Temperature

Output Current Versus Output Voltage (Output Voltage Compliance)
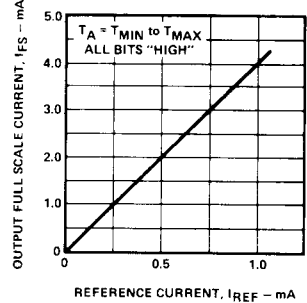
Bit Transfer Characteristics (Note 10)

Logic Input Current Versus Input Voltage and Logic Input Range (Note 11)

Output Full Scale Current Versus Reference Input Current

LIC-273

Notes: 6. THD is nearly independent of the logic input code.
7. Similar results are obtained for a high input impedance connection using $V_{R(-)}$ as an input.
8. Increased distortion above 50kHz is due to a slew rate limiting effect which determines the large signal bandwidth. For an input of ±2.5V peak (25% modulation), the bandwidth is 100kHz.
9. Positive common mode range is always (V+) −1.5V.
10. All bits are fully switched with less than a half step error at switching points which are guaranteed to lie between 0.8V and 2.0V over the operating temperature range.
11. The logic input voltage range is independent of the positive power supply and logic inputs may swing above the supply.

APPLICATIONS

The companding D/A converter is particularly suited for applications requiring a wide dynamic range.

Systems requiring fine control resulting in a constant rate of change or set point controls are economically achieved using these devices.

Instrumentation, Control and μ-Processor based applications include:
Digital data recording
PCM telemetry systems
Servo systems
Function generation
Data acquisition systems

Telecommunications applications include:
PCM Codec telephone systems
Intercom systems
Military voice communication systems
Radar systems
Voice Encryption

Audio Applications:
Recording
Multiplexing of analog signals
Voice synthesis

Other companding converters offered by Advanced Micro Devices:

If particular interest lies in a companding D/A converter operating to the D3 compandor tracking specification and meeting the Bell System μ-255 companding law, see the Am6072 data sheet.

For a CCITT unit having an A-law characteristic see the Am6073 data sheet.

μ-law applications other than telecommunications systems are described in the Am6070 data sheet.

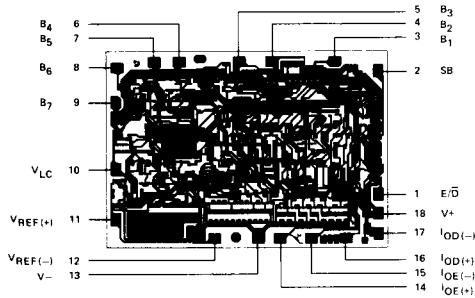# SERIAL DATA TRANSCEIVING CONVERTER
(1/2 OF SYSTEM SHOWN)
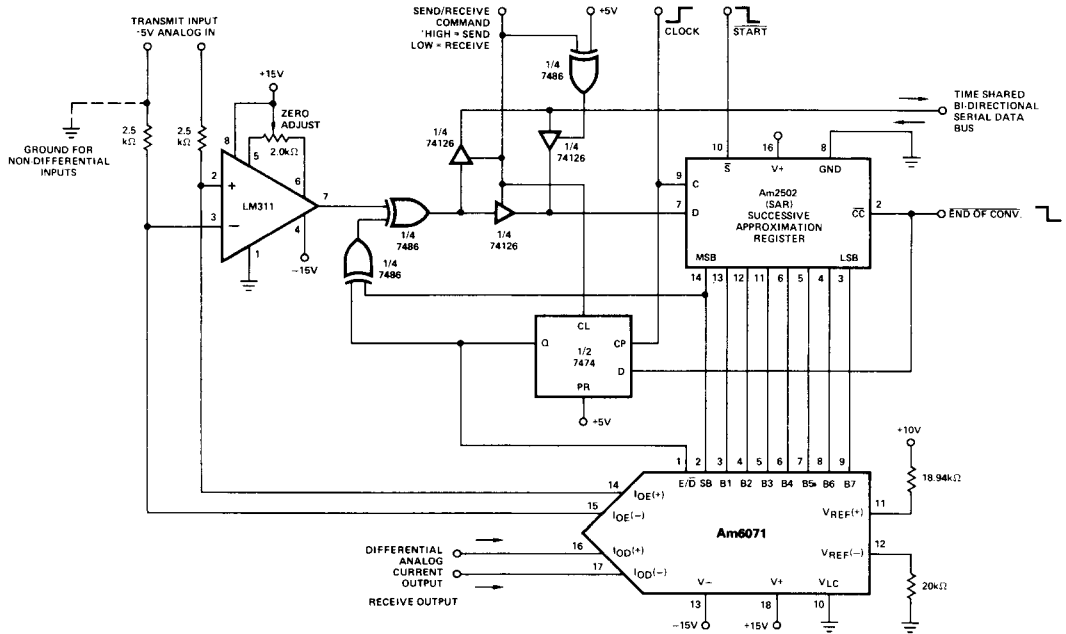
LIC-274

Notes:
1. Complementary send/receive commands are required for the two ends.
2. START must be held low for one clock cycle to begin a send or receive cycle.
3. The SAR is used as a serial-in/parallel out register in the receive mode.
4. CLOCK and START may be connected in parallel at both ends.
5. Conversion is completed in 9 clock cycles.
6. Receive output is available for one full clock cycle.

Metallization and Pad Layout

80 X 114 Mils