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AN231E04 Datasheet Rev 1.0

3rd Generation

Dynamically Reconfigurable dpASP

This device is RoHS compliant

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AN231E04 Datasheet – Dynamically Reconfigurable dpASP

PRODUCT AND ARCHITECTURE OVERVIEW

The AN231E04 device is an “Analog Signal Processor”; ideally suited to signal conditioning, filtering, gain, rectification, summing, subtracting, multiplying, etc. The device also accommodates nonlinear functions such as sensor response linearization and arbitrary waveform synthesis.

The AN231E04 device consists of a 2x2 matrix of fully Configurable Analog Blocks (CABs), surrounded by programmable interconnect resources and analog input/output cells with active elements. On chip clock generator block controls multiple non-overlapping clock domains generated from an external stable clock source. Internal band-gap reference generator is used to create temperature compensated reference voltage levels. The inclusion of an 8x256 bit look-up table enables waveform synthesis and several non-linear functions.

Configuration data is stored in an on-chip SRAM configuration memory. An SPI like interface is provided for simple serial load of configuration data from a microprocessor or DSP. This memory is shadowed allowing a different circuit configuration to be loaded as a background task without disrupting the current circuit functionality.

The AN231E04 device features seven configurable input/output structures each can be used as input or output, 4 of the 7 have integrated differential amplifiers. There is also a single chopper stabilized amplifier that can be used by 3 of the 7 output cells.

Circuit design is enabled using Anadigmdesigner2 software, a high level block diagram based circuitry entry tool. Circuit functions are represented as CAMs (Configurable Analog Modules) these are configurable block which map onto portions of CABs. The software and a development board facilitate instant prototyping of any circuit captured in the tool.

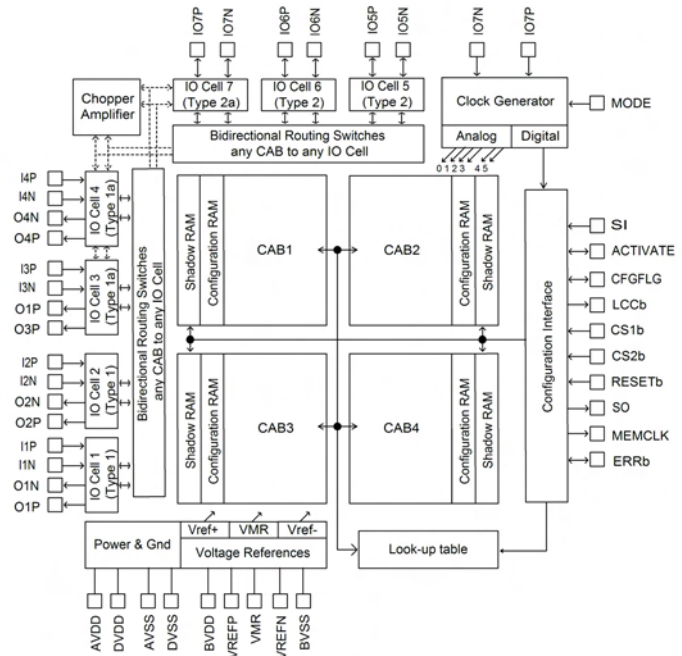


Figure 1: Architectural overview of the AN231E04 device
With dynamic reconfigurability, the functionality of the AN231E04 can be reconfigured in-system by the designer or on-the-fly by a microprocessor. A single AN231E04 can thus be programmed to implement multiple analog functions and/or to adapt on-the-fly to your circuit requirements.

PRODUCT FEATURES

- Dynamic reconfiguration
- Seven configurable I/O cells, two dedicated output cells
- Fully differential architecture
- I/O buffering with single ended to differential conversion
- Low input offset through chopper stabilized amplifiers
- 256 Byte Look-Up Table (LUT) for linearization and arbitrary signal generation
- Typical Signal Bandwidth: DC-2MHz (Bandwidth is CAM dependent)
- Signal to Noise Ratio:
 - Broadband 90dB
 - Narrowband (audio) 120dB
- Total Harmonic Distortion (THD): 100dB
- User controlled Compensated low DC offset <250µV
- DC Offset via chopper stabilized architecture <50uV
- Package: 44-pin QFN (7x7x0.9mm)
 - Lead pitch 0.5mm
- Supply voltage: 3.3V

ORDERING CODES

AN231E04-e2-QFNTY dpASP Tray (260 /tray, 2600/box)
 AN231E04-e2-QFNTR dpASP Tape & Reel (1000 /reel, 4000/box)

APPLICATIONS

- Analog Signal Processing
- RFID IF (Baseband Filtering)
- Real-time software control of analog system peripherals
- Intelligent sensors
- Adaptive filtering and control
- Adaptive DSP front-end
- Adaptive industrial control and automation
- Self-calibrating systems
- Compensation for aging of system components
- Dynamic recalibration of remote systems
- Ultra-low frequency signal conditioning
- Custom analog signal processing

[For more detailed information on the features of the AN231E04 device, please refer to the AN131E04/AN231E04 User Manual]

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1 ELECTRICAL CHARACTERISTICS

1.1 Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--------------------------------|--|---------|-----|------------|------|---|
| DC Power Supplies ^a | AVDD BVDD DVDD | -0.5 | - | 3.6 V | V | AVSS, BVSS and DVSS all held to 0.0 V |
| xVDD to yVDD Offset | | -0.5 | | 0.5 | V | Ideally all supplies should be at the same voltage |
| Package Power Dissipation, | P _{max} 25°C P _{max} 85°C | - | - | 4.5 1.8 | W | (Theoretical values based on T _j =125deg.C) Still air, No heatsink, 44 pads and exposed die pad soldered to PCB θ _{ja} = 22.5°C/W. VDD = 3.3V |
| AN231E04 max power dissipation | dpASP _{max} | - | - | 0.25 | W | Maximum power dissipation all resources used, (see section 1.5.13 for more detail). |
| Input Voltage | V _{inmax} | VSS-0.5 | - | VDD+0.5 | V | |
| Ambient Operating Temperature | T _{op} | -40 | - | 85 | °C | |
| Storage Temperature | T _{stg} | -40 | | 125 | °C | |

^a Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for VDD of up to 5 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

1.2 Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------------|----------------------|---------------------------|-----|---------------------------|------|--|
| DC Power Supplies | AVDD BVDD DVDD | 3.0 | 3.3 | 3.6 | V | AVSS, BVSS and DVSS all held to 0 V |
| Analog Input Voltage. | V _{ina} | V _{MR} -1.375 | - | V _{MR} +1.375 | V | Conditional on the circuit which is being driven. This limit is defined as maximum signal amplitude through input Sample and hold cell which results in >-80dB THD+N using a 1KHz test signal. V _{MR} is 1.5 volts above AVSS |
| Digital Input Voltage | V _{ind} | 0 | - | DVDD | V | |
| Junction Temp ^b | T _j | -40 | - | 125 | °C | Assume a package θ _{ja} =22.5°C/W |

^b To calculate the junction temperature (T_j) you must first empirically determine the current draw (total I_{dd}) for the design. The programmable nature of this device means this can vary by orders of magnitude between different circuit designs. Once the current consumption is established then the following formula can be used; T_j = T_a + I_{dd} x VDD x 22.5 °C/W, where T_a is the ambient temperature. Worst case θ_{ja} = 22.5 °C/W assumes no air flow and no additional heatsink, 44 pads and the exposed die pad soldered to PCB.

1.3 General Digital I/O Characteristics (VDD = 3.3v +/- 10%, -40 to 85 deg.C)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-----------------------|---------------------|-----|-----|------|------|--|
| Input Voltage Low | V _{ih} | 0 | - | 30 | - | % of DVDD |
| Input Voltage High | V _{il} | 70 | - | 100 | - | % of DVDD |
| Output Voltage Low | V _{ol} | 0 | - | 20 | - | % of DVDD |
| Output Voltage High | V _{oh} | 80 | - | 100 | - | % of DVDD |
| Input Leakage Current | I _{il} | - | - | +/-1 | µA | Some pins have active pull up/down, please see below. |
| Max. Capacitive Load | C _{max} | - | - | 10 | pF | |
| Min. Resistive Load | R _{min} | 50 | - | - | Kohm | Each pins has a specific load driving capability, detailed in sections 1.4 and 1.5 |
| ACLK Frequency | F _{max} | - | 16 | 40 | MHz | Divide down to <4 MHz prior to use as a CAB clock |
| Clock Duty Cycle | CLK _{duty} | 45 | - | 55 | % | All clocks |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.4 Digital I/O Characteristics (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

1.4.1 Pins ACLK, SCLK, RESETb, CS1b, CS2b, SI, MODE (standard CMOS inputs)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--------------------|--------|-----|-----|-----|------|-----------|
| Input Voltage Low | Vil | 0 | - | 30 | % | % of DVDD |
| Input Voltage High | Vih | 70 | - | 100 | % | % of DVDD |

1.4.2 Pin SO, (standard CMOS output)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------|---------|------|-----|-----|------|--|
| Output Voltage Low | Vol | VSS | - | VSS | mV | Load 10pF//50Kohm to VSS |
| Output Voltage High | Voh | 3.28 | - | VDD | V | Load 10pF//50Kohm to VSS VDD = 3.3 V. |
| Max. Capacitive Load | Cmax | - | - | 100 | pF | Maximum load 100 pF // 5 Kohm at up to 5MHz. |
| Min. Resistive Load | Rmin | 5 | - | - | Kohm | Maximum load 100 pF // 5 Kohm at up to 5MHz. |
| Current Sink | Isnkmax | 60 | 100 | 135 | mA | Pin shorted to VDD Current should be limited externally so that it does not exceed 3mA |
| Current Source | Isrcmax | 50 | 80 | 110 | mA | Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA |

1.4.3 Digital functions of mixed signal Pins IO1, IO2, IO3, IO4, IO5, IO6, IO7,

These pins can be configured by the user to be standard CMOS input or outputs.

I/O cells 5, 6 and 7 the pin pairs can be connected to and used individually.

I/O cells 1 through 4 provide pin pairs for differential (complimentary) digital connections.

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------|---------|------|-----|-----|------|---|
| Input Voltage Low | Vil | 0 | | 30 | % | % of DVDD |
| Input Voltage High | Vih | 70 | | 100 | % | % of DVDD |
| Output Voltage Low | Vol | VSS | - | VSS | mV | Pin load = 20pF//10K to VSS |
| Output Voltage High | Voh | 3.25 | - | VDD | V | Pin load = 20pF//10K to VSS VDD = 3.3 V. |
| Max. Capacitive Load | Cmax | - | - | 50 | pF | Maximum load 20 pF // 10 Kohm at up to 4MHz signal |
| Min. Resistive Load | Rmin | 50 | - | - | Kohm | Maximum load 20 pF // 10 Kohm at up to 4MHz signal |
| Current Sink | Isnkmax | 15 | 30 | 40 | mA | Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA |
| Current Source | Isrcmax | 15 | 25 | 35 | mA | Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA. |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.4 Digital I/O Characteristics continued (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

1.4.4 Pins ERRb (Open Drain, CMOS transistor)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---------------------------|------------|------|-----|------|------|--|
| Input Voltage Low | Vil | 0 | | 30 | % | % of DVDD, |
| Input Voltage High | Vih | 70 | | 100 | % | % of DVDD |
| Output Voltage Low | Vol | VSS | - | 7.0 | mV | 10KOhm to VDD VDD = 3.3 V. |
| Output Voltage High | Voh | 3.29 | - | VDD | V | 10KOhm to VDD VDD = 3.3 V. |
| Max. Capacitive Load | Cmax | - | - | 10 | pF | Maximum load 10 pF // 50 Kohm at full BW |
| Min. Resistive Load | Rmin | 50 | - | - | Kohm | Maximum load 10 pF // 50 Kohm at full BW |
| Current Sink | Isnkmax | 50 | - | 110 | mA | Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA |
| Current Source | Isrcmax | - | - | +/-1 | µA | Pin shorted to VSS |
| External Resistive Pullup | Rpullupext | 10 | 10 | 10 | Kohm | MUST be used |

1.4.5 Pins ACTIVATE, CFGFLGb

These pins are Open Drain CMOS transistors, with optional user configurable internal pull-up resistor
We also note that the output voltage on these pins is "sensed" by internal circuitry, (see figure 2 below)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|------------|------|-----|------|------|---|
| Input Voltage Low | Vil | 0 | | 30 | % | % of DVDD |
| Input Voltage High | Vih | 70 | | 100 | % | % of DVDD |
| Output Voltage Low | Vol | 80 | - | 140 | mV | Pin load = Internal pullup + external 10pF//50K to VSS VDD = 3.3 V. |
| Output Voltage High, internal pull-up. | Voh | 3.05 | - | 3.16 | V | Pin load = Internal pullup + external 10pF//50K to VSS VDD = 3.3 V. |
| Output Voltage Low, external pull-up. | VolE | 529 | - | 773 | mV | Pin load = 5K to VSS VDD = 3.3 V. |
| Output Voltage High | Voh | VDD | - | VDD | V | Pin load = 5K + 10pF to VSS |
| Max. Capacitive Load | Cmax | - | - | 10 | pF | Maximum load 10 pF // 50 Kohm at full BW |
| Min. Resistive Load | Rmin | 50 | - | - | Kohm | Maximum load 10 pF // 50 Kohm at full BW |
| Current Sink, pull down only | Isnkmax | 1.8 | - | 3.7 | mA | Pin shorted to VDD. |
| Current Source, pull up only | Isrcmax | 0.34 | - | 1.1 | mA | Pin shorted to VSS. |
| Internal Resistive Pullup | Rpullupint | 3.5 | 5.3 | 8.4 | Kohm | Default, not used with external pullup. |
| External Resistive Pullup | Rpullupext | 5 | 7.5 | 10 | Kohm | Optional - to be used only if internal pullup is deselected |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.4 Digital I/O Characteristics continued (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

1.4.6 Pin LCCb/DOUT1 (CMOS Output)

The primary function of this pin is as LCCb (Local Configuration Complete), this signal is used in multiple dpASP designs to pass Chips Select from dpASP to dpASP enabling primary configuration of a serial chain of dpASP's from a single SPI bus, please refer to the AN231E04 User Guide for details.

If the LCCb signal pin is not required (e.g. a circuit design with a single dpASP device) then via dpASP configuration this pin can be used as a digital output, this is realized by adjusting the properties of the dpASP "digital I/O cell".

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------------|------|------|------|------|---|
| Output Voltage Low, (LCCb) | Vol(LCCb) | VSS | - | VSS | mV | Load 10pF//50Kohm to VSS, during configuration. |
| Output Voltage High, (LCCb) | Voh(LCCb) | 3.00 | - | 3.20 | V | Load 10pF//50Kohm to VSS, during configuration. VDD = 3.3 V |
| Output Voltage Low, (DOUT1) | Vol(DOUT1) | VSS | - | VSS | mV | Load 10pF//50Kohm to VSS, When configured to pin39=DOUT1 |
| Output Voltage High, (DOUT1) | Voh(DOUT1) | 3.29 | - | VDD | V | Load 10pF//50Kohm to VSS, When configured to pin39=DOUT1 VDD = 3.3 V. |
| Max. Capacitive Load | Cmax | - | - | 10 | pF | Maximum load 10 pF // 50 Kohm |
| Min. Resistive Load | Rmin | 50 | - | - | Kohm | Maximum load 10 pF // 50 Kohm |
| Current Sink, (LCCb) | Isnk(LCCb) | 3.0 | - | 7.0 | mA | LCCb (pin 39) shorted to VDD, during configuration. Current should be limited externally so that it does not exceed 3mA. |
| Current Source, (LCCb) | Isrc(LCCb) | 0.25 | - | 0.80 | mA | LCCb (pin 39) shorted to VSS, during configuration. |
| Current Sink, (DOUT1) | Isnk(DOUT1) | 20.0 | - | 60.0 | mA | DOUT1 (pin 39) shorted to VDD,. Current should be limited externally so that it does not exceed 3mA. |
| Current Source, (DOUT1) | Isrc(DOUT1) | 12.5 | - | 35.0 | mA | DOUT1 (pin 39) shorted to VSS, Current should be limited externally so that it does not exceed 3mA. |
| Clock skew (DOUT1 connected to "clocka") | CLK _{SKREW} | - | 8.0 | - | ns | Skew at DOUT1 (pin 39) relative to external signal clock applied to input pin ACLK (pin 34). Note; This is only valid when DOUT1 is selected to output the CAM clockA, and CAM clockA is derived from ACLK divided by1. |
| Comparator skew (DOUT1 connected to "comparator") | COMP _{SKREW} | - | 25.0 | - | ns | This is the delay of the comparator CAM output transition relative to the exported comparator clock clock appears on the output pin. Note. The comparator is clocked with a user programmable CAM clock derived from a division of ACLK |
| RAM transfer delay (DOUT1 connected to "RAM transfer Pulse") | RAM _{DELAY} | - | 20.0 | - | ns | This is the delay of the signal at the dpASP pin 39, (DOUT1) relative to the actual internal transfer event. |
| Auto-null/Osc start delay (DOUT1 connected to "Auto-null/Osc start done" signal) ¹ | DONE _{DELAY} | - | 40 | - | ms | This is the delay of the signal at the dpASP pin 39, (DOUT1) relative to the actual internal event. |

¹ see application note AN231002 "Auto-nulling within the AN231E04"

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.4 Digital I/O Characteristics, continued (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

1.4.7 MEMCLK/DOUT2 (CMOS Output)

The primary function of this pin is as MEMCLK (Memory Clock), this signal is used as a clock output in circuit designs which require configuration from an SPI PROM (or SPI EEPROM), please refer to the AN231E04 User Guide for details. If the MEMCLK signal pin is not required (e.g. a circuit configured from a microcontroller) then via dpASP configuration this pin can be used as a digital output.

The MEMCLK signal is only active when the dpASP MODE (pin35) is high (tied to VDD).

DOUT2 function cannot be used if dpASP MODE (pin35) is high (tied to VDD).

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------------|------|------|------|------|---|
| Output Voltage Low, (MODE pin 35 = VSS, DOUT2 inactive) | V _{ol} | VSS | - | VSS | mV | Load 10pF//50Kohm to VSS. This Pin MEMCLK is unused in this MODE=VSS, there is an internal weak pull down resistor |
| Output Voltage Low, (MODE pin 35 = VSS, DOUT2 active) | V _{ol} | VSS | - | VSS | mV | Load 100pF//5Kohm to VSS |
| Output Voltage Low, (MODE pin 35 = VDD) | V _{ol} | VSS | - | VSS | mV | Load 100pF//5Kohm to VSS |
| Output Voltage High | V _{oh} | 3.28 | - | VDD | V | Load 100pF//5Kohm to VSS, VDD = 3.3V. |
| Max. Capacitive Load | C _{max} | - | - | 100 | pF | Maximum load 100 pF // 5 Kohm |
| Min. Resistive Load | R _{min} | 5 | - | - | Kohm | Maximum load 100 pF // 5 Kohm |
| Current Sink, (MODE pin 35 = VSS & DOUT2 inactive) | I _{snk} | 0.01 | 0.03 | 0.05 | mA | Pin shorted to VDD. Th This Pin MEMCLK is unused when MODE=VSS and DOUT2 is inactive. Thus No active drive. |
| Current Source, (MODE pin 35 = VSS & DOUT2 inactive) | I _{src} | - | - | +/-1 | uA | Pin shorted to VSS. This Pin MEMCLK is unused when MODE=VSS and DOUT2 is inactive. Thus No active drive. |
| Current Sink, (MODE pin 35 = VDD or DOUT2 active) | I _{snk} | 60 | 100 | 135 | mA | Pin shorted to VDD. Current should be limited externally so that it does not exceed 3mA |
| Current Source, (MODE pin 35 = VDD or DOUT2 active) | I _{src} | 50 | 80 | 110 | mA | Pin shorted to VSS. Current should be limited externally so that it does not exceed 3mA |
| Clock skew (DOUT2 connected to "clocka") | CLK _{SKEW} | - | 8.0 | - | ns | Skew at DOUT2 (pin 42) relative to external signal clock applied to input pin ACLK (pin 34). Note; This is only valid when DOUT2 is selected to output the CAM clockA, and CAM clockA is derived from ACLK divided by1. |
| Comparator skew (DOUT2 connected to "comparator") | COMP _{SKEW} | - | 25.0 | - | ns | This is the delay of the comparator CAM output transition relative to the exported comparator clock clock appears on the output pin. Note, The comparator is clocked with a user programmable CAM clock derived from a division of ACLK |
| RAM transfer delay (DOUT2 connected to "RAM transfer Pulse") | RAM _{DELAY} | - | 20.0 | - | ns | This is the delay of the signal at the dpASP pin 42, (DOUT2) relative to the actual internal transfer event. |
| Auto-null/Osc start delay (DOUT2 connected to "Auto-null/Osc start done" signal) ² | DONE _{DELAY} | - | 40 | - | ms | This is the delay of the signal at the dpASP pin 42, (DOUT2) relative to the actual internal event. |

² see application note AN231002 "Auto-nulling within the AN231E04"

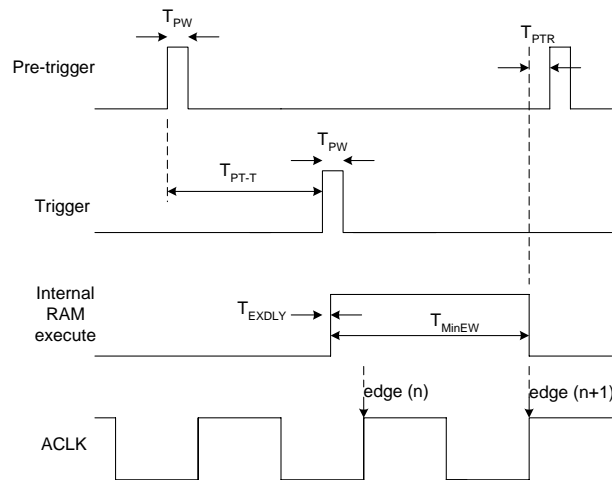
AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.4.8 RAM Transfer – Trigger and Arm

These digital inputs do not have dedicated pins, a connection exists within the dpASP, an external signal can be routed to either of these virtual pins from a type2 I/O cell (I/O cells 5, 6 and 7. Pins 15,16,17,18,19 or 20).

The purpose of these virtual pins is to extend optional asynchronous timing control of the dpASP configuration to the user.

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---------------------------------|--------|-----|--------|------|---|
| Input Voltage Low | V _{il} | 0 | | 30 | % | % of DVDD |
| Input Voltage High | V _{ih} | 70 | | 100 | % | % of DVDD |
| Minimum pulse width connected to where | T _{PW} setup time | 5 | - | - | ns | Time to register the event internally. |
| Pulse-Pulse edge delay | T _{PT-T} setup time | 10 | - | - | ns | Delay between pre-trigger and trigger. Need not be observed if pre-trigger is not used, is set at the end of configuration automatically. |
| Execute delay | T _{EXDLY} | 0 | 10 | 20 | ns | Delay from trigger rising edge to internal execute event. |
| Execute minimum width | T _{MinEW} | 1 ACLK | - | 2 ACLK | - | Duration of execute pulse guaranteed 1 ACLK period. Can be as long as 2 periods depending on relative phases. |
| Pre-trigger reset. | T _{PTR} | 10 | - | - | ns | Pre-trigger circuit is reset ready to accept another pre-trigger. |



AnadigmDesigner2 options, (these are set using the software tool AnadigmDesigner2)

RAM Transfer Trigger = Automatic :

RAM transfer happens automatically immediately after the "end" byte of a configuration bit stream. Timing control is entirely inside the AN231E04 device and not visible to a user.

RAM Transfer Trigger = Event driven.

RAM Trigger = Off.

no pre-trigger used. The "end" byte of configuration bit stream arms the RAM transfer and the user signal then acts as the trigger.

Arm Trigger = On

External Signal Allowed = Trigger. This setting allows the external signal connected to be the trigger, Arming must be from an internal signal.

External Signal Allowed = Arm. This setting allows the external signal connected to be the arming signal, Trigger be from an internal signal.

RAM Transfer Trigger = Clock synch

RAM transfer happens automatically immediately following the first occurrence of all internal clocks being synchronous. Timing control is entirely inside the AN231E04 device and not visible to a user.

HINT: The RAM transfer timings above are for the trigger block hardware - The **Trigger** and **Arm** signals can come from many sources, propagation delays to the trigger block inputs will vary depending on the source and routing of the signals to this block.

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.5 Analog I/O Characteristics (VDD = 3.3v +/-10%, -40 to 85 deg.C unless commented)

1.5.1 Analog Inputs General

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-------------------------|----------|-------------|-----|-------------|------|--|
| Input Range | Vina | VMR - 1.375 | - | VMR + 1.375 | V | VMR set to 1.5V |
| Differential Input | Vdiffina | 0 | - | +/-2.75 | V | VMR = 1.5 V. |
| Common Mode Input Range | Vcm | 1.4 | 1.5 | 1.6 | V | Limited by signal clipping for large waveforms. Please see figures |
| Input Offset | VosIOInt | - | 3.0 | 18 | mV | IO cell, unity gain mode intrinsic |
| | VosIOAZ | - | 0.5 | 1.0 | mV | IO cell, unity gain mode, auto-null on. |
| | VosCabI | - | 3 | 18 | mV | CAB, unity gain mode. |
| | VosCabAZ | - | 250 | 1000 | uV | CAB, unity gain mode, auto-null on. |
| | VosCabzC | - | 75 | 250 | uV | CAB, unity gain mode, auto-null and chopping on. |
| Input Frequency | Fain | 0 | <2 | 8 | MHz | Max value is clock, CAM and input stage dependent. Input frequency for most CAMs is limited to approx <2MHz due to CAM signal processing which is based on sampled data architectures. |

1.5.2 IO Differential Operational Amplifier

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------|-------------|------|------------|--------|--|
| Output voltage range | Vinouta | VMR - 1.375 | - | VMR+ 1.375 | V | VMR = 1.5V. Measured for IO SnH circuit. |
| Differential Input/Output | Vdiffioa | - | - | +/- 2.75 | V | Common mode voltage = 1.5 V. Measured for IO SnH circuit. |
| Common Mode Input Voltage Range (Note1) | Vcm | VMR | VMR | VMR | V | Limited due to causing signal clipping for large waveforms. VMR can be varied if supplied externally (+200mV to -1.0volt) |
| Common Mode Output Voltage Deviation from VMR | Vcm | - | 23.5 | 72.7 | mV | Due to common mode offsets. |
| Equivalent Input Voltage Offset. | VoffsetI | - | 3.0 | 18.0 | mV | Intrinsic offset voltage. |
| Equivalent Input Voltage Offset. | VoffsetAZ | - | 500 | 1000 | uV | Auto-null offset voltage, rectangular distribution. |
| Auto-null time, from LCCb falling edge. | T _{AZ} | - | 60 | - | ms | see application note AN231002 "Auto-nulling within the AN231E04" |
| Offset Voltage Temperature Coefficient | VoffsetAZ TC | - | 4 | - | µV/°C | Auto-null mode, from -40°C to 125°C. |
| Power Supply Rejection Ratio | PSSR | 60 | - | - | dB | Sample and Hold mode, 1MHz clk, at DC |
| Common Mode Rejection Ratio | CMRR | 60 | - | - | dB | Sample and Hold mode, 1MHz clk, at DC |
| Differential Slew Rate | Slew | - | 50 | - | V/µsec | Opamp driving off chip with Max load. Effective internal slew is affected by the internal routing and load is normally much faster |
| Unity Gain Bandwidth. | UGB | - | 63 | - | MHz | 10pF external load |
| Open loop gain | Av | - | 103 | - | dB | |
| Input Impedance | Rin | 10 | - | - | Mohm | Voltage gain mode |
| Output Impedance | Rout | - | 33 | - | Ohms | Measured at package pins. Track impedance increases the |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

| | | | | | | |
|--------------------------------------|-------|---|------|-----|--------------------------------|--|
| | | | | | | effective output impedance. The OpAmp is designed to drive all internal nodes, |
| Output Load, External | Rload | 1 | - | - | Kohm | |
| Output Load, External | Cload | - | - | 100 | pF | |
| Noise Figure | NF | - | 0.16 | - | $\mu\text{V}/\sqrt{\text{Hz}}$ | Unity gain mode. |
| Signal-To Noise Ratio and Distortion | SINAD | - | 97 | - | dB | Unity gain mode. |
| Spurious Free Dynamic Range | SFDR | - | 96 | - | dB | Unity gain mode. |

1.5.3 IO Cell, Sample and Hold Mode

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---|------------------------|------|------|--------------------------------|--|
| Input Range | V _{ina} V _{dif} fina | See analog input above | | | | |
| Equivalent Input Offset Voltage | V _{osl} | - | 3 | 18 | mV | Non auto-null differential opamp offset ³ |
| | V _{osAZ} | - | 500 | 1000 | μV | Auto-null differential opamp offset ³ |
| Offset Voltage Temperature Coefficient | V _{offset} tAZ | - | 4 | - | $\mu\text{V}/^\circ\text{C}$ | With auto-null active. From -40°C to 125°C |
| Input Frequency | F _{ain} | 0 | - | 2 | MHz | Generally limited by aliasing to half Sample and Hold clock. |
| Power Supply Rejection Ratio | PSRR | 60 | - | - | dB | d.c. |
| Common Mode Rejection Ratio | CMRR | 60 | - | - | dB | |
| Input Resistance | R _{in} | 10 | - | - | Mohm | R=1/Cf equivalent |
| Input Capacitance | C _{in} | - | - | 8.0 | pF | Switched capacitances |
| Input Referred Noise Figure | NF | - | 0.16 | - | $\mu\text{V}/\sqrt{\text{Hz}}$ | 0dBu input, 1KHz, Noise summed from 20Hz to 22KHz |
| Signal-to Noise Ratio and Distortion | SINAD | - | 84 | - | dB | 0dBu input, 1KHz, Noise summed from 20Hz to 22KHz |
| Spurious Free Dynamic Range | SFDR | - | 90 | - | dB | 0dBu input, 1KHz |

1.5.4 Chopper Amplifier Cell

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|---|------------------------|-----|------|------------------------------|---|
| Input Range | V _{ina} V _{dif} fina | See analog input above | | | - | Usable input range will be reduced by the effective gain setting ⁴ |
| Gain | G _{inamp} | 0dB | - | 60dB | - | Software selected |
| Gain Accuracy | GA 0dB | - | - | 5 | % | 0dB setting, 1KHz test signal. |
| | GA 10dB | - | - | 5 | % | 10dB setting, 1KHz test signal. |
| | GA 20dB | - | - | 5 | % | 20dB setting, 1KHz test signal. |
| | GA 30dB | - | - | 5 | % | 30dB setting, 1KHz test signal. |
| | GA 40dB | - | - | 5 | % | 40dB setting, 1KHz test signal. |
| Equivalent Input Offset Voltage | V _{osl} | - | 0.5 | 14 | mV | Intrinsic differential opamp offset |
| Equivalent Input Offset Voltage | V _{osAZ1} | - | 250 | 500 | μV | Differential opamp offset, auto-nulled, NOT chopped. |
| Equivalent Input Offset Voltage | V _{osAZ2} | - | 25 | 100 | μV | Differential opamp offset, auto-nulled and chopped. |
| Offset Voltage Temperature Coefficient | V _{offset} tAZ | - | 15 | TBD | $\mu\text{V}/^\circ\text{C}$ | With auto-null and chopping active. From -40°C to 125°C |
| Input Frequency | F _{ain} | 0 | - | - | KHz | Generally 10x slower than clock, application dependent. |

³ The sample and hold offset varies from phase1 to phase2. This is an average of both values

⁴ To avoid clipping the maximum input range should be divided by the chopper gain

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

| | | | | | | |
|--------------------------------------|-------|----|-----|-----|------------------------|--|
| Power Supply Rejection Ratio | PSRR | - | 62 | - | dB | DC. Amp Gain = 0dB |
| Common Mode Rejection Ratio | CMRR | - | 81 | - | dB | 250kHz clock, 1kHz 0dBu output. See figure 1 |
| Large Signal Harmonic Distortion | Dist | - | -77 | - | dB | Unity-gain. 0dBu input at 1KHz |
| Input Resistance | Rin | 10 | | - | Mohm | |
| Input Capacitance | Cin | - | | 5.0 | pF | |
| Input Referred Noise Floor | IRN | - | 20 | - | nV/ $\sqrt{\text{Hz}}$ | 20dB-gain, 250kHz clock. Idle channel. |
| Input Referred Noise Floor | IRN | - | 4 | - | nV/ $\sqrt{\text{Hz}}$ | 60dB-gain, 250kHz clock. Idle channel. |
| Signal-to Noise and Distortion Ratio | SINAD | - | 76 | - | dB | 20dB-gain, 250kHz clock. 0dBu output at 1KHz. Noise and distortion summed from 22Hz to 22KHz |
| Spurious Free Dynamic Range | SFDR | - | 90 | - | dB | 20dB-gain, 250kHz clock. 0dBu output at 1KHz, See figure 2 |

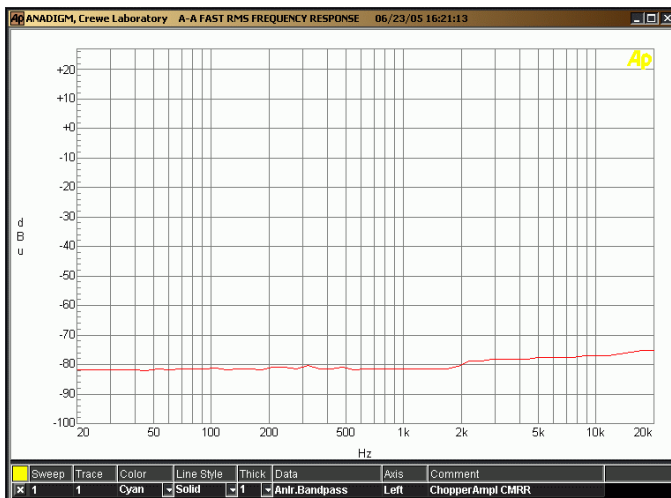


Figure 1: Chopper Amplifier CMRR

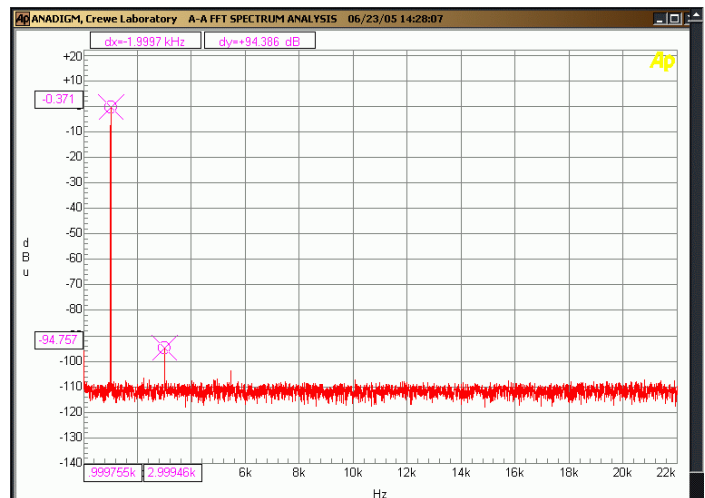


Figure 2: Chopper Amplifier SFDR

1.5.5 Analog Outputs, Loading & Signal Conditioning

(The IO cells use the same circuits as the input cells)

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-------------------------------|----------------------|------------------------|-----------------|------------------------|------|--|
| Min load R | RloadMin | 1 | - | - | KOhm | to VSS |
| Rout | R _{OUTIO} | - | 33 | - | Ohms | For IO opamp to package pins. |
| | R _{OUTCAB} | - | 530 | - | Ohms | For CAB opamp to package pins, (depends on CAB and IO used) Core to outside in bypass I/O. |
| Max load C | Cload Max | - | - | 100 | pF | to VSS. |
| Large signal swing | SIG _{LARGE} | V _{MR} -1.375 | - | V _{MR} +1.375 | V | Differential voltage where -80dB THD is reached for IO cell in SnH mode. 10pF load. |
| Common Mode Voltage | V _{cm} | - | V _{MR} | - | V | Derived from on chip VMR voltage. |
| Common Mode Voltage Deviation | V _{cmDV} | - | - | - | mV | Deviation from supplied VMR. Values are quoted for IO cell or CAB opamp. See other tables. |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.5.6 Clock Dividers

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|----------------------------------|-------------------------|------|------------------------------------|------|--------|--|
| Division ratio Primary divider | DIV _{RATIOPR} | 1 | - | 510 | - | Software controlled. |
| Division ratio secondary divider | DIV _{RATIOSEC} | 1 | - | 510 | - | Software controlled. |
| Division ratio auto zero clock | DIV _{AZ} | 1000 | 162K | 510K | - | Typical is default value. |
| Min clock speed | CLK _{MIN} | - | 1kHz @ 25°C) 10kHz @ 85°C | - | KHz | Each CAM has a different lower clock frequency depending on the parameters set. Excessively low clock frequency will cause signal droop. |
| Max clock speed | CLK _{MAX} | - | - | 8 | MHz | Each CAM has a different upper clock frequency depending on the parameters set. Excessively high clock frequency will cause poor settling and loss of precision. |
| Phase delay | Phase _D | 0 | - | 255 | cycles | Measured in terms of cycles of clock from a primary clock divider. |

1.5.7 PORb & Auto-null

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|-------------------------------|-----------------------|-----|-----|-----|------|---|
| Intrinsic Porb duration | Porb _{DEL} | 0.5 | 1 | 2 | ms | After release of Porb pin. |
| Porb brown out voltage | Porb _{BROWN} | 0.8 | 1.1 | 1.5 | V | Porb will reset device if VDD drops below this level to prevent RAM corruption. |
| Auto-null period ⁵ | AZ _{DEL} | - | 60 | - | ms | Duration for AZ cycle of opamps |

1.5.8 VMR (voltage Mid Rail) and VREF (Reference Voltage) Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|---------------------|------|------|------|------|--|
| VMR Output Voltage | V _{vmr} | 1491 | 1500 | 1509 | mV | At 25°C, VDD=3.3 volts, see figure 3 |
| VREF+ Output Voltage | V _{ref+} | 2469 | 2492 | 2515 | mV | At 25°C, VDD=3.3 volts, see figure 4 |
| VREF- Output Voltage | V _{ref-} | 481 | 501 | 520 | mV | At 25°C, VDD=3.3 volts, see figure 4 |
| Output Voltage Deviation VMR | V _{refout} | - | 0.5 | 1.0 | % | Over process and supply voltage corners |
| Output Voltage Deviation VREF+, VREF- | V _{refout} | - | 1.0 | 2.0 | % | Over process and supply voltage corners |
| Voltage Temperature Coefficient VREF+, VMR, VREF- | V _{reftc} | - | - | - | - | See typical graphical data below -40°C to 125°C |
| Power Supply Rejection Ratio, VMR | PSSR | TBD | - | - | dB | DC |
| Power Supply Rejection Ratio Vref+ and Vref- | PSSR | TBD | - | - | dB | DC |
| Start Up Time | T _{start} | - | - | 1 | ms | Assuming recommended capacitors, 25°C, VDD=3.3 volts |

⁵ see application note AN231002 "Auto-nulling within the AN231E04"

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

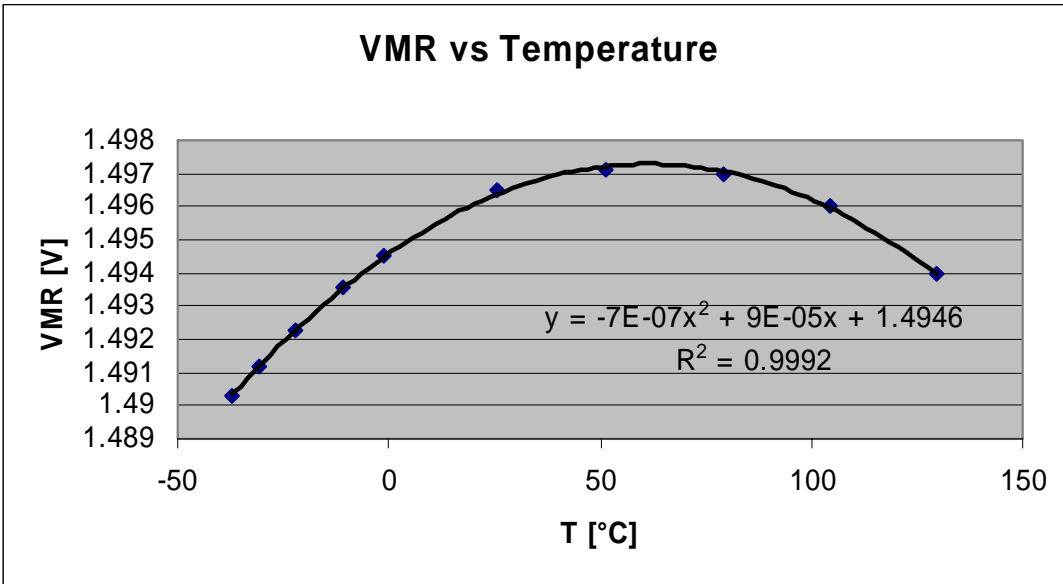


Figure 3: GainHold CMRR

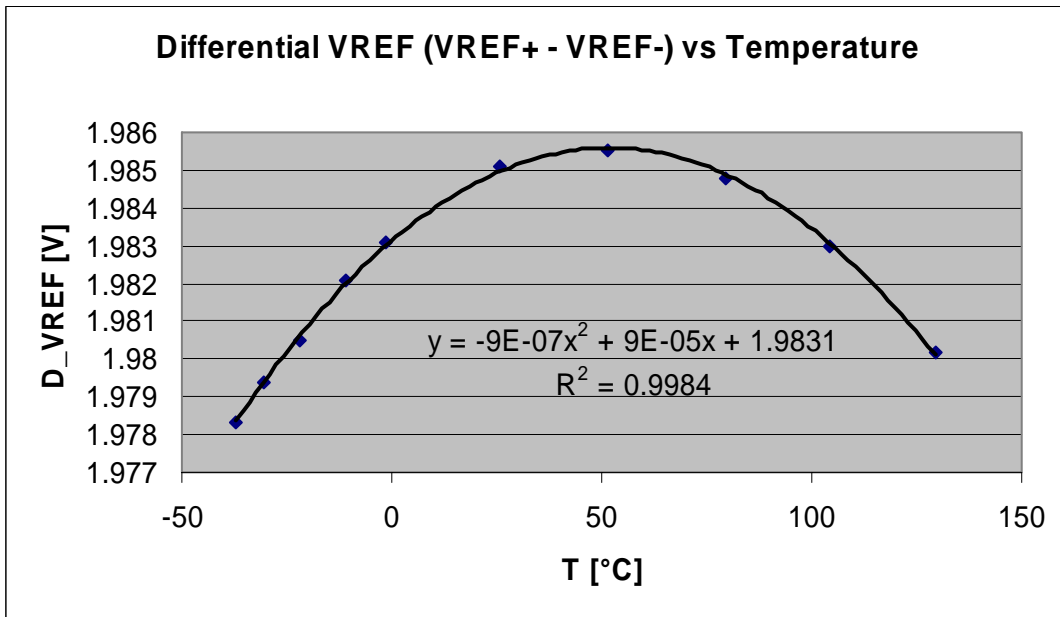


Figure 4: GainHold CMRR

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.5.9 CAB (Configurable Analog Block) Differential Operational Amplifier

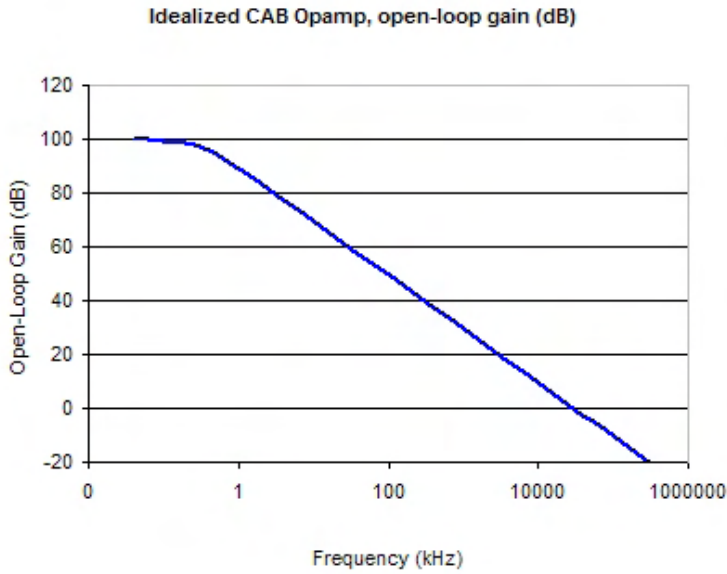
| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------|------|-----------|--------|--------|---|
| Output Range | Vinouta | 0.05 | - | 2.95 | V | GainInv 1kHz THD > -80dB. Common mode voltage = 1.5 V |
| Differential Output voltage | Vdiffioa | - | - | +/-2.9 | V | Limited by signal clipping. GainInv THD exceeds -80dB Common mode voltage = 1.5 V |
| Common Mode Input Voltage Range ⁶ | Vcm | 1.4 | 1.5 | 1.6 | V | VMR set to 1.5V ⁶ |
| Common Mode Voltage Deviation | VcmD | 0 | - | +/-50 | mV | Deviation is caused by opamp common mode offset voltages. |
| Equivalent Input Voltage Offset. | Voffsetl | - | 3 | 18 | mV | Intrinsic offset voltage. |
| Equivalent Input Voltage Offset. | VosAZ | - | 250 | 1000 | uV | Auto-null offset voltage. |
| Equivalent Input Voltage Offset. | VosAZchpl | - | 75 | 250 | uV | Auto-null & chopped offset |
| Offset Voltage Temperature Coefficient | VosAZ | - | see graph | 19 | μV/°C | Auto-null mode, from -40°C to 125°C. |
| Offset Voltage Temperature Coefficient | VosAZChp | - | - | < 0.1 | μV/°C | Auto-null and chopped mode, from -40°C to 125°C. |
| Power Supply Rejection Ratio | PSSR | - | 60 | - | dB | DC. Variation between CAMs is expected because of variations in architecture. |
| Common Mode Rejection Ratio | CMRR | - | 54 | - | dB | GainInv CAM, clock = 1MHz, gain = 1. -20dBu input at 1kHz See figure 6 |
| Differential Slew Rate, Internal | Slewl | - | 35 | - | V/μsec | Applicable when the OpAmp load is internal to the dpASP |
| Differential Slew Rate, External | SlewE | - | 30 | - | V/μsec | Applicable when the OpAmp driving signal out of the dpASP package. Routing resistance causes degradation from Slew |
| Unity Gain Bandwidth, Full Power Mode. | UGB | - | 18 | - | MHz | Applicable when sourcing and loading the OpAmp with a load internal to the dpASP. CAMs limit signal frequency to a lower value. See figure 5 |
| Input Impedance, Internal | Rin | 10 | - | - | Mohm | |
| Output Impedance, Internal | Rout | - | - | - | Ohms | The OpAmp output is designed to drive all internal nodes, these are dominantly capacitive loads |
| Output Impedance, External | Rout | - | 600 | - | Ohms | Output to a dpASP output pin (output cell bypass mode). This variable is influenced by CAB capacitor size, CAB clock frequency and CAB architecture |
| Output Load, External ⁷ | Rload | 1 | - | - | Kohm | |
| Output Load, External | Cload | - | - | 100 | pF | |
| Input Referred Noise Floor ⁸ | IRN | - | 300 | - | nV/√Hz | Unity-gain GainHold CAM, 1MHz clocking. Idle channel. |
| Signal-To Noise and Distortion Ratio ⁸ | SINAD | - | 86 | - | dB | Unity-gain GainHold CAM, 1MHz clocking. 0dBu input at 1KHz, Noise and distortion summed from 22Hz to 22KHz |
| Spurious Free Dynamic Range ⁸ | SFDR | - | 100 | - | dB | Unity-gain GainHold CAM and SnH output cell. 1MHz clocking. 0dBu input at 1KHz. See figure 7 |

⁶ The is for the OpAmp. The use of virtual earth architectures means the CAMs can exceed these values

⁷ The maximum load for an analog output is 100 pF || 1 K Ohms. This load is with respect to AVSS. Using the DPASP with CAB Opamps driving directly off chip is not recommended. Full characterization of the performance of each application circuit by the designer is necessary

⁸ Using an I/O Cell Sample & Hold is used to prevent the variable routing resistance affecting the harmonic response

AN231E04 Datasheet – Dynamically Reconfigurable dpASP



The idealized open loop gain plot is provided for information only. This information is associated with the dpASP in full power mode of operation. The dpASP operational amplifier open loop gain cannot be observed nor used when associated with external connections to the device. Internal reprogrammable routing impedances and switched capacitor circuit architectures using this operational amplifier limit the effective usable bandwidth.

Figure 5: CAB Opamp Open Loop Gain Response

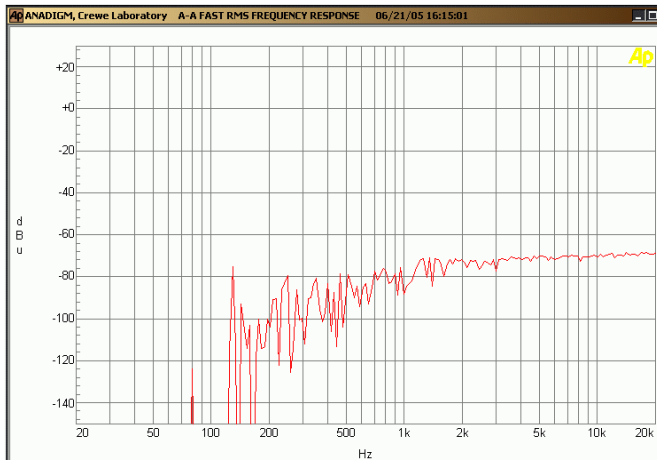


Figure 6: GainHold CMRR

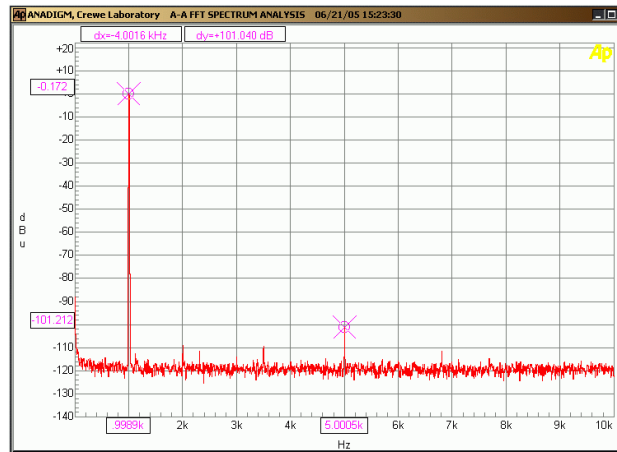


Figure 7: GainHold SFDR

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.5.10 CAB (Configurable Analog Block) Differential Comparator

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|--|-----------------------|---------------------|----------------------|----------------------|-------|--|
| Input Range, External or Internal | V _{ina} | 0.0 | - | VDD | V | Will operate correctly. |
| Differential Input, Internal | V _{diffina} | - | - | - | V | Set by internal signal clipping based on common mode voltage. |
| Differential Output bypass (bypass with core comparator is not a recommended operating mode) | V _{outdiffL} | 0.163 | - | 3.138 | V | 3.3VDD. In digital output mode, 10KOhms connected between output pins. Varies with internal routing. Pad buffers are recommended in this mode. |
| | V _{outdiffA} | 0.592 | - | 2.396 | | In analogue V _{ref} level output mode. 10KOhms connected between output pins. Will vary with internal routing. |
| Input Voltage Offset | V _{offcomp} | - | 0.78 | 1.22 | mV | Zero hysteresis |
| Offset Voltage Temperature Coefficient | V _{offsettc} | - | 1 | - | μV/°C | from -40°C to 125°C, Zero hysteresis |
| Setup Time, Internal | T _{setint} | - | - | 125 | nsec | |
| Setup Time, External | T _{setext} | - | - | 500 | nsec | |
| Delay Time | T _{delay} | ½T _d +25 | - | 1½T _d +25 | nsec | T _d = 1/F _c F _c = master clock frequency |
| Output Load | R _{load} | 10 | - | - | Kohm | Applies if comparator drive off chip with output cell in bypass mode |
| Output Load | C _{load} | - | - | 50 | pF | Applies if comparator drive off chip with output cell in bypass mode |
| Differential Hysteresis | Hysta0 | - | V _{offcomp} | - | mV | Hysteresis setting OFF |
| Differential Hysteresis | Hysta1 | - | 10 | - | mV | Hysteresis setting ON |
| Hysteresis Temperature Coefficient | Hysttc1 | - | 10 | - | μV/°C | Hysteresis setting = ON |

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

1.5.11 ESD Characteristics

| Pin Type | Human Body Model | Machine Model | Charged Device Model |
|-----------------------|------------------|---------------|----------------------|
| Digital Inputs | 4000V | 250V | 4kV |
| Digital Outputs | 4000V | 250V | 4kV |
| Digital Bidirectional | 4000V | 250V | 4kV |
| Digital Open Drain | 4000V | 250V | 4kV |
| Analog Inputs | 2000V | 200V | 4kV |
| Analog Outputs | 1500V | 100V | 4kV |
| Reference Voltages | 1500V | 100V | 4kV |

The AN231E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN231E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

1.5.12 Power Consumption – Various Modes

| Parameter | Symbol | Min | Typ | Max | Unit | Comment |
|---|-----------------|-----|----------------|--------------|-------|---|
| Deep sleep mode ^{1a} | I _{dd} | - | 0.004 | - | mA | VDD=3.3 volts, T _j =25°C |
| Stand Standby mode ^{1b} | I _{dd} | - | 0.3 | - | mA | VDD=3.3 volts, T _j =25°C |
| Small circuit mode ^{1c} | I _{dd} | - | 15 | - | mA | VDD=3.3 volts, T _j =25°C |
| Nominal circuit mode ^{1d} | I _{dd} | - | 42 | - | mA | VDD=3.3 volts, T _j =25°C |
| HighPower ^{1e} | I _{dd} | - | 61 67 73 | - 75 - | mA | VDD=3.0 volts, T _j =85°C VDD=3.3 volts, T _j =25°C VDD=3.6 volts, T _j = -40°C |
| Temperature Coefficient for High power. | - | - | -2 | -10 | μA/°C | |

1a. External clock stopped, all analog function disabled, memory active.

1b. External clock at 16MHz on ACLK, all analog functions disabled, memory active.

1c. dpASP active elements – Gain hold CAM, One IO in SnH and both clocked at 1MHz, One IO bypass, all references on.

1d. dpASP active elements - Four gain hold CAMs (4 CAB opamps), one CAB comparator, one CAB multiplier (1 CAB opamp, 1 CAB comparator, 1 CAB SAR ADC), Two IO in SnH, One IO in bypass, one simple IO in digital mode. 4 MHz clock for all, all references on.

1e. dpASP active elements - Seven gain hold CAMs (seven CAB opamps), 1 arbitrary waveform generator (one CAB opamp, LUT, counter) 4 CAB comparators, 4 IO Sample and hold, references on, 4 MHz clock for all where possible, all references on.

AN231E04 Datasheet – Dynamically Reconfigurable dpASP

PINOUT

| Pin No. | Pin Name | Pin Type | Comments |
|---------|------------------|------------------|--|
| 1 | I1P | +ve Input | Type1 Input/Output cell. (IO Cell 1) Analog or digital input and output pins |
| 2 | I1N | -ve Input | |
| 3 | O1N | -ve Output | |
| 4 | O1P | +ve Output | |
| 5 | AVSS | Ground Supply | Analog ground, 0 Volts |
| 6 | O2P | +ve Input | Type1 Input/Output cell. (IO cell 2) Analog or digital input and output pins |
| 7 | O2N | -ve Input | |
| 8 | I2N | -ve Output | |
| 9 | I2P | +ve Output | |
| 10 | AVDD | Positive Supply | Analog power 3.3 Volts |
| 11 | I3P | +ve Input | Type1a Input/Output cell. (IO cell 3) Analog or digital input and output pins |
| 12 | I3N | -ve Input | |
| 13 | O3N | -ve Output | |
| 14 | O3P | +ve Output | |
| 15 | IO5P | +ve Input/Output | Type 2 Input/Output cell. (IO cell 5) |
| 16 | IO5N | -ve Input/Output | |
| 17 | IO6P | +ve Input/Output | Type 2 Input/Output cell. (IO cell 6) |
| 18 | IO6N | -ve Input/Output | |
| 19 | IO7P | +ve Input/Output | Type 2a Input/Output cell. (IO cell 7) |
| 20 | IO7N | -ve Input/Output | |
| 21 | O4P | +ve Input | Type1a Input/Output cell. (IO cell 3) Analog or digital input and output pins |
| 22 | O4N | -ve Input | |
| 23 | I4N | -ve Output | |
| 24 | I4P | +ve Output | |
| 25 | BVDD | Positive Supply | Voltage reference power 3.3 Volts |
| 26 | VREFP | Reference load | Reference Voltage Noise suppression. Connected a 100nF capacitor from each pin to BVSS. The capacitive reservoir is used to sink and source peak current, thus reducing noise and maintaining stable reference voltages. |
| 27 | VMR | Reference load | |
| 28 | VREFN | Reference load | |
| 29 | BVSS | Ground Supply | |
| 30 | CFGFLGb | Digital Output | Voltage reference ground 0 Volts Config status pin. Open Drain Output with optional internal Pull-up resistor. The output voltage is also sensed by internal circuitry, See figure XX for schematic. |
| 31 | CS2b | Digital input | Chip select pin |
| 32 | CS1b | Digital input | Device select |
| 33 | SCLK | Digital input | CMOS, configuration logic strobe clock. |
| 34 | ACLK | Digital input | CMOS, Analog clock input |
| 35 | MODE | Digital input | Connect to VSS (ACLK and SCLK sourced externally). Connect to VDD (ACLK sourced externally, MEMCLK & SO generated internally). |
| 36 | DVDD | Positive Supply | Digital power 3.3 Volts |
| 37 | DVSS | Ground Supply | Digital ground 0.0 Volts |
| 38 | SI | Digital input | CMOS Serial data input. |
| 39 | LCCb/ DOUT1 | Digital output | CMOS. Default function, Indicates Local Configuration Complete. Optional function (Single dpASP designs only), pin can be configured as user assignable signal path digital output under software control. |
| 40 | ERRb | Digital output | Error indication. Open Drain, External Pull-up resistor must be used (10KOhms) See fig XXa |
| 41 | ACTIVATE | Digital Output | Indicates Device activation. Open Drain Output with optional internal Pull-up resistor. The output voltage is also sensed by internal circuitry, See figure XX for schematic. |
| 42 | MEMCLK/ DOUT2 | Digital Output | Outputs MEMCLK clock when MODE pin = VSS. Caution - Do not load this pin during reset (NOT to be pulled low externally) |
| 43 | SO | Digital Output | Serial Out, ONLY used as an output for SPI-PROM setup bytes during configuration. |
| 44 | RESETb | Digital Input | Connected to VSS to reset the dpASP. If held low the dpASP will remain in reset (2msec delay internal set-up time follows release of RESETb (when this pin is pulled high)) |

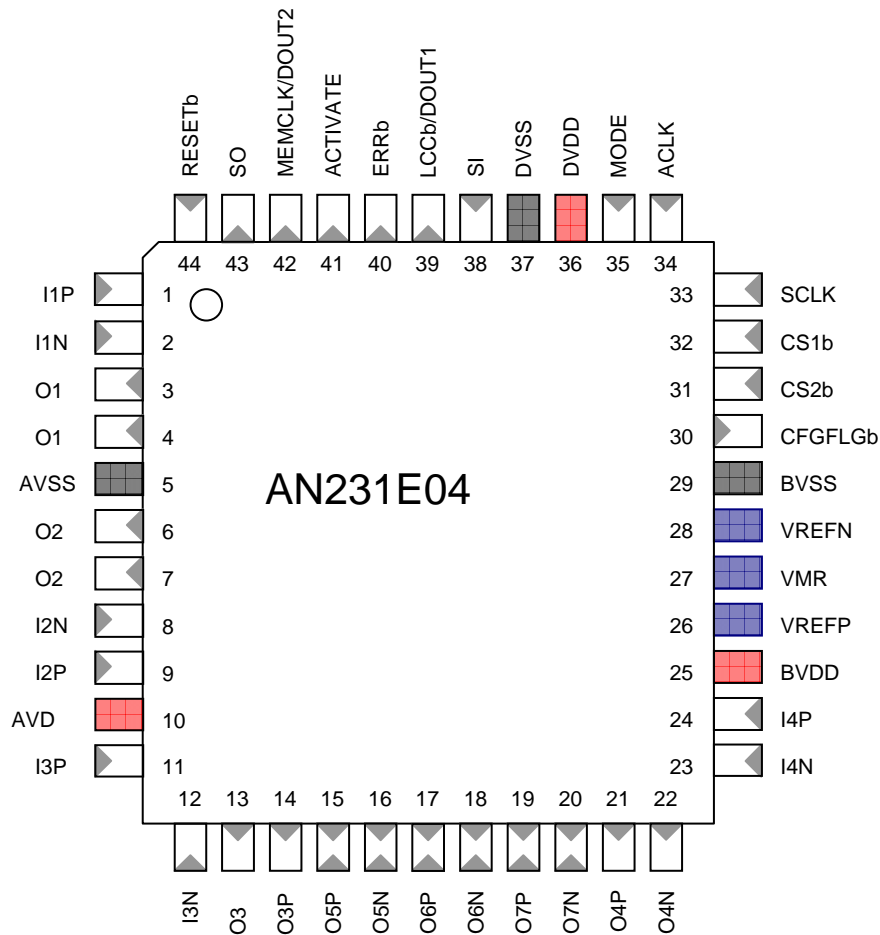
AN231E04 Datasheet – Dynamically Reconfigurable dpASP

MECHANICAL AND HANDLING

The AN231E04 comes in the industry standard 44 lead QFN package.

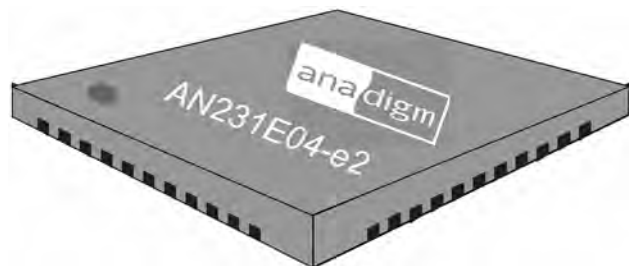
Dry pack handling is recommended. The package is qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.

The package is compliant with RoHS and is Lead-free. Lead finish is Matt tin (Sn-Cu).



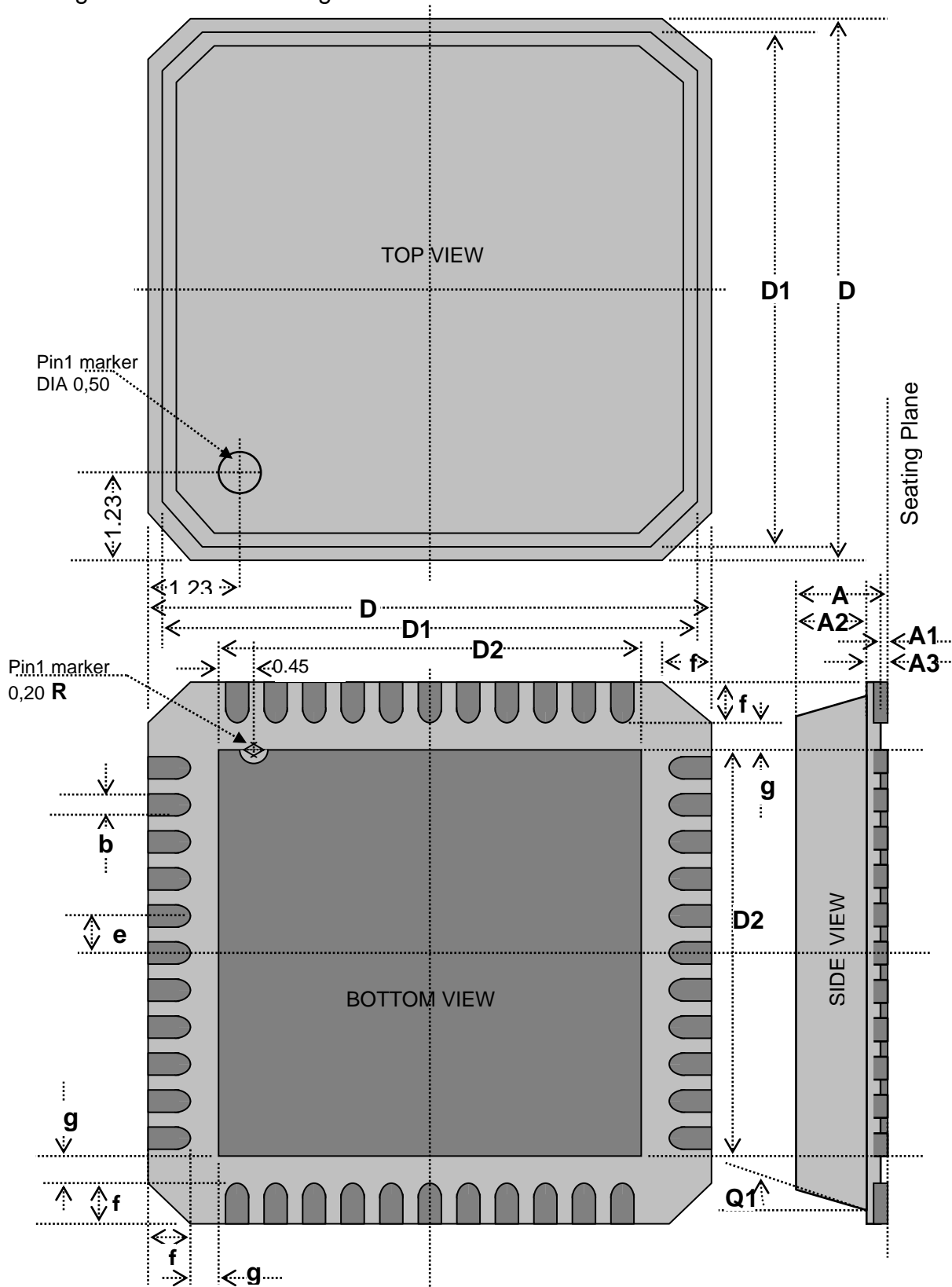
All dimension are in mm

| Symbol | Min | Nom | Max |
|--------|------|------------|------|
| A | - | - | 0.90 |
| A1 | 0.00 | 0.01 | 0.05 |
| A2 | - | 0.65 | 0.70 |
| A3 | - | 0.20 | - |
| D | - | 7.00 | - |
| D1 | - | 6.75 | - |
| D2 | 5.30 | 5.50 | 5.70 |
| b | 0.20 | 0.25 | 0.32 |
| e | - | 0.50 | - |
| f | 0.26 | 0.42 | 0.60 |
| g | 0.2 | - | - |
| Q1 | 0.0° | (Ang.deg.) | 12° |
| R | 0.09 | - | - |



AN231E04 Datasheet – Dynamically Reconfigurable dpASP

QFN Package mechanical drawing



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