# ROBUST ELECTRICAL SURGE IMMUNITY FOR POE PDS THROUGH INTEGRATED PROTECTION

1. Introduction

The Si3400 and Si3401 Power over Ethernet (PoE) powered device (PD) controllers are designed in an efficient Silicon on Insulator (SOI) process technology, which enables the integration of a robust surge protection function. Competitive PoE PD devices require external transient voltage suppressors (TVS), such as an SMAJ58A, to provide surge protection. However, due to their inherently wider range of clamping voltage specifications, external TVS-based protectors typically necessitate the use of 100 V processes for the PD controller device. This note discusses some of the detailed considerations regarding the Si3400's proprietary surge protection circuitry that enable the Si3400 and Si3401 devices to yield robust and standards-compliant electrical surge immunity when used in Power over Ethernet powered device applications.

2. Traditional PD Surge Protection Considerations

As will be discussed later, surge currents of up to 5 A must be tolerated in PoE applications. The surge protector most often used with PD controllers is an external SMAJ58A TVS diode (D1 in Figure 1).
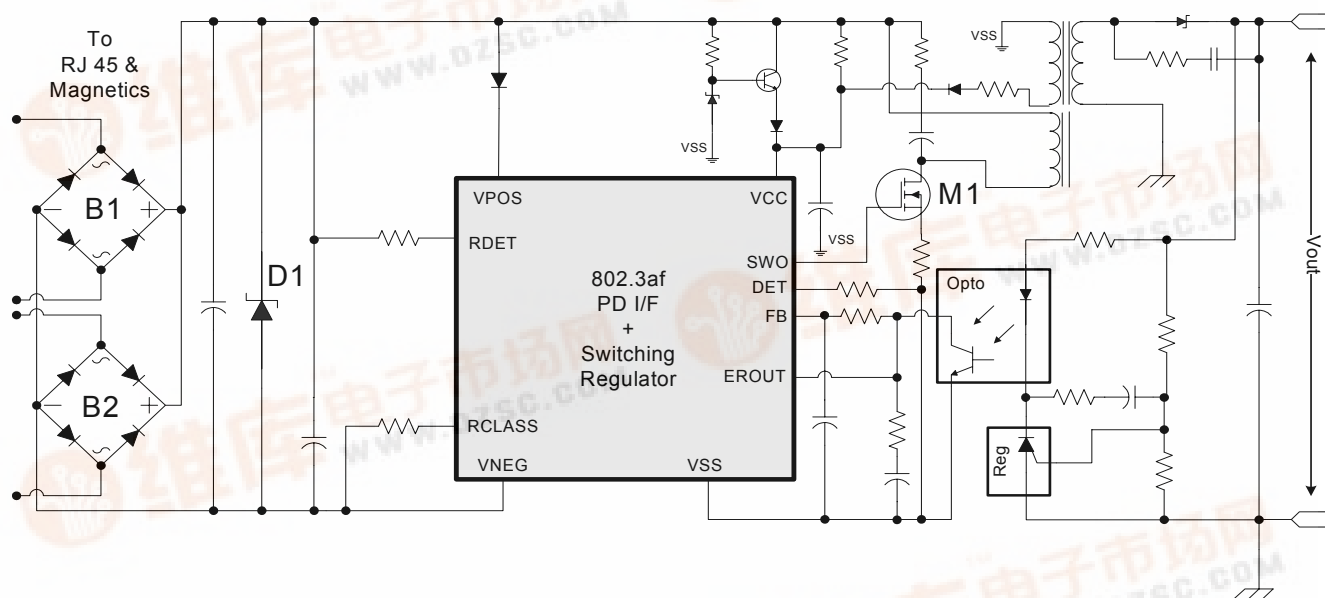
Figure 1. Traditional PoE PD Interface and Switching Regulator (without High Voltage Device Integration)

For example, a standard SMAJ58A TVS from Diodes Incorporated has a maximum operating voltage of 58 V, 25 °C ratings of between 64.4 and 71.2 V at 1 mA, and a clamping voltage under 93.6 V at 4.3 A.

While it is possible to sort individual devices for tighter clamp voltage ratings, the typical maximum clamping voltage (including temperature variations) when using this type of protector is close to 100 V. Consequently, most PoE PD controllers are implemented in processes providing a 100 V breakdown voltage.

3. Detailed Description of Si3400 Protection

Si3400 and Si3401 protection consists of a stack of ten, high-current 6.2 V Zener diodes. These lower-voltage Zener diodes have a lower temperature and process variation than a higher voltage Zener clamp, such as an SMAJ58A. Consequently, the range of initial breakdown for the complete stack is much tighter: typically <1 V variation at room temperature (as compared to 6.8 V for the SMAJ58A) and <4 V variation over –40 to +85 °C. Due to the incremental resistance of the Zener diode stack, the voltage at 0.5 A current typically increases to 73 V, and the voltage at 5 A current is less than 79 V for the Si3400's on-chip protector. As a result, the Si3400's maximum clamping voltage of 79 V is considerably lower than the 90 to 100 V range of a typical SMAJ58A TVS protector.

Because the Zener stack is part of the Si3400's internal circuitry, it becomes straightforward to detect a surge condition internal to the IC. To provide additional protection against high current and longer-duration transients, the switcher is shut down, and the hot swap switch is turned on with the current limit disabled when current starts to flow in the Zener diode stack. Disabling the switcher section during a transient event prevents damage to the switching FET. Turning on the hot swap switch allows steering of some of the surge current to the switching rectifier input filter capacitor, which reduces the current in the Zener stack and allows for very high current spike tolerance without damage.

4. Surge Test Considerations for the Si3400 and Si3401

There are five basic surge conditions that must be accounted for when evaluating surge protection as detailed below. The Si3400's performance has been tested in all of these conditions with excellent results.

4.1. Standards-Based Surge Testing

IEEE STD™ 802.3-2005 specifies a 1000 V surge tolerance with a 300 nsec virtual front and 50 µsec half value (as defined in IEC 60060) with an impedance applied via a 402 Ω resistor to each wire in the wire pair. While the return path is not specified, a worst case interpretation is that the return pair is grounded so that 2.5 A flows in each of the wires to the PD, resulting in a 5 A surge to the PD.

The 5 A surge will charge the typical 0.1 µF PD input capacitor to 50 V in 1 µsec. After this time, the Zener diode clamps, and once the hot swap switch is turned on, some of this surge is steered to the switcher input filter capacitor as well.

The Si3400's performance has been tested with this worst-case interpretation surge condition. All devices tested survived the standard 1000 V condition for 10 repetitions with substantial margin.

4.2. ESD

An Si3400 isolated EVB (Revision 1.2) was tested for ESD immunity. The test method reference is IEC 61000-4-2. A Schaffner model NSG 435 ESD gun was used to generate the ESD pulses.

For this test, the connector shield was tied to the Vneg heat sink/isolated ground plane of the Si3400 ISO EVB, and the ESD pulses were applied to the shield with the output of the EVB grounded. The ESD discharge path in this case would be through the 1000 pF high-voltage capacitors connected from the output side ground plane to Vpos and Vneg. An attempt was made to discharge to the RJ-45 pins, but the discharge was always to the shield indicating that surging the shield is an appropriate test method.

The ESD gun was used in contact mode and the ESD pulses were applied in both polarities in 500 V increments up to 9 kV. Above 9 kV, contact mode is not supported with the ESD gun; so, air discharge mode was used, again increasing the voltage in 500 V steps up to the maximum available voltage of 16.5 kV in both polarities. After each voltage increment, the board was tested and was not damaged. The 15 kV test was repeated 10 times for each polarity, again with no damage observed after each test.

4.3. Telephony Voltages

IEEE STD™ 802.3-2005 also specifies that the application of telephony ringing of up to 56 VDC plus ac with a peak of up to 175 V applied through 400 Ω source shall not result in a safety hazard.

Continuous application of such a large signal will eventually result in a device failure due to the high power present at the clamp. Si3400 devices tested in this condition survive over one second and then eventually fail in a shorted condition, which does not present a safety hazard. However, according to Telecordia GR1089 October 2002 7.5.2 and Figure 7-6, the approximately 300 mA peak current that results from this test requires that a "ring trip" be detected and the ringing be removed within 0.1 seconds. This means that when exposed to even a very severe fault condition of ringing directly applied, the Si3400 PD will not be damaged.

4.4. Cable Discharge

It is possible for the conductors in an Ethernet cable to develop a static charge, for example, by being dragged across carpeting before being plugged in. While there is no standards-based test for this, a uniform test procedure has been described[1].

A Si3400 PD evaluation board was tested using this procedure with the test diagram shown in Figure 2.
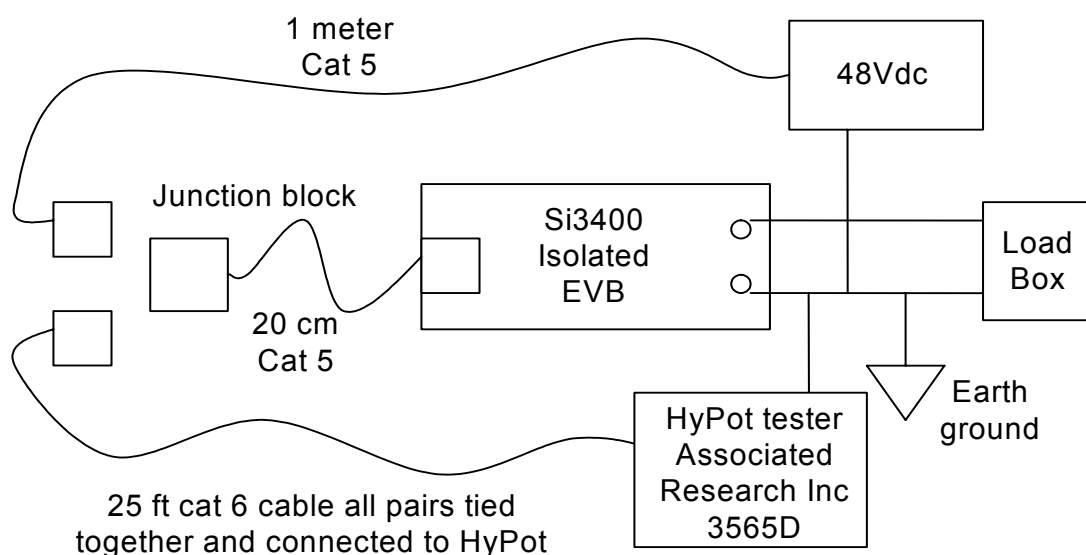

Figure 2. Test Diagram

Test procedure:

1. Verify board functionality with 48 VDC Supply.
2. Unplug 1 m cable from junction block.
3. Charge 25 ft cable with HyPot tester at 1000 V.
4. Plug 25 ft cable into junction block with HyPot tester connected.
5. Unplug 25 ft cable while HyPot tester is still putting out voltage.
6. Plug in 48 V supply through 1 m cable.
7. Verify board functionality.
8. Repeat steps 2-7 testing twice at 1000 V and twice at each voltage above 1000 V in 500 V increments.

The test board survived up to 3500 V. This board was designed for 2500 V isolation. Testing at higher voltage would require a board design that is capable of withstanding higher voltage or that the Hypot source be removed, assuming that the cable maintains its charge prior to being plugged in.

This puts the performance of the Si3400 well into the "excellent" CDE category.

4.5. Hot Insertion

Due to the detection process in IEEE STD™ 802.3-2005, which prescribes the use of low voltages and a 5 mA current limit, hot insertion is not a common problem. However, it is common to have an auxiliary supply as shown below:
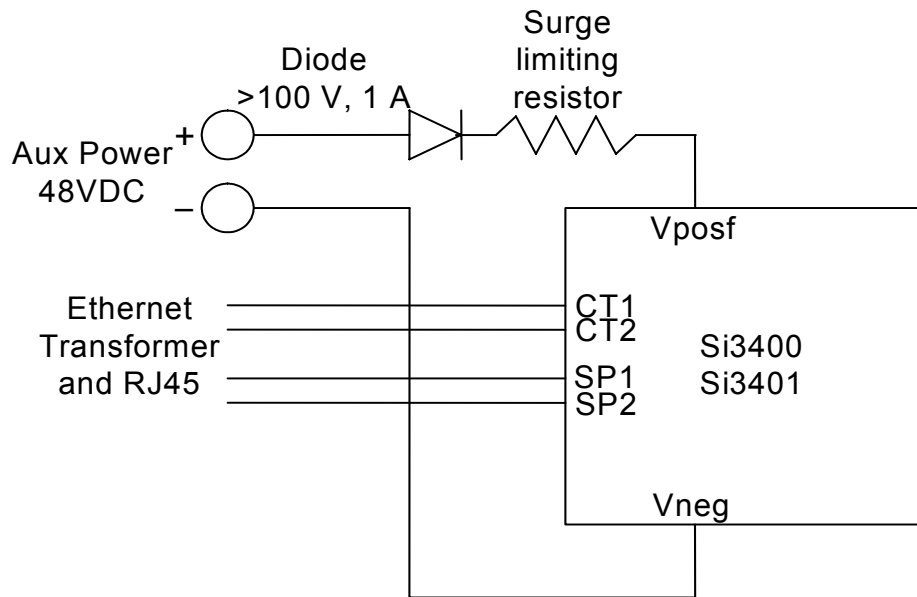
Figure 3. Auxiliary Supply

If the auxiliary supply has a large output capacitor, hot insertion damage may result. This arises from the typical PD 0.1 μF input capacitor being quickly charged, with voltage overshoot resulting from the lead inductance to the auxiliary power source. While this overshoot will be clamped by the Si3400's protector, for low values of lead inductance, the peak current can exceed 10 A. A surge limiting resistor will reduce the overshoot and peak current. A 3 Ω resistor has been found to be an effective value for the surge-limiting resistor in typical applications. Since this resistor does carry up to the maximum 350 mA of dc PD input current, a 0.5 W resistor is recommended.

5. Conclusions

The proprietary protector integrated within the Si3400 and Si3401 PD controllers provides protection against all required surge conditions and results in a significant BOM savings over the typical external surge protector (SMAJ58A).

The test results are summarized in Table 1.

Table 1. Test Results

Specification	Surge Type	Si3400, Si3401 Test Results
IEEE 802.3af (IEC 60060)	Transient surge	> 1 kV @ 5 A (10 repetitions)
ESD (IEC 61000-4-2)	ESD events	16.5 kV (both polarities) 15 kV (10 repetitions)
CDE (Cisco specification)[1]	Cable Discharge Event	> 3.5 kV multiple repetitions ("excellent" category)
IEEE 802.3af (telephony voltage compatibility)	Telephony ringing voltage immunity	>175 V for 1 second
AUX supply hot insertion	Current surge	3 Ω recommended for good margin

The integrated surge protection allows detection of the surge and subsequent shutdown of the switcher as well as steering of surge currents through the on-chip protector for even more robust performance. The tighter distribution of the clamping voltage of the integrated surge protector allows the use of an efficient SOI process, which yields optimal cost and performance compared to solutions requiring an external surge protector.

6. References

[1] J. Deatherage and D. Jones, "Multiple Factors Trigger Cable Discharge Events in Ethernet LANs", Electronic Design Dec. 4, 2000.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated Table 1 on page 5.
  - Added reference to IEC 61000-4-2 specification for ESD test.

NOTES:

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