



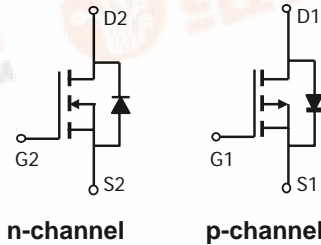
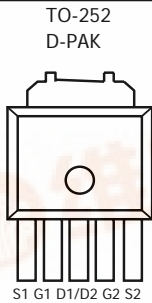
## AOD603 Complementary Enhancement Mode Field Effect Transistor

### General Description

The AOD603 uses advanced trench technology MOSFETs to provide excellent  $R_{DS(ON)}$  and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. *Standard Product AOD603 is Pb-free (meets ROHS & Sony 259 specifications). AOD603L is a Green Product ordering option. AOD603 and AOD603L are electrically identical.*

### Features

n-channel	p-channel
$V_{DS}$ (V) = 60V	-60V
$I_D$ = 12A ( $V_{GS}=10V$ )	-12A ( $V_{GS}=-10V$ )
$R_{DS(ON)}$	$R_{DS(ON)}$
< 60m $\Omega$ ( $V_{GS}=10V$ )	< 115m $\Omega$ ( $V_{GS} = -10V$ )
< 85m $\Omega$ ( $V_{GS}=4.5V$ )	< 150m $\Omega$ ( $V_{GS} = -4.5V$ )



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	$V_{DS}$	60	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current <sup>G</sup>	$I_D$	$T_C=25^\circ\text{C}$	12	A
		$T_C=100^\circ\text{C}$	12	
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	30	-30	
Avalanche Current <sup>C</sup>	$I_{AR}$	12	-12	A
Repetitive avalanche energy $L=0.1\text{mH}$ <sup>C</sup>	$E_{AR}$	23	23	mJ
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	20	W
		$T_C=100^\circ\text{C}$	10	
Power Dissipation <sup>A</sup>	$P_{DSM}$	$T_A=25^\circ\text{C}$	2	W
		$T_A=70^\circ\text{C}$	1.3	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 175	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	n-ch	17.4	30	$^\circ\text{C/W}$
		p-ch	50	60	$^\circ\text{C/W}$
Maximum Junction-to-Case <sup>B</sup>	$R_{\theta JC}$	n-ch	4	7.5	$^\circ\text{C/W}$
		p-ch	16.7	25	$^\circ\text{C/W}$
Maximum Junction-to-Ambient <sup>A</sup>	$R_{\theta JA}$	n-ch	40	50	$^\circ\text{C/W}$
		p-ch	2.5	4	$^\circ\text{C/W}$



N-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=10\text{mA}$ , $V_{GS}=0\text{V}$	60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=48\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=250\mu\text{A}$	1	2.4	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$ , $V_{DS}=5\text{V}$	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$ , $I_D=12\text{A}$		47	60	m $\Omega$
		$T_J=125^\circ\text{C}$		85		
		$V_{GS}=4.5\text{V}$ , $I_D=6\text{A}$		67	85	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=5\text{V}$ , $I_D=12\text{A}$		14		S
$V_{SD}$	Diode Forward Voltage	$I_S=1\text{A}$ , $V_{GS}=0\text{V}$		0.74	1	V
$I_S$	Maximum Body-Diode Continuous Current				12	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=30\text{V}$ , $f=1\text{MHz}$		450	540	pF
$C_{oss}$	Output Capacitance			61		pF
$C_{rss}$	Reverse Transfer Capacitance			27		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		1.35	2	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$ , $V_{DS}=30\text{V}$ , $I_D=12\text{A}$		7.5	10	nC
$Q_g(4.5\text{V})$	Total Gate Charge			3.8	5	nC
$Q_{gs}$	Gate Source Charge			1.2		nC
$Q_{gd}$	Gate Drain Charge			1.9		nC
$t_{D(on)}$	Turn-On Delay Time	$V_{GS}=10\text{V}$ , $V_{DS}=30\text{V}$ , $R_L=2.5\Omega$ , $R_{GEN}=3\Omega$		4.2		ns
$t_r$	Turn-On Rise Time			3.4		ns
$t_{D(off)}$	Turn-Off Delay Time			16		ns
$t_f$	Turn-Off Fall Time			2		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=12\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		27.6	35	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=12\text{A}$ , $dI/dt=100\text{A}/\mu\text{s}$		30		nC

A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation  $P_{DSM}$  is based on  $R_{\theta JA}$  and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation  $P_D$  is based on  $T_{J(MAX)}=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=175^\circ\text{C}$ .

D: The  $R_{\theta JA}$  is the sum of the thermal impedance from junction to case  $R_{\theta JC}$  and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\mu\text{s}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^\circ\text{C}$ .

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

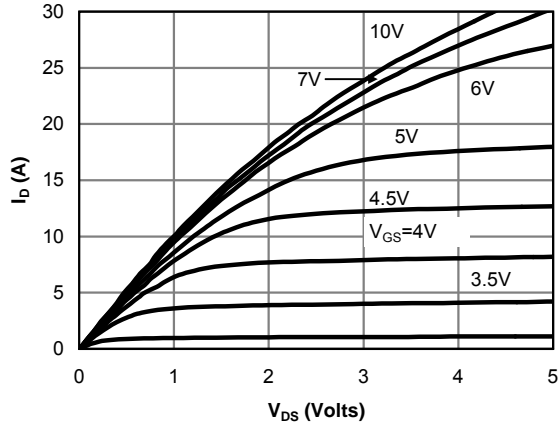


Fig 1: On-Region Characteristics

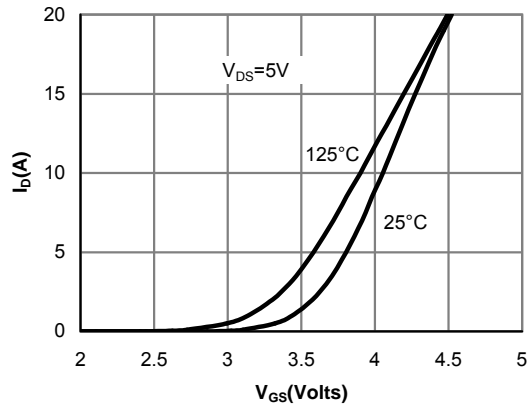


Figure 2: Transfer Characteristics

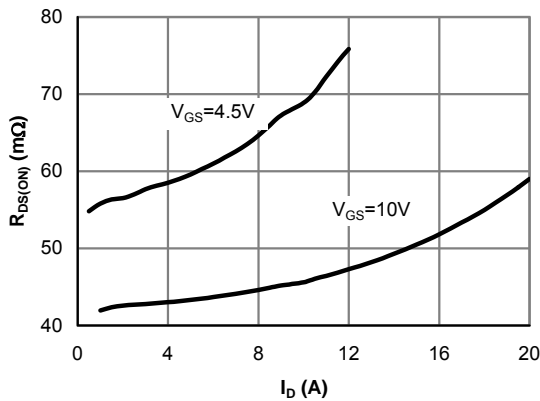


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

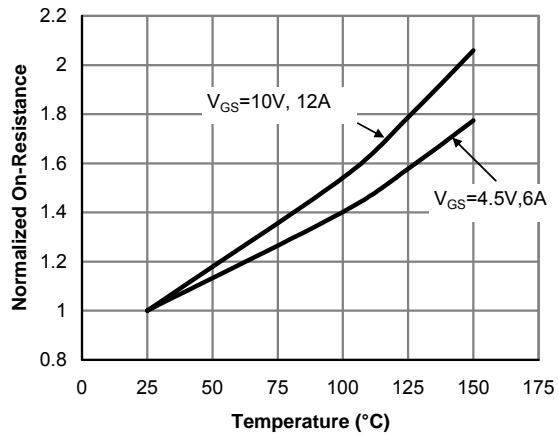


Figure 4: On-Resistance vs. Junction Temperature

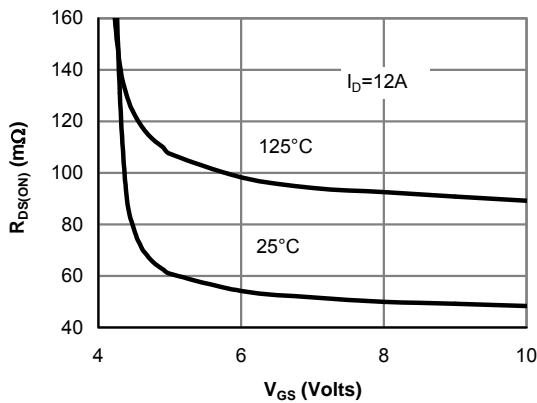


Figure 5: On-Resistance vs. Gate-Source Voltage

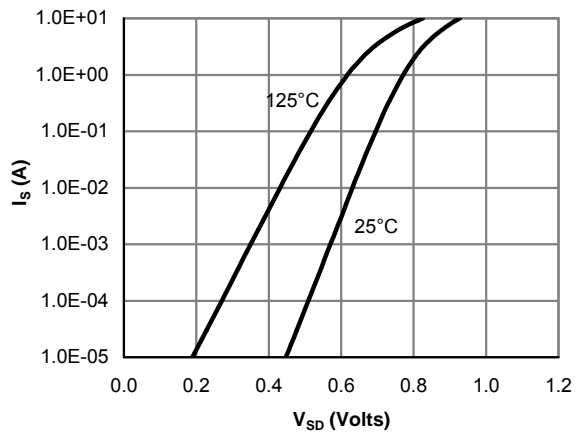


Figure 6: Body-Diode Characteristics

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

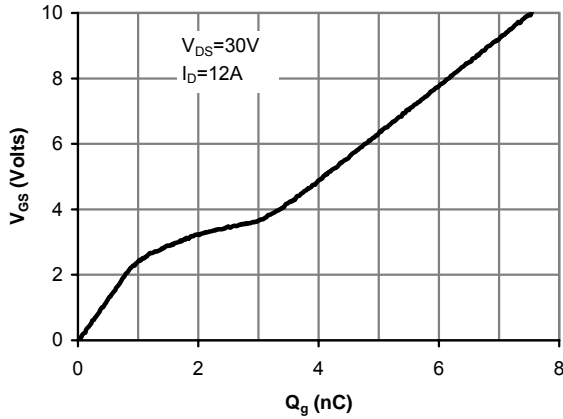


Figure 7: Gate-Charge Characteristics

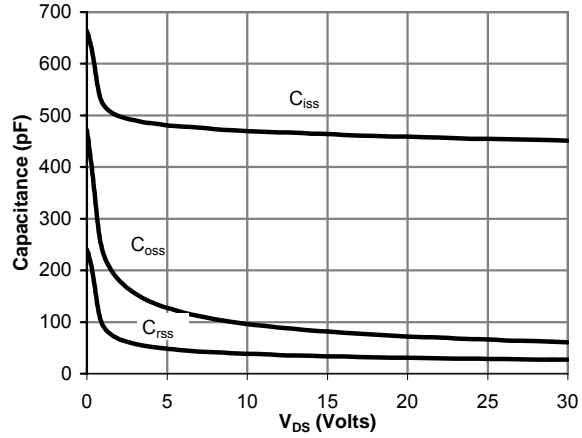


Figure 8: Capacitance Characteristics

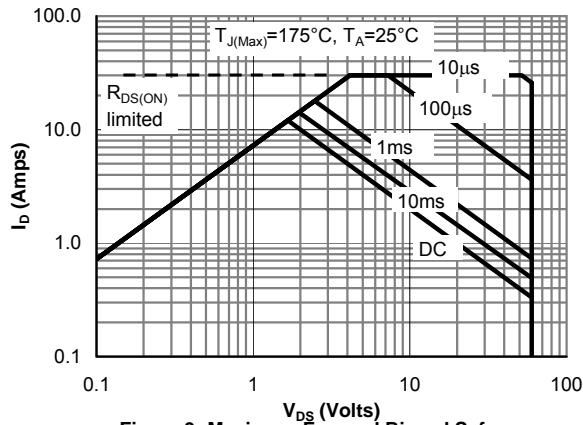


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

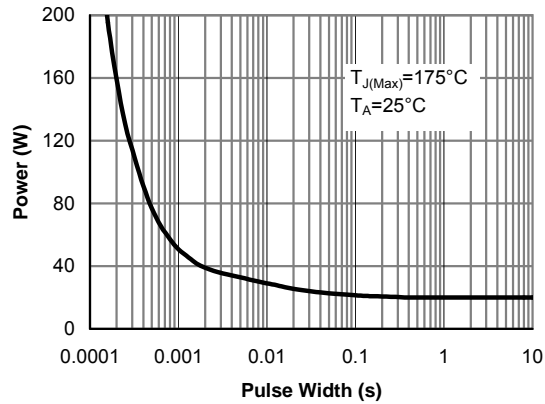


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

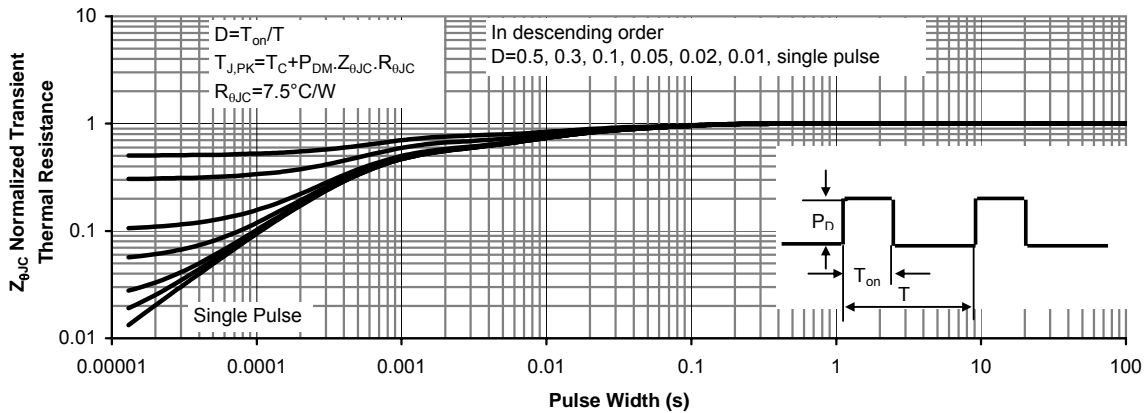


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

N-Channel MOSFET TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

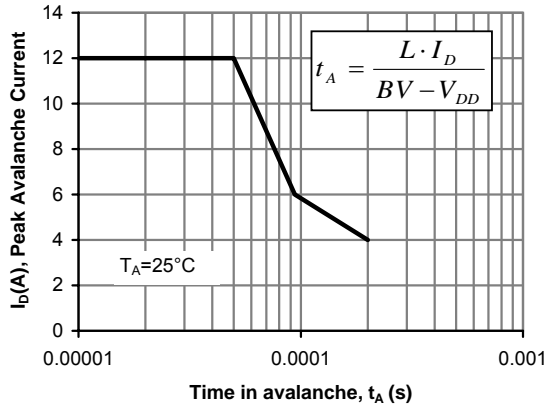


Figure 12: Single Pulse Avalanche capability

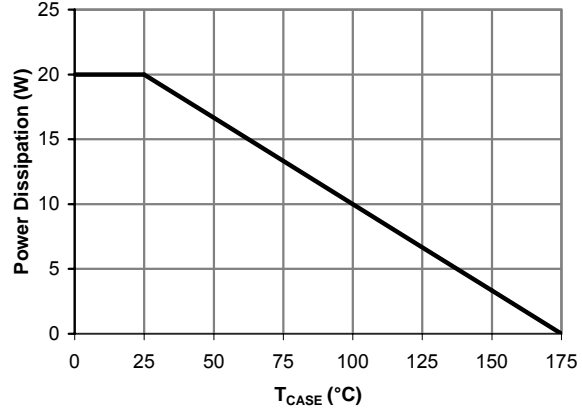


Figure 13: Power De-rating (Note B)

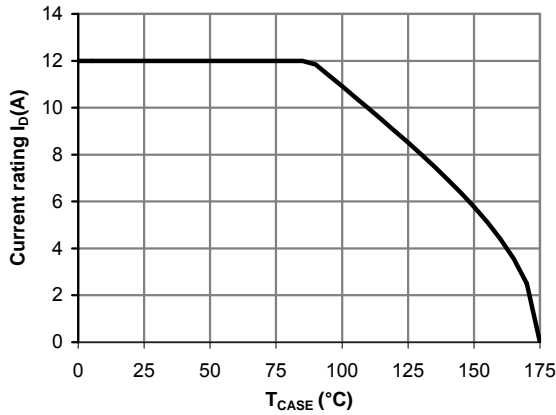


Figure 14: Current De-rating (Note B)

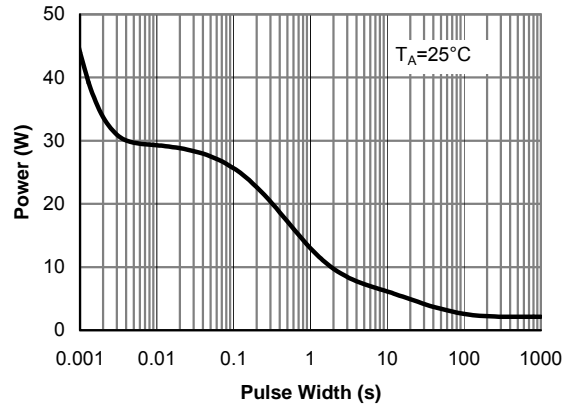


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

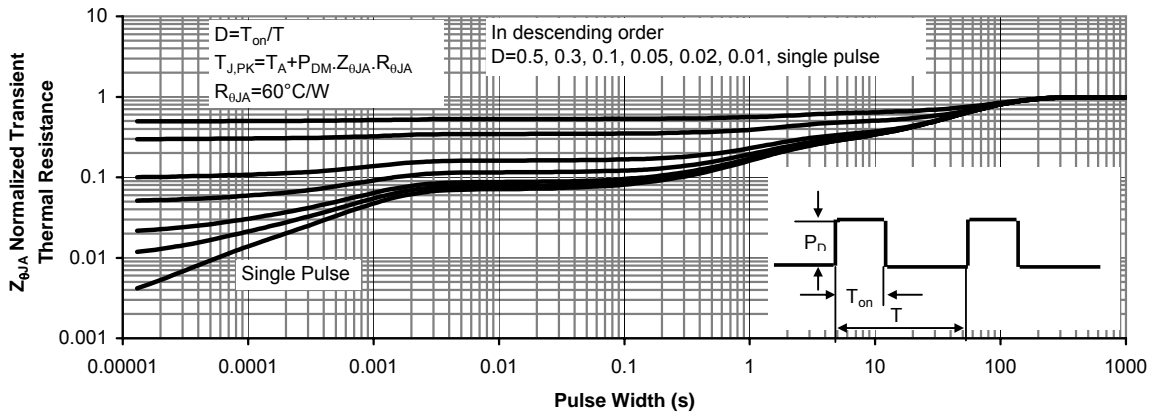


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}$ , $V_{GS}=0\text{V}$	-60			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-48\text{V}$ , $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$		-0.003	-1	$\mu\text{A}$
$I_{GSS}$	Gate-Body leakage current	$V_{DS}=0\text{V}$ , $V_{GS}=\pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ , $I_D=-250\mu\text{A}$	-1.5	-2.1	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10\text{V}$ , $V_{DS}=-5\text{V}$	-30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}$ , $I_D=-12\text{A}$ $T_J=125^\circ\text{C}$		91	115	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$ , $I_D=-6\text{A}$		114	150	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS}=-5\text{V}$ , $I_D=-12\text{A}$		12.8		S
$V_{SD}$	Diode Forward Voltage	$I_S=-1\text{A}$ , $V_{GS}=0\text{V}$		-0.76	-1	V
$I_S$	Maximum Body-Diode Continuous Current				-12	A
<b>DYNAMIC PARAMETERS</b>						
$C_{iss}$	Input Capacitance	$V_{GS}=0\text{V}$ , $V_{DS}=-30\text{V}$ , $f=1\text{MHz}$		987	1185	pF
$C_{oss}$	Output Capacitance			114		pF
$C_{rss}$	Reverse Transfer Capacitance			46		pF
$R_g$	Gate resistance	$V_{GS}=0\text{V}$ , $V_{DS}=0\text{V}$ , $f=1\text{MHz}$		7	10	$\Omega$
<b>SWITCHING PARAMETERS</b>						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}$ , $V_{DS}=-30\text{V}$ , $I_D=-12\text{A}$		15.8	20	nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			7.4	9	nC
$Q_{gs}$	Gate Source Charge			3		nC
$Q_{gd}$	Gate Drain Charge			3.5		nC
$t_{D(on)}$	Turn-On Delay Time			9		ns
$t_r$	Turn-On Rise Time	$V_{GS}=-10\text{V}$ , $V_{DS}=-30\text{V}$ , $R_L=2.5\Omega$		10		ns
$t_{D(off)}$	Turn-Off Delay Time	$R_{GEN}=3\Omega$		25		ns
$t_f$	Turn-Off Fall Time			11		ns
$t_{rr}$	Body Diode Reverse Recovery Time	$I_F=-12\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$		27.5	35	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge	$I_F=-12\text{A}$ , $di/dt=100\text{A}/\mu\text{s}$		30		nC

A: The value of R qJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The Power dissipation PDSM is based on R qJA and the maximum allowed junction temperature of  $150^\circ\text{C}$ . The value in any given application depends on the user's specific board design, and the maximum temperature of  $175^\circ\text{C}$  may be used if the PCB allows it.

B: The power dissipation PD is based on  $T_J(\text{MAX})=175^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature  $T_J(\text{MAX})=175^\circ\text{C}$ .

D: The R qJA is the sum of the thermal impedance from junction to case R qJC and case to ambient.

E: The static characteristics in Figures 1 to 6 are obtained using  $<300\text{ms}$  pulses, duty cycle 0.5% max.

F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_J(\text{MAX})=175^\circ\text{C}$ .

G: The maximum current rating is limited by bond-wires.

H: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^\circ\text{C}$ . The SOA curve provides a single pulse rating.

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P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

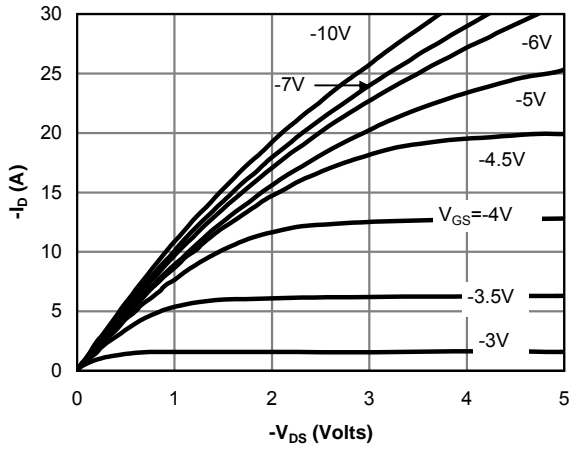


Fig 1: On-Region Characteristics

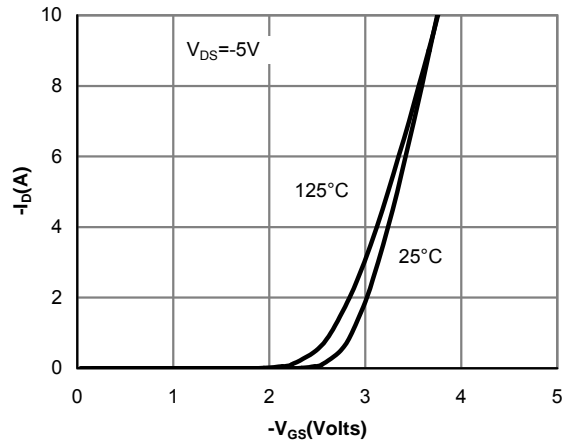


Figure 2: Transfer Characteristics

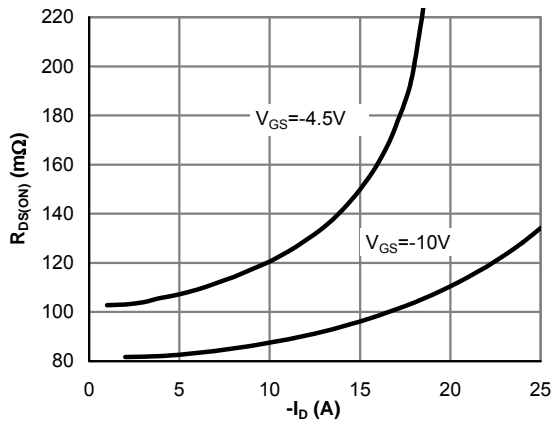


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

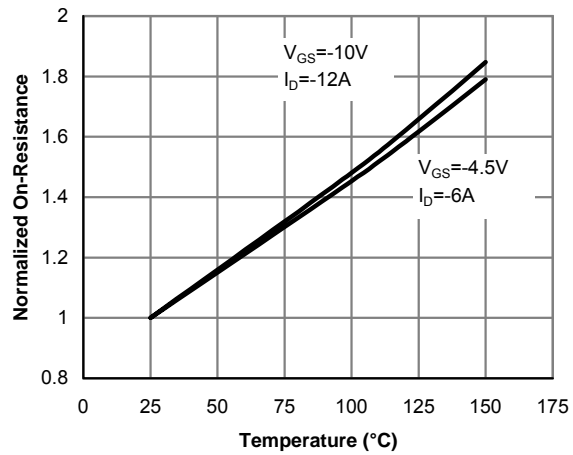


Figure 4: On-Resistance vs. Junction Temperature

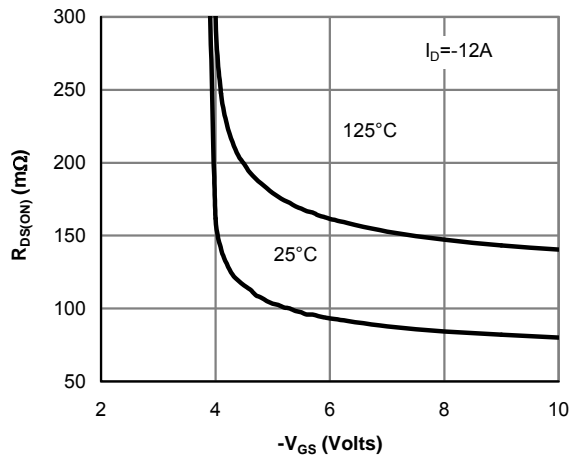


Figure 5: On-Resistance vs. Gate-Source Voltage

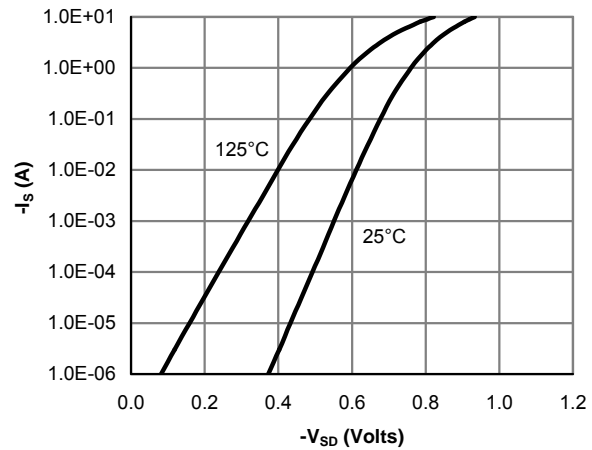


Figure 6: Body-Diode Characteristics

P-Channel MOSFET Electrical Characteristics ( $T_J=25^\circ\text{C}$  unless otherwise noted)

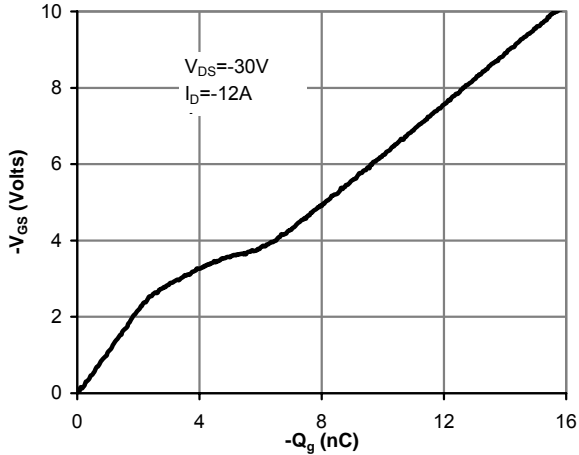


Figure 7: Gate-Charge Characteristics

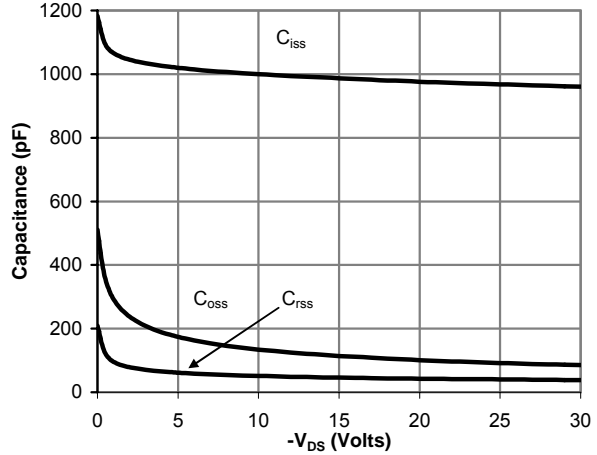


Figure 8: Capacitance Characteristics

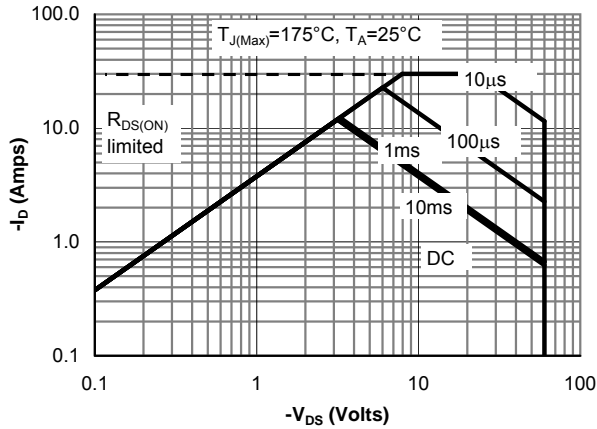


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

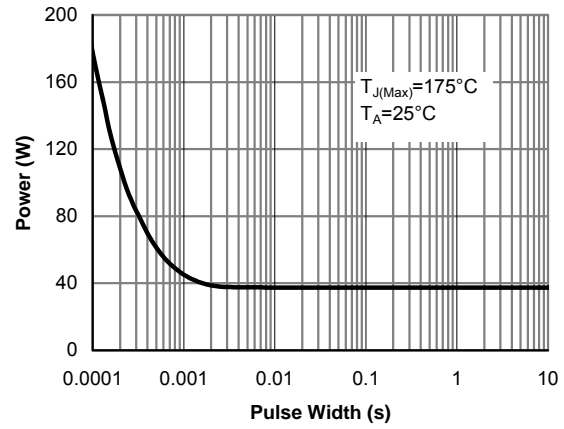


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

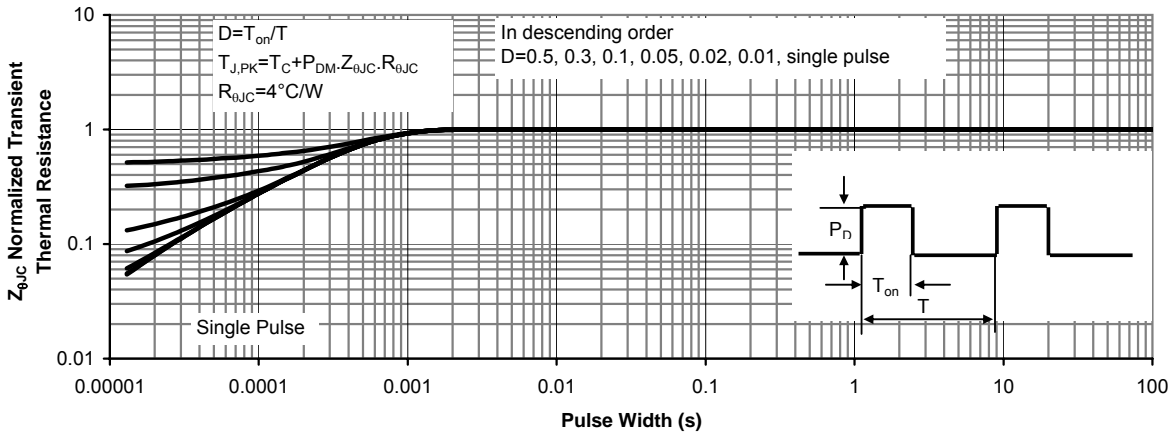


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



P-Channel MOSFET Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

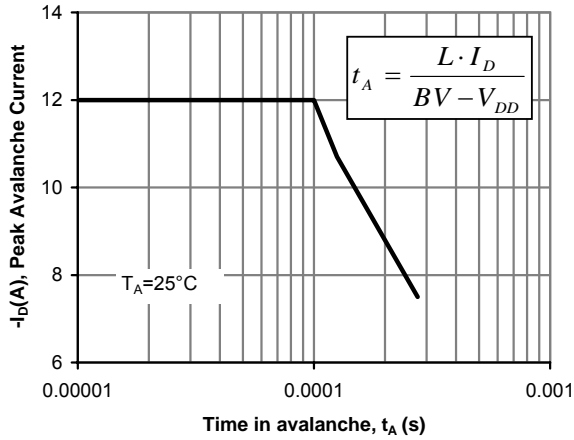


Figure 12: Single Pulse Avalanche capability

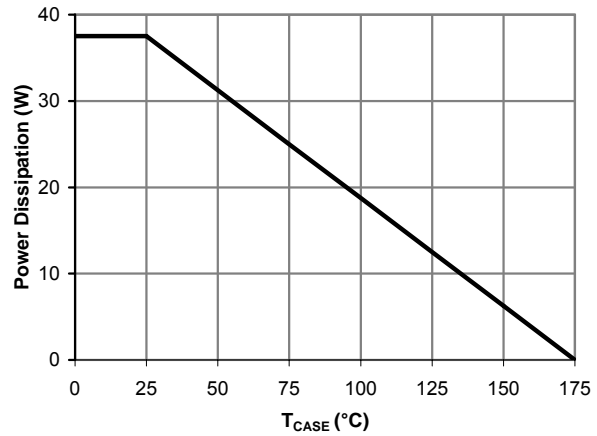


Figure 13: Power De-rating (Note B)

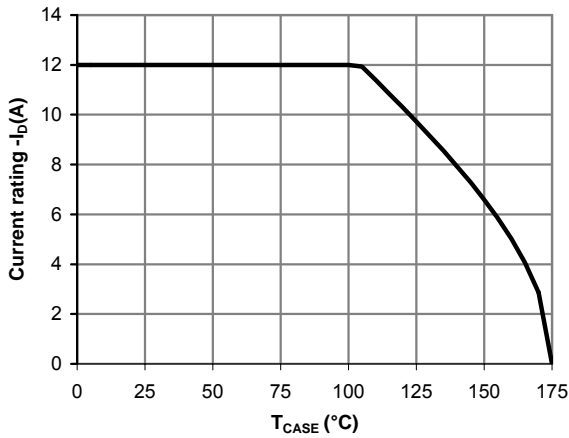


Figure 14: Current De-rating (Note B)

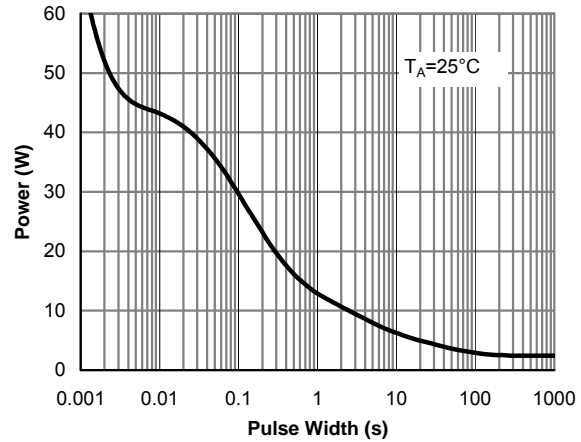


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

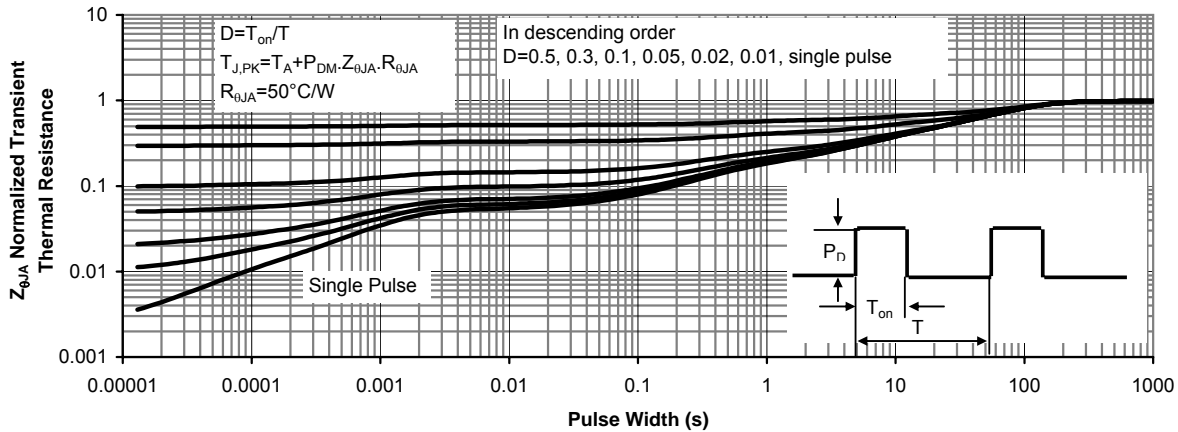


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)