



AO4614B

Complementary Enhancement Mode Field Effect Transistor

General Description

The AO4614B/L uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications. AO4614B and AO4614BL are electrically identical.

-RoHS Compliant

-AO4614BL is Halogen Free

Features

n-channel

V_{DS} (V) = 40V, I_D = 6A (V_{GS} =10V)

$R_{DS(ON)}$ < 30m Ω (V_{GS} =10V)

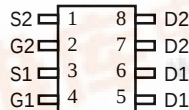
$R_{DS(ON)}$ < 38m Ω (V_{GS} =4.5V)

p-channel

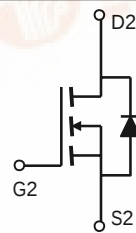
V_{DS} (V) = -40V, I_D = -5A (V_{GS} =-10V)

$R_{DS(ON)}$ < 45m Ω (V_{GS} = -10V)

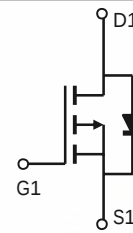
$R_{DS(ON)}$ < 63m Ω (V_{GS} = -4.5V)



SOIC-8



n-channel



p-channel

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Max n-channel	Max p-channel	Units
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current ^A	I_D	6	-5	A
$T_A=25^\circ\text{C}$		5	-4	
$T_A=70^\circ\text{C}$		30	-30	
Pulsed Drain Current ^B	I_{DM}	14	-20	
Avalanche Current ^B	I_{AR}	9.8	20	mJ
Repetitive avalanche energy $L=0.1\text{mH}$ ^B	E_{AR}	2	2	W
Power Dissipation	P_D	1.28	1.28	W
$T_A=25^\circ\text{C}$				
$T_A=70^\circ\text{C}$				
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	-55 to 150	$^\circ\text{C}$

Thermal Characteristics: n-channel and p-channel

Parameter	Symbol	Device	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
$t \leq 10\text{s}$		n-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	48	62.5	$^\circ\text{C/W}$
Steady-State		p-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	n-ch	35	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	p-ch	35	50	$^\circ\text{C/W}$
$t \leq 10\text{s}$		p-ch	35	50	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	n-ch	48	62.5	$^\circ\text{C/W}$
Steady-State		n-ch	74	110	$^\circ\text{C/W}$
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	p-ch	35	50	$^\circ\text{C/W}$

N Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D =250μA	1.7	2.5	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =6A T _J =125°C		24 36	30 45	mΩ
		V _{GS} =4.5V, I _D =5A		30	38	
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =6A		19		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz		516	650	pF
C _{oss}	Output Capacitance			82		pF
C _{rss}	Reverse Transfer Capacitance			43		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		4.6		Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =6A		8.9	10.8	nC
Q _g (4.5V)	Total Gate Charge			4.3	5.6	nC
Q _{gs}	Gate Source Charge			2.4		nC
Q _{gd}	Gate Drain Charge			1.4		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =3.3Ω, R _{GEN} =3Ω		6.4		ns
t _r	Turn-On Rise Time			3.6		ns
t _{D(off)}	Turn-Off DelayTime			16.2		ns
t _f	Turn-Off Fall Time			6.6		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =6A, dI/dt=100A/μs		18	24	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =6A, dI/dt=100A/μs		10		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

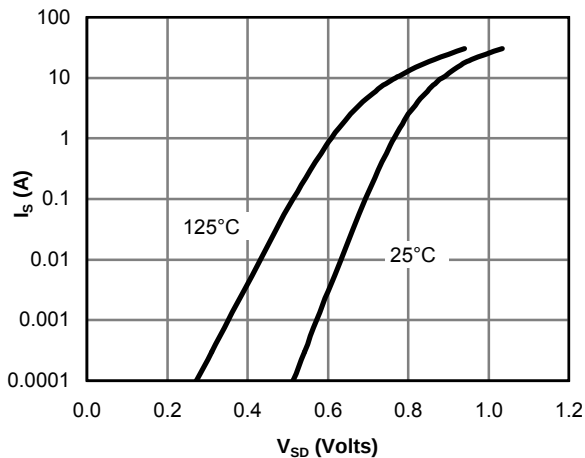
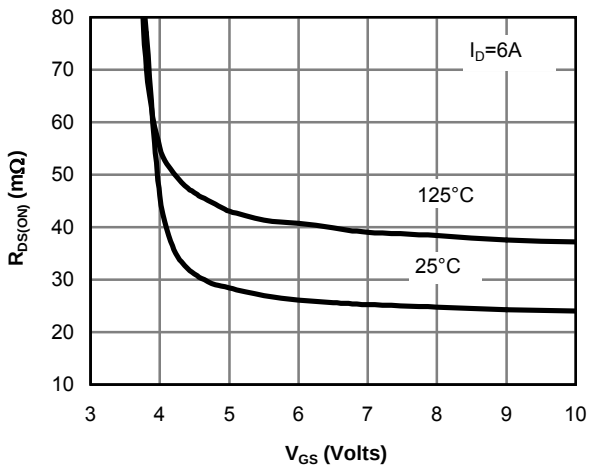
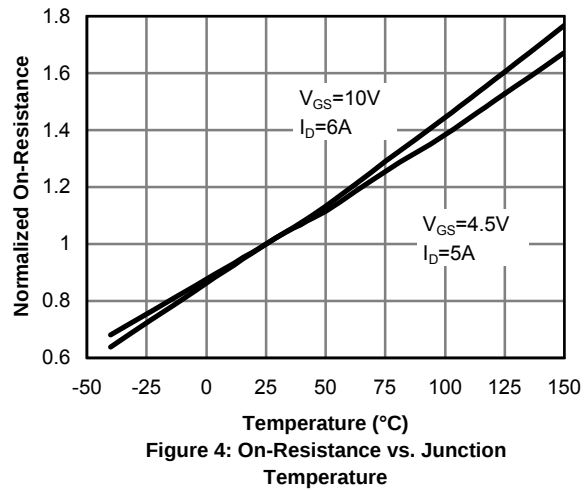
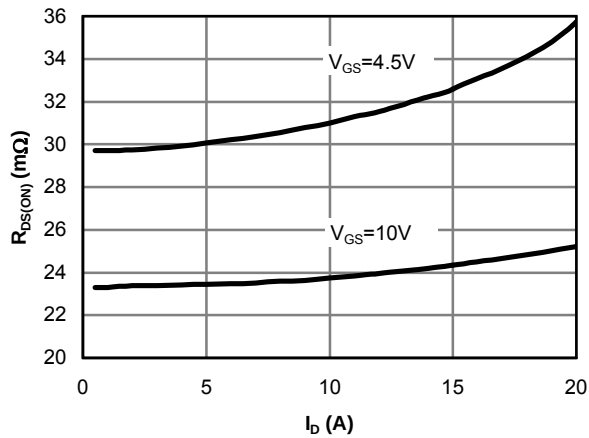
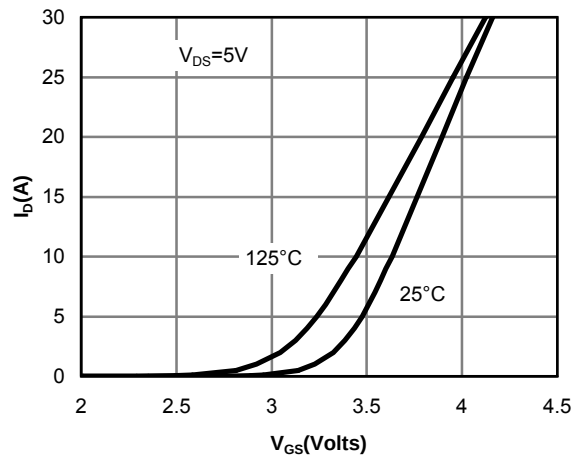
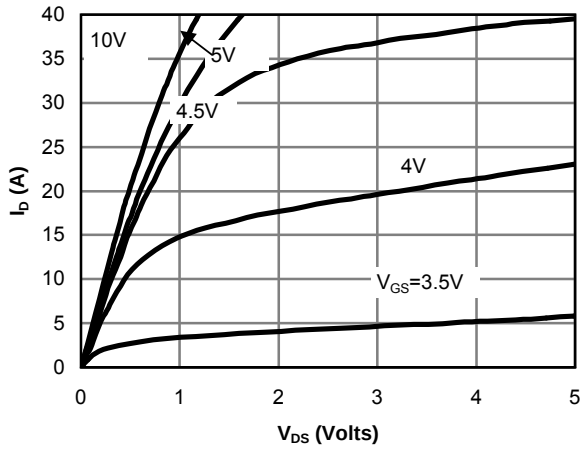
D. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev0 : Sept 2007

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: N-CHANNEL



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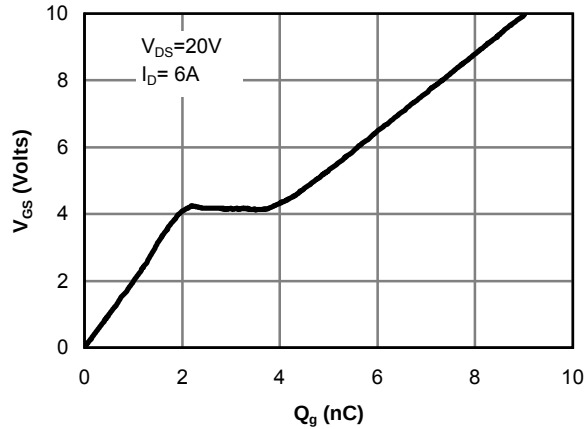


Figure 7: Gate-Charge Characteristics

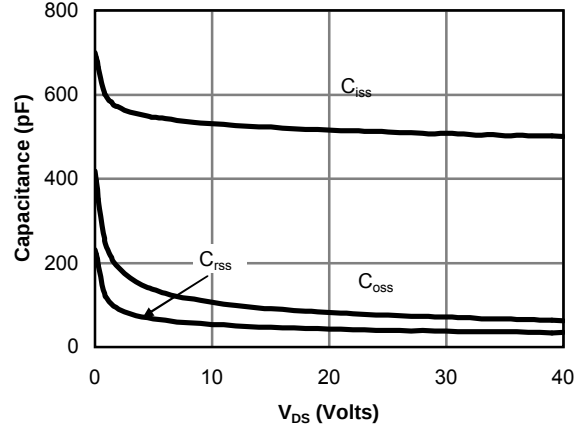


Figure 8: Capacitance Characteristics

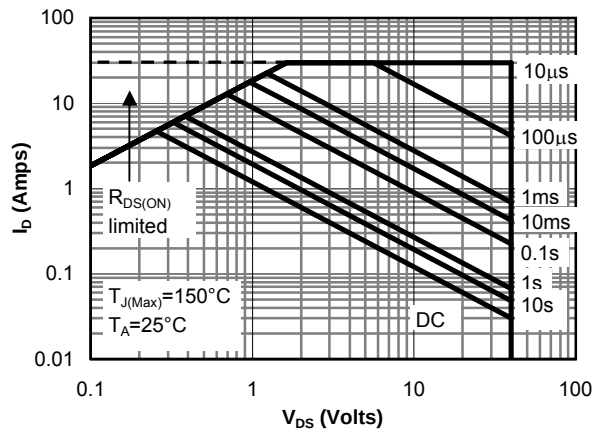


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

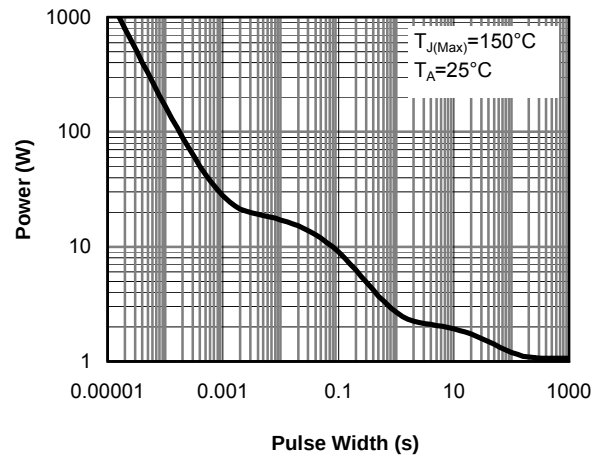


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

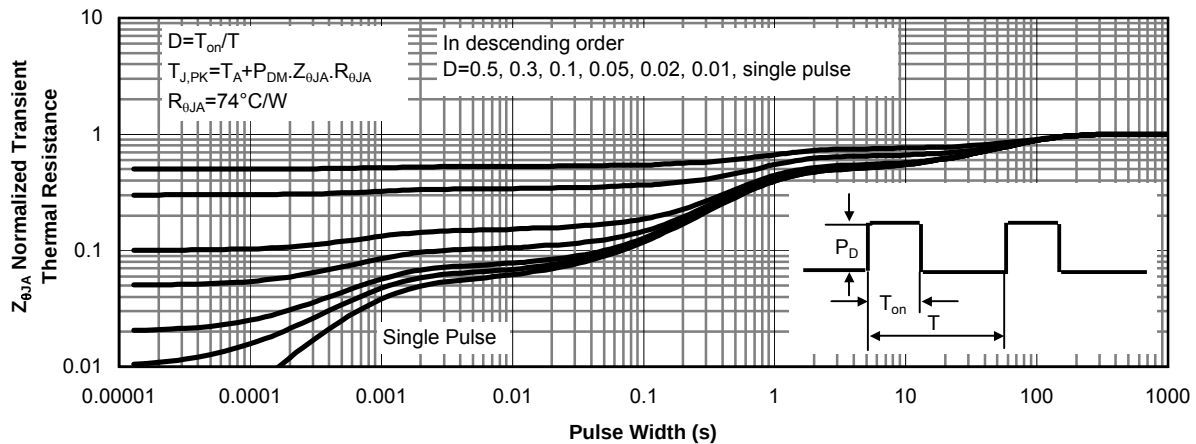


Figure 11: Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = -250μA, V _{GS} =0V	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} I _D = -250μA	-1.7	-2	-3	V
I _{D(ON)}	On state drain current	V _{GS} = -10V, V _{DS} = -5V	-30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} = -10V, I _D = -5A T _J =125°C		36 52	45 65	mΩ
		V _{GS} = -4.5V, I _D = -4A		50	63	
g _{FS}	Forward Transconductance	V _{DS} = -5V, I _D = -5A		13		S
V _{SD}	Diode Forward Voltage	I _S = -1A, V _{GS} =0V		-0.76	-1	V
I _S	Maximum Body-Diode Continuous Current				-2	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} = -20V, f=1MHz		940	1175	pF
C _{oss}	Output Capacitance			97		pF
C _{rss}	Reverse Transfer Capacitance			72		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		14		Ω
SWITCHING PARAMETERS						
Q _g (-10V)	Total Gate Charge	V _{GS} = -10V, V _{DS} = -20V, I _D = -5A		17	22	nC
Q _g (-4.5V)	Total Gate Charge			7.9	10	nC
Q _{gs}	Gate Source Charge			3.4		nC
Q _{gd}	Gate Drain Charge			3.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} = -10V, V _{DS} = -20V, R _L =4Ω, R _{GEN} =3Ω		6.2		ns
t _r	Turn-On Rise Time			8.4		ns
t _{D(off)}	Turn-Off DelayTime			44.8		ns
t _f	Turn-Off Fall Time			41.2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F = -5A, dI/dt=100A/μs		21	27	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F = -5A, dI/dt=100A/μs		14		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

D: The static characteristics in Figures 1 to 6,12,14 are obtained using <300μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

Rev0 : Sept 2007

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

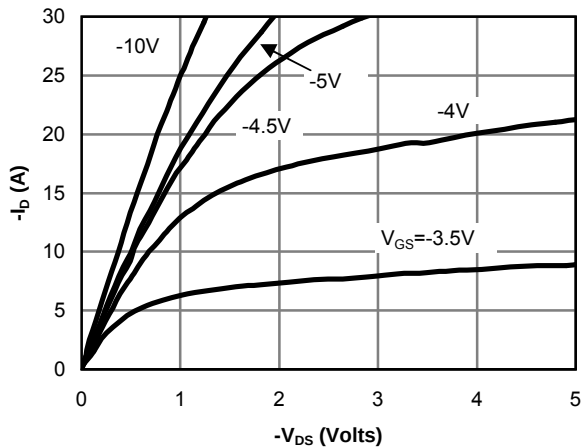


Fig 12: On-Region Characteristics

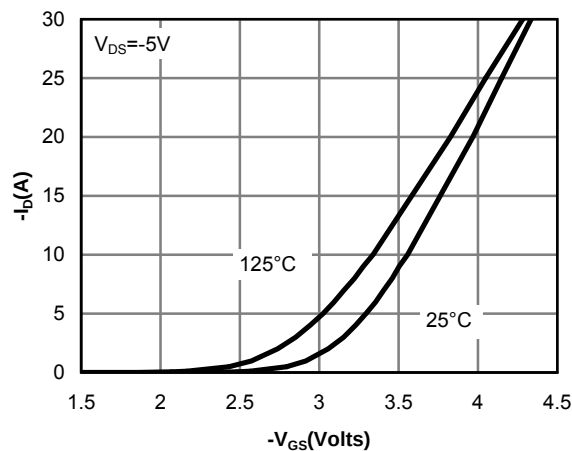


Figure 13: Transfer Characteristics

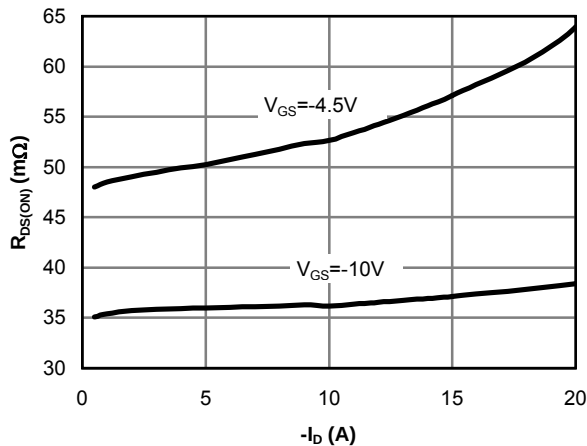


Figure 14: On-Resistance vs. Drain Current and Gate Voltage

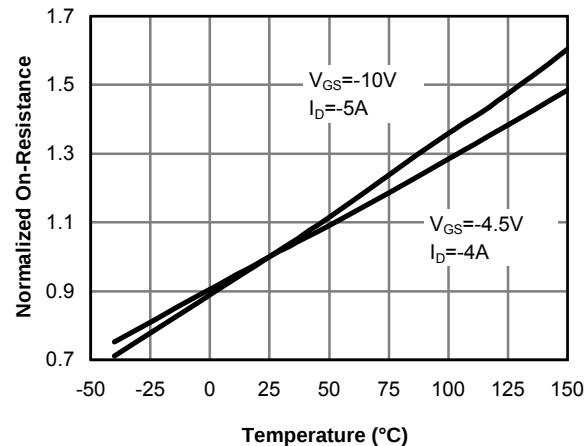


Figure 15: On-Resistance vs. Junction Temperature

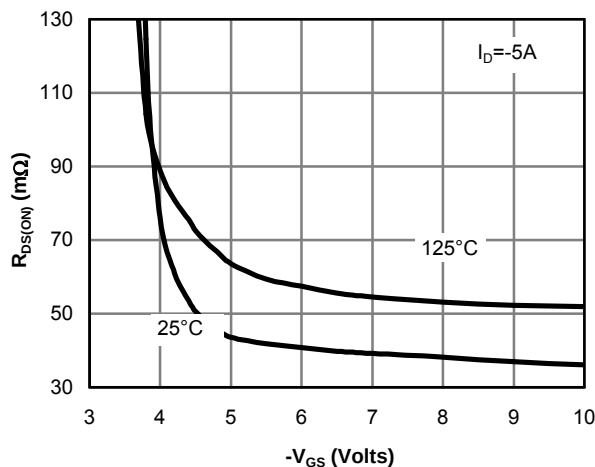


Figure 16: On-Resistance vs. Gate-Source Voltage

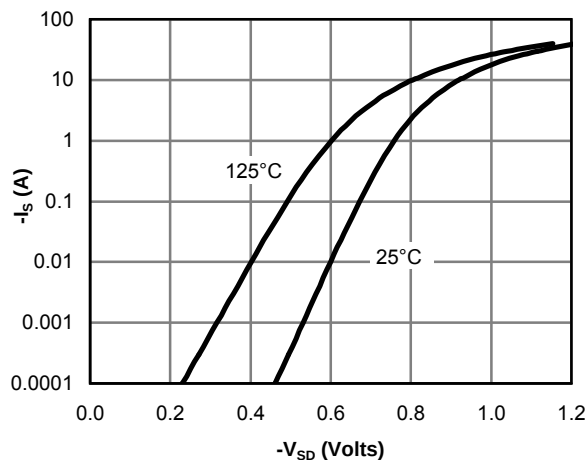


Figure 17: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS: P-CHANNEL

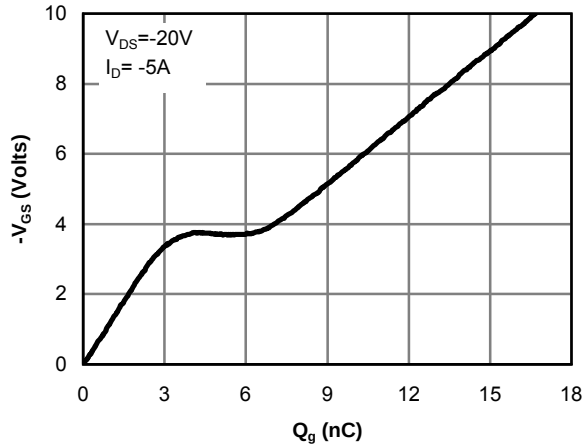


Figure 18: Gate-Charge Characteristics

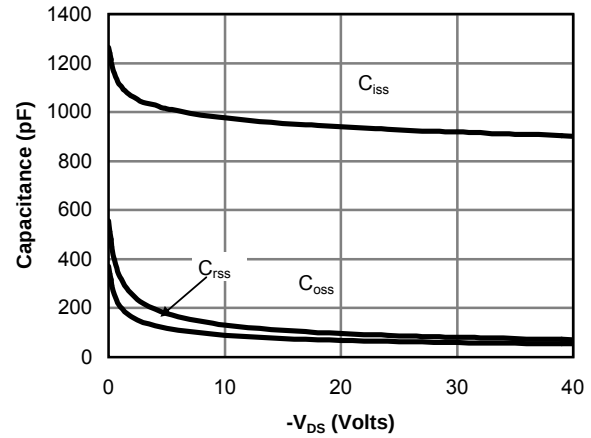


Figure 19: Capacitance Characteristics

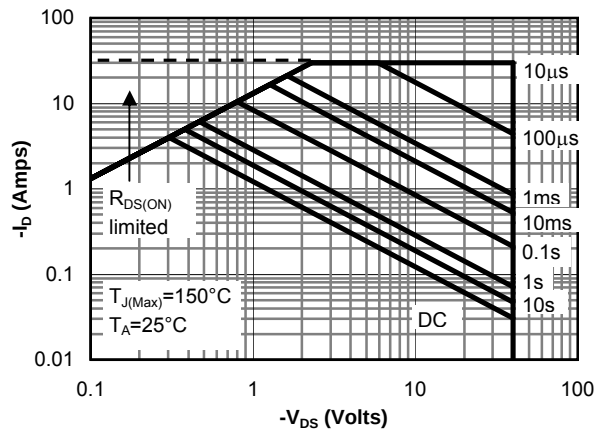


Figure 20: Maximum Forward Biased Safe Operating Area (Note E)

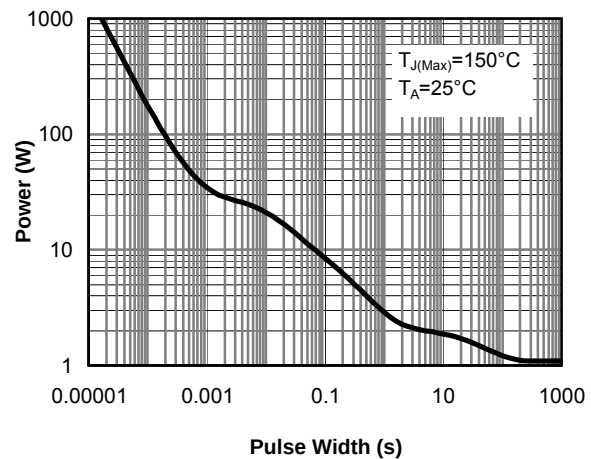


Figure 21: Single Pulse Power Rating Junction-to-Ambient (Note E)

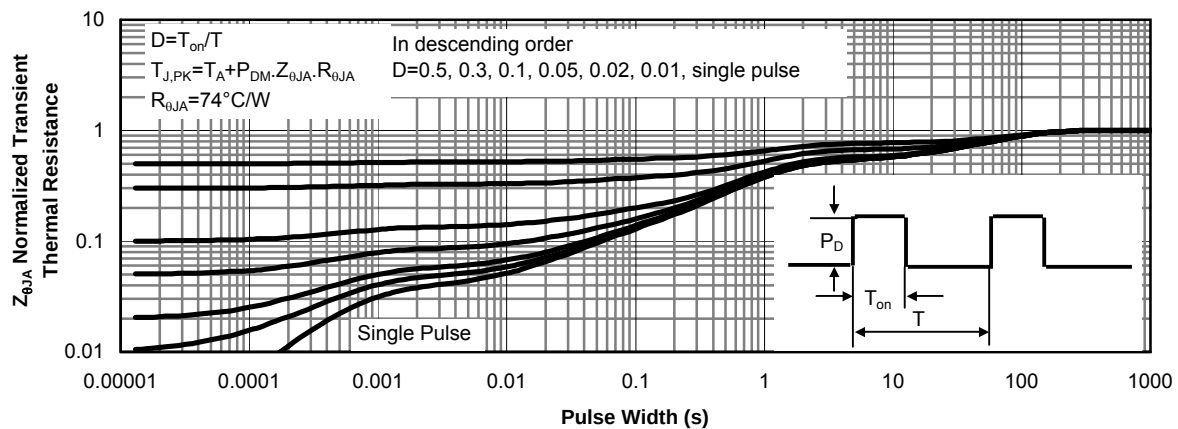


Figure 22: Normalized Maximum Transient Thermal Impedance