

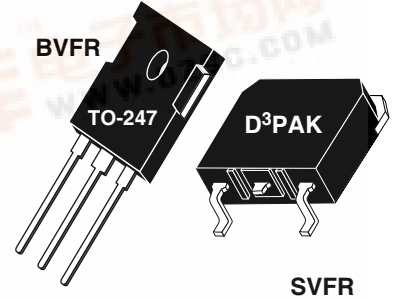


APT1201R6BVFR APT1201R6SVFR

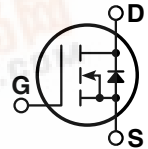
1200V 8A 1.600Ω

POWER MOS V[®] FREDFET

Power MOS V[®] is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V[®] also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **Avalanche Energy Rated**
- **Lower Leakage**
- **FAST RECOVERY BODY DIODE**
- **TO-247 or Surface Mount D³PAK Package**



MAXIMUM RATINGS

All Ratings: T_C = 25°C unless otherwise specified.

Symbol	Parameter	APT1201R6BVFR_SVFR	UNIT
V _{DSS}	Drain-Source Voltage	1200	Volts
I _D	Continuous Drain Current @ T _C = 25°C	8	Amps
I _{DM}	Pulsed Drain Current ^①	32	
V _{GS}	Gate-Source Voltage Continuous	±30	Volts
V _{GSM}	Gate-Source Voltage Transient	±40	
P _D	Total Power Dissipation @ T _C = 25°C	280	Watts
	Linear Derating Factor	2.24	W/°C
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T _L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I _{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	8	Amps
E _{AR}	Repetitive Avalanche Energy ^①	30	mJ
E _{AS}	Single Pulse Avalanche Energy ^④	1210	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV _{DSS}	Drain-Source Breakdown Voltage (V _{GS} = 0V, I _D = 250μA)	1200			Volts
I _{D(on)}	On State Drain Current ^② (V _{DS} > I _{D(on)} × R _{DS(on)} Max, V _{GS} = 10V)	8			Amps
R _{DS(on)}	Drain-Source On-State Resistance ^② (V _{GS} = 10V, I _D = 4A)			1.600	Ohms
I _{DSS}	Zero Gate Voltage Drain Current (V _{DS} = 1200V, V _{GS} = 0V)			250	μA
	Zero Gate Voltage Drain Current (V _{DS} = 960V, V _{GS} = 0V, T _C = 125°C)			1000	
I _{GSS}	Gate-Source Leakage Current (V _{GS} = ±30V, V _{DS} = 0V)			±100	nA
V _{GS(th)}	Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 1.0mA)	2		4	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT1201R6BVFR_SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$		3050	3660	pF
C_{oss}	Output Capacitance	$V_{DS} = 25V$		255	360	
C_{rss}	Reverse Transfer Capacitance	$f = 1\text{ MHz}$		125	190	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$		155	230	nC
Q_{gs}	Gate-Source Charge	$V_{DD} = 0.5 V_{DSS}$		15	23	
Q_{gd}	Gate-Drain ("Miller") Charge	$I_D = I_D[\text{Cont.}] @ 25^\circ\text{C}$		78	115	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$		12	24	ns
t_r	Rise Time	$V_{DD} = 0.5 V_{DSS}$		10	20	
$t_{d(off)}$	Turn-off Delay Time	$I_D = I_D[\text{Cont.}] @ 25^\circ\text{C}$		50	75	
t_f	Fall Time	$R_G = 1.6\Omega$		15	30	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			8	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			32	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -I_D[\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D[\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		220	ns
		$T_j = 125^\circ\text{C}$		450	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D[\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	1.0		μC
		$T_j = 125^\circ\text{C}$	3.0		
I_{RRM}	Peak Recovery Current ($I_S = -I_D[\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$	10		Amps
		$T_j = 125^\circ\text{C}$	14		

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.45	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

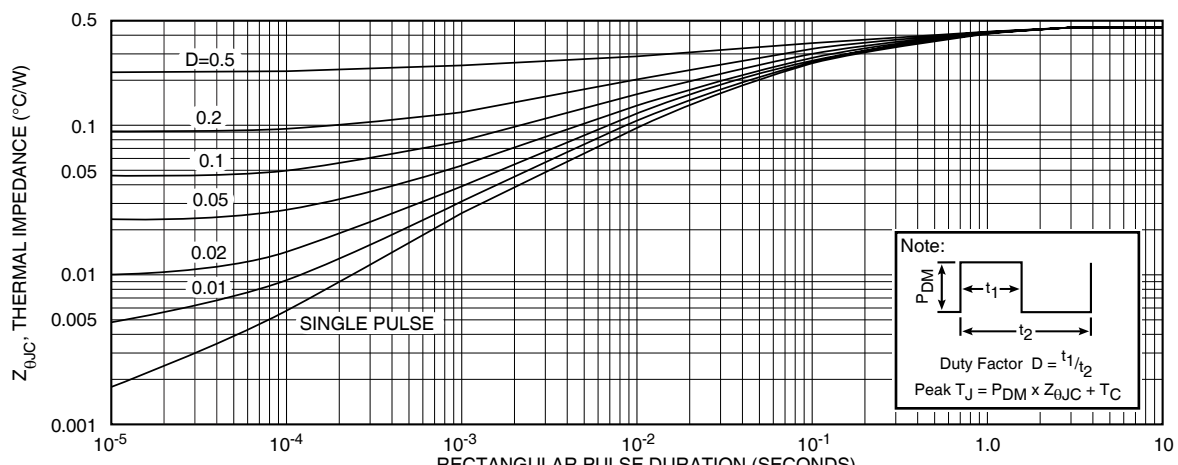
② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 37.81\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 8\text{A}$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq I_D - 8\text{A}$, $di/dt \leq 700\text{A}/\mu\text{s}$, $v_R \leq 1200\text{V}$, $T_j \leq 150^\circ\text{C}$

APT Reserves the right to change, without notice, the specifications and information contained herein.



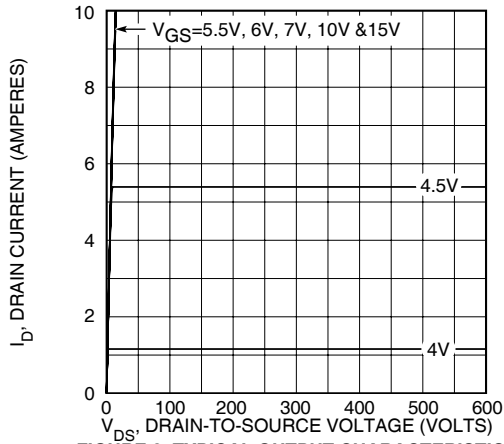


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

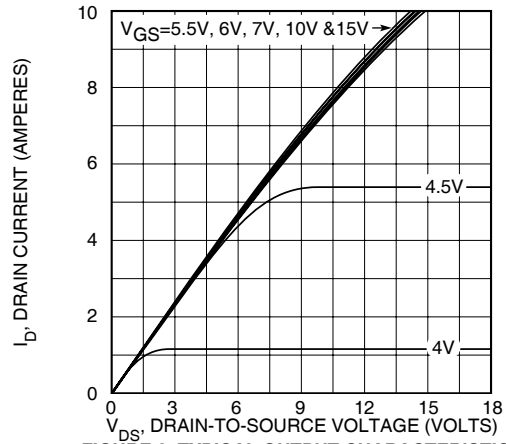


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

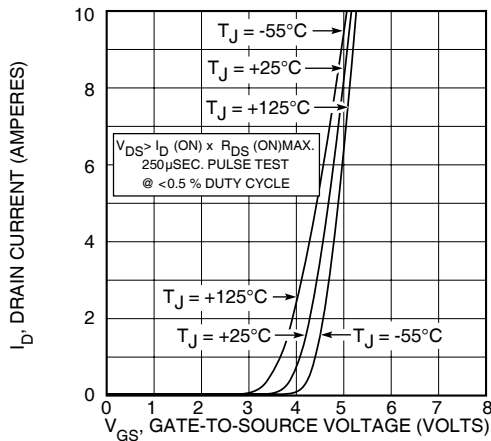


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

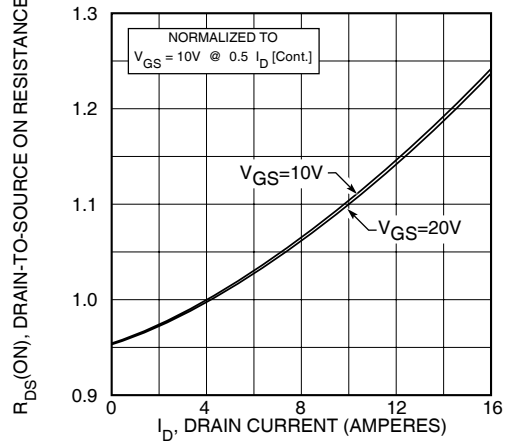


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

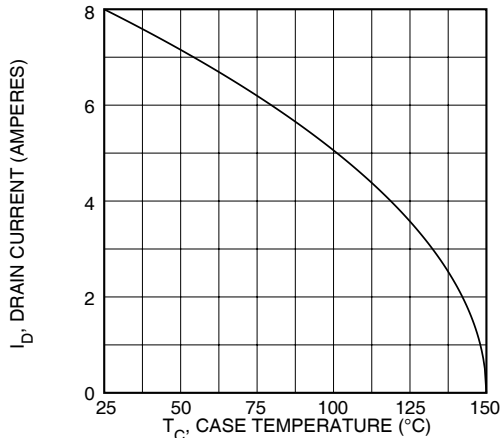


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

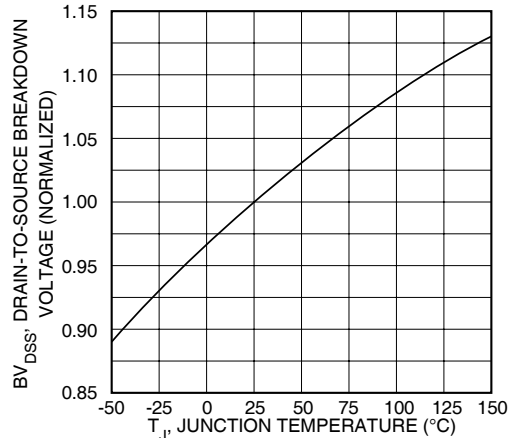


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

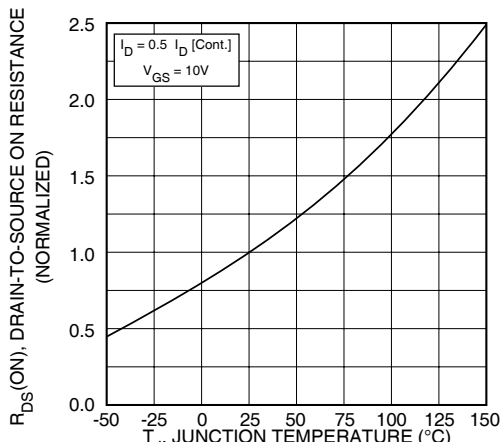


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

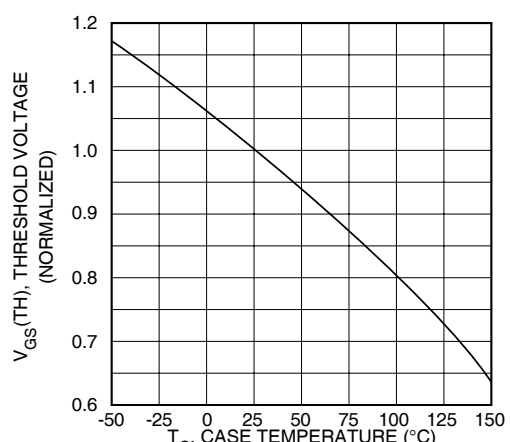


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

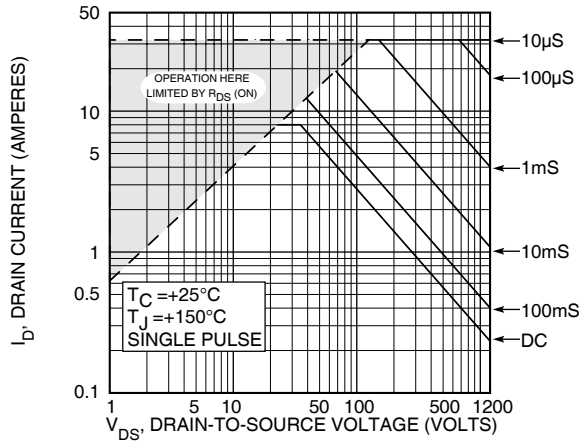


FIGURE 10, MAXIMUM SAFE OPERATING AREA

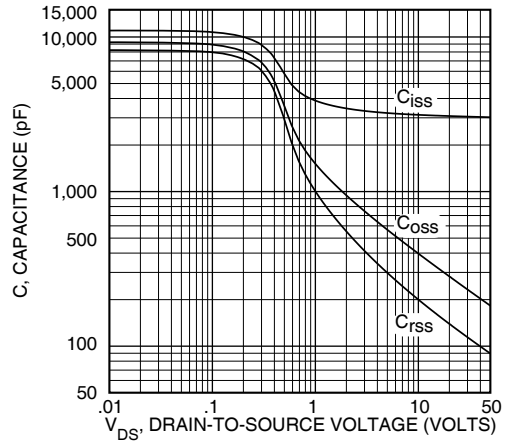


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

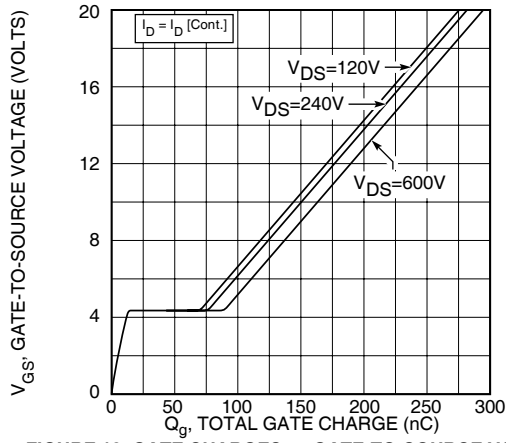


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

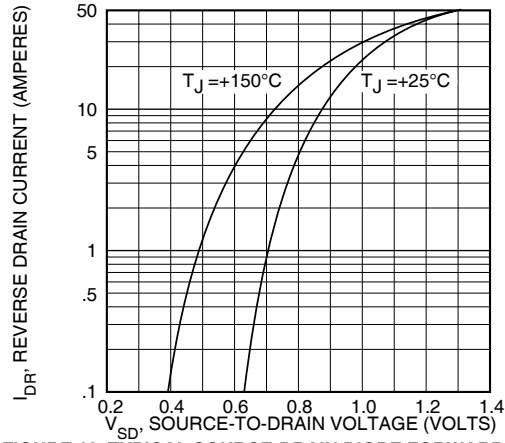
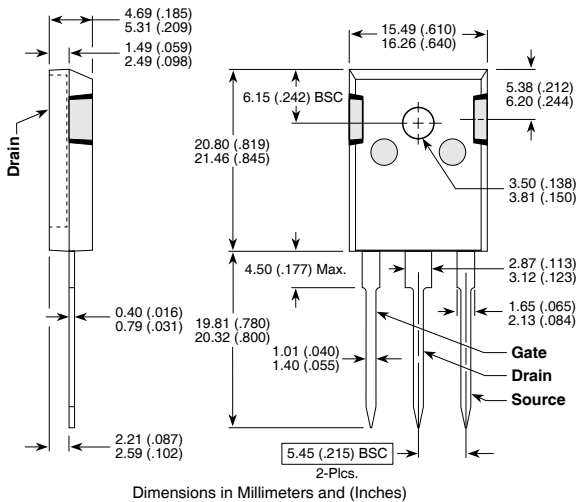


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline (BVFR)



D³PAK Package Outline (SVFR)

