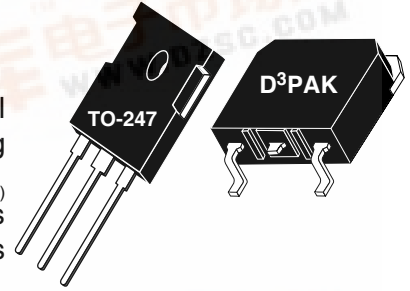




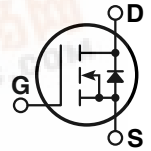
APT1204R7BFLFLL APT1204R7SFLFLL 1200V 3.5A 4.700Ω

POWER MOS 7[®] FREDFET

Power MOS 7[®] is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7[®] by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7[®] combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.



- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ C$ unless otherwise specified.

Symbol	Parameter	APT1204R7BFLFLL_SFLFLL	UNIT
V_{DSS}	Drain-Source Voltage	1200	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ C$	3.5	Amps
I_{DM}	Pulsed Drain Current ^①	14	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ $T_C = 25^\circ C$	135	Watts
	Linear Derating Factor	1.08	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	3.5	Amps
E_{AR}	Repetitive Avalanche Energy ^①	10	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	425	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu A$)	1200			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, I_D = 1.75A$)			4.70	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = 1200V, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 960V, V_{GS} = 0V, T_C = 125^\circ C$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1mA$)	3		5	Volts

CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

DYNAMIC CHARACTERISTICS

APT1204R7BFL SFL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$		716	900	pF
C_{oss}	Output Capacitance			132	200	
C_{rss}	Reverse Transfer Capacitance			36	60	
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 600V$ $I_D = 3.5A @ 25^\circ C$		31	50	nC
Q_{gs}	Gate-Source Charge			4	5	
Q_{gd}	Gate-Drain ("Miller") Charge			21	40	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 600V$ $I_D = 3.5A @ 25^\circ C$ $R_G = 1.6\Omega$		7	14	ns
t_r	Rise Time			2	4	
$t_{d(off)}$	Turn-off Delay Time			20	30	
t_f	Fall Time			24	50	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			3.5	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			14	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -I_D 3.5A$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ⑤			18	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D 3.5A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		250	ns
		$T_j = 125^\circ C$		515	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D 3.5A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$.5	μC
		$T_j = 125^\circ C$		1.1	
I_{RRM}	Peak Recovery Current ($I_S = -I_D 3.5A, di/dt = 100A/\mu s$)	$T_j = 25^\circ C$		8.3	Amps
		$T_j = 125^\circ C$		11.5	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.90	$^\circ C/W$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

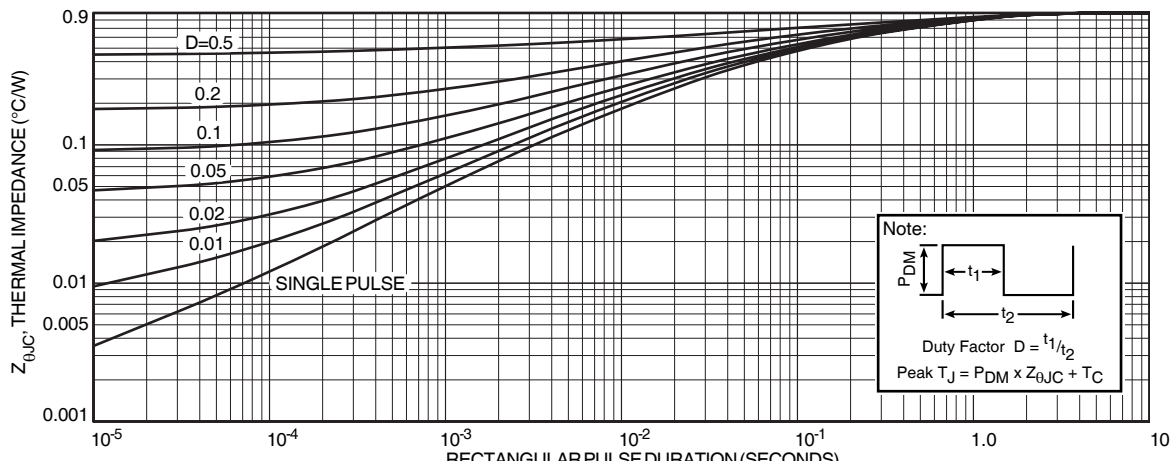
② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ C, L = 69.39mH, R_G = 25\Omega, \text{Peak } I_L = 3.5A$

⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. $I_S \leq -I_D 3.5A \quad di/dt \leq 700A/\mu s \quad V_R \leq 1200 \quad T_j \leq 150^\circ C$

APT Reserves the right to change, without notice, the specifications and information contained herein.



Typical Performance Curves

APT1204R7 BFLI_SFLI

Graph Deleted

FIGURE 2, HIGH VOLTAGE OUTPUT CHARACTERISTICS

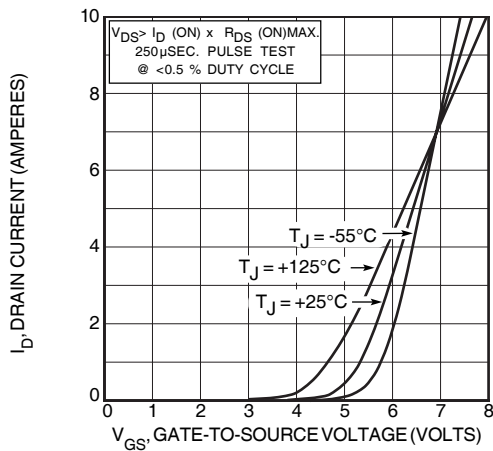


FIGURE 4, TRANSFER CHARACTERISTICS

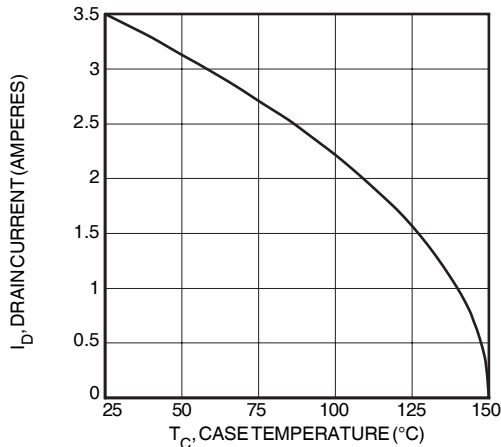


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

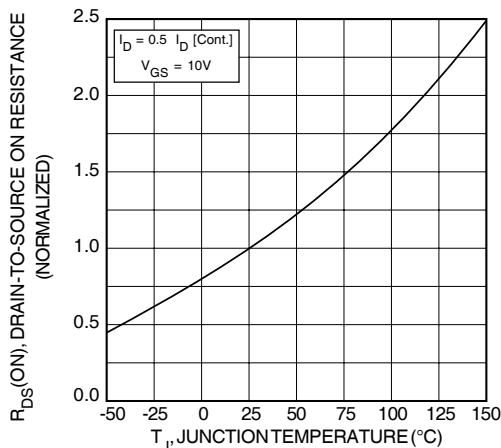


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

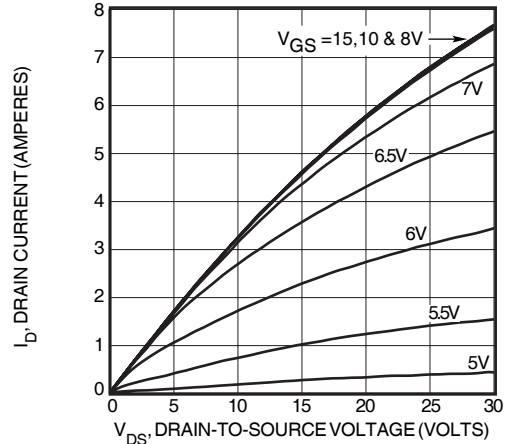


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

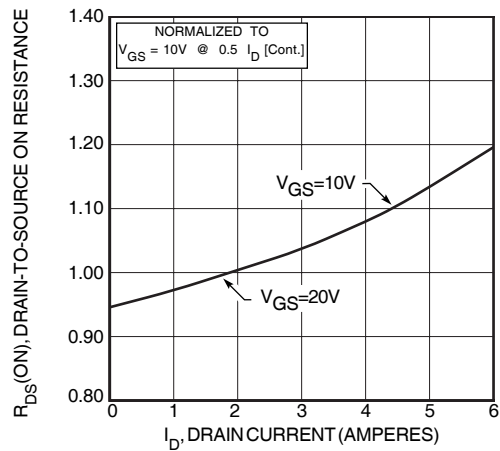


FIGURE 5, RDS(ON) vs DRAIN CURRENT

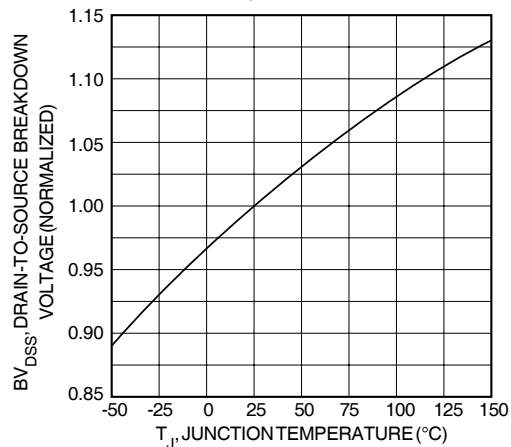


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

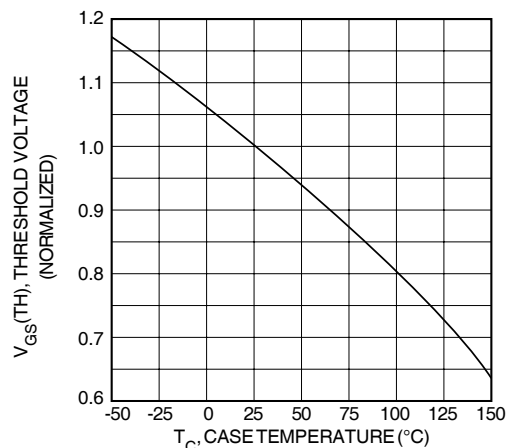


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

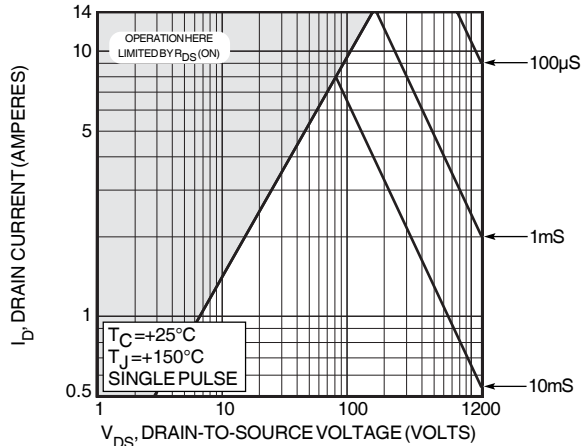


FIGURE 10, MAXIMUM SAFE OPERATING AREA

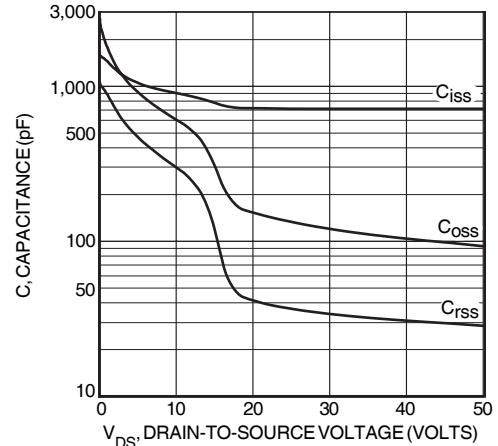


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

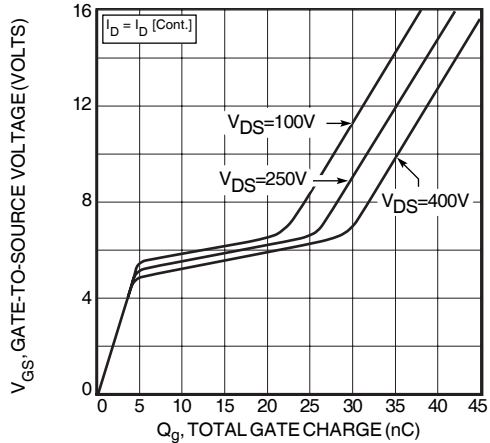


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

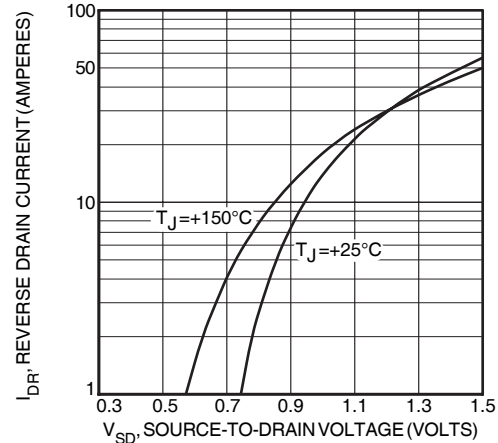
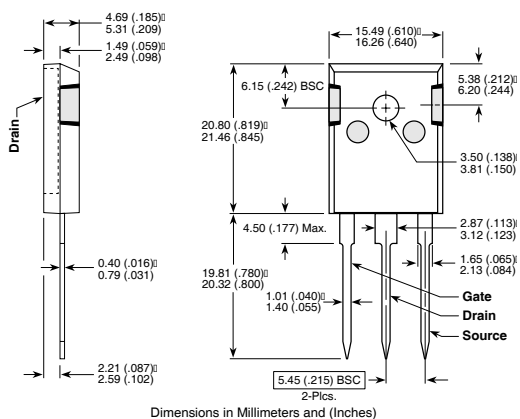


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

TO-247 Package Outline



D³PAK Package Outline

