Microsemi
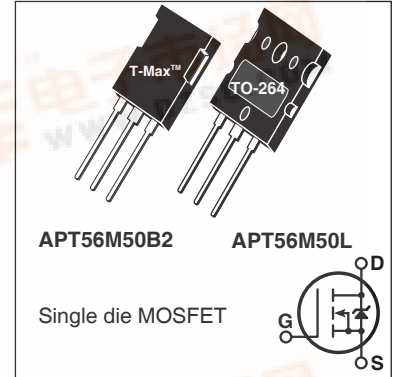**POWER PRODUCTS GROUP**

Power MOS 8 Cooler!

APT56M50B2
APT56M50L

500V, 56A, 0.10Ω Max

N-Channel MOSFET

Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low C_{rss} "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.

APT56M50B2   **APT56M50L**

Single die MOSFET

FEATURES

- Fast switching with low EMI/RFI
- Low $R_{DS(on)}$
- Ultra low C_{rss} for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant

TYPICAL APPLICATIONS

- PFC and other boost converter
- Buck converter
- Two switch forward (asymmetrical bridge)
- Single switch forward
- Flyback
- Inverters

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_D	Continuous Drain Current @ $T_C = 25°C$	56	A
	Continuous Drain Current @ $T_C = 100°C$	35	
I_{DM}	Pulsed Drain Current [1]	175	
V_{GS}	Gate-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy [2]	1200	mJ
I_{AR}	Avalanche Current, Repetitive or Non-Repetitive	28	A

Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
P_D	Total Power Dissipation @ $T_C = 25°C$			780	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.16	°C/W
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55		150	°C
T_L	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
W_T	Package Weight		0.22		oz
			6.2		g
Torque	Mounting Torque (TO-247 Package), 6-32 or M3 screw			12	in·lbf
				1.4	N·m

Static Characteristics

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250µA		500			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I_D = 250µA			0.60		V/°C
$R_{DS(on)}$	Drain-Source On Resistance③	V_{GS} = 10V, I_D = 28A			0.085	0.10	Ω
$V_{GS(th)}$	Gate-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 2.5mA		3	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient				-10		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V	T_J = 25°C			100	µA
		V_{GS} = 0V	T_J = 125°C			500	
I_{GSS}	Gate-Source Leakage Current	V_{GS} = ±30V				±100	nA

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}	Forward Transconductance	V_{DS} = 50V, I_D = 28A		42		S
C_{iss}	Input Capacitance	V_{GS} = 0V, V_{DS} = 25V f = 1MHz		8800		pF
C_{rss}	Reverse Transfer Capacitance			120		
C_{oss}	Output Capacitance			945		
$C_{o(cr)}$ ④	Effective Output Capacitance, Charge Related	V_{GS} = 0V, V_{DS} = 0V to 333V		550		
$C_{o(er)}$ ⑤	Effective Output Capacitance, Energy Related	$C_{o(er)} = \dfrac{-2.04\text{E-}7}{V_{DS}^2} + \dfrac{4.76\text{E-}8}{V_{DS}} + 1.36\text{E-}10$		275		
Q_g	Total Gate Charge	V_{GS} = 0 to 10V, I_D = 28A, V_{DS} = 250V		220		nC
Q_{gs}	Gate-Source Charge			50		
Q_{gd}	Gate-Drain Charge			100		
$t_{d(on)}$	Turn-On Delay Time	**Resistive Switching** V_{DD} = 333V, I_D = 28A R_G = 4.7Ω⑥, V_{GG} = 15V		38		ns
t_r	Current Rise Time			45		
$t_{d(off)}$	Turn-Off Delay Time			100		
t_f	Current Fall Time			33		

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			100	A
I_{SM}	Pulsed Source Current (Body Diode)①				200	
V_{SD}	Diode Forward Voltage	I_{SD} = 28A, T_J = 25°C, V_{GS} = 0V			1	V
t_{rr}	Reverse Recovery Time	I_{SD} = 28A③		660		ns
Q_{rr}	Reverse Recovery Charge	di_{SD}/dt = 100A/µs, T_J = 25°C		13.2		µC
dv/dt	Peak Recovery dv/dt	$I_{SD} \leq$ 28A, di/dt $\leq$ 1000A/µs, V_{DD} = 333V, T_J = 125°C			8	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at T_J = 25°C, L = 3.06mH, R_G = 4.7Ω, I_{AS} = 28A.

③ Pulse test: Pulse Width < 380µs, duty cycle < 2%.

④ $C_{o(cr)}$ is defined as a fixed capacitance with the same stored charge as C_{OSS} with V_{DS} = 67% of V_{DSS}.

⑤ $C_{o(er)}$ is defined as a fixed capacitance with the same stored energy as C_{OSS} with V_{DS} = 67% of V_{DSS}. The equation in the test conditions box can be used to calculate $C_{o(er)}$ for any value of V_{DS} less than V_{DSS}.

⑥ R_G is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

Microsemi reserves the right to change, without notice, the specifications and information contained herein.
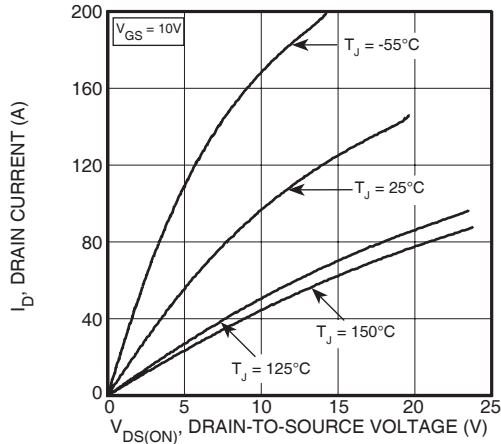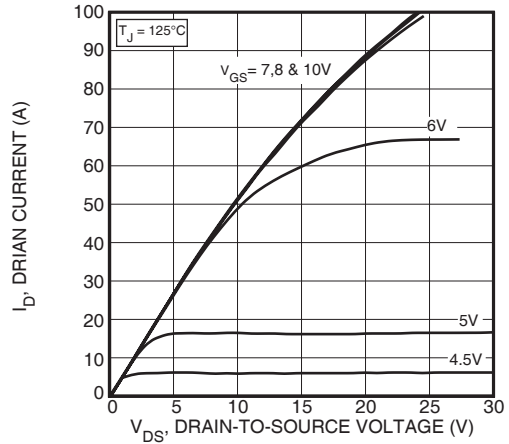
Figure 1, Output Characteristics
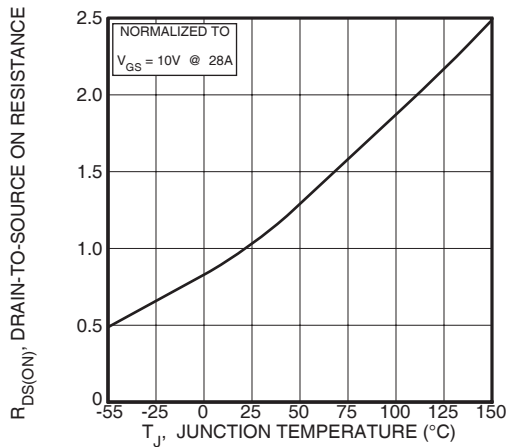

Figure 2, Output Characteristics

Figure 3, R$_{DS(ON)}$ vs Junction Temperature
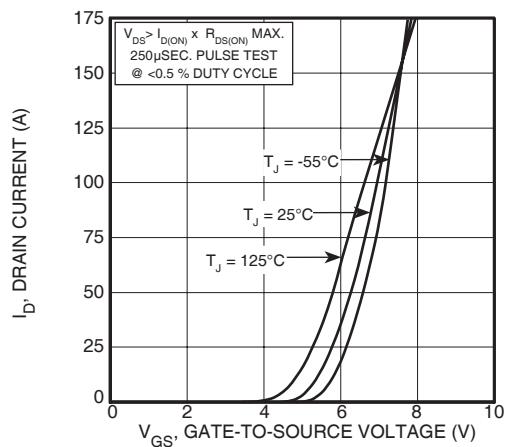

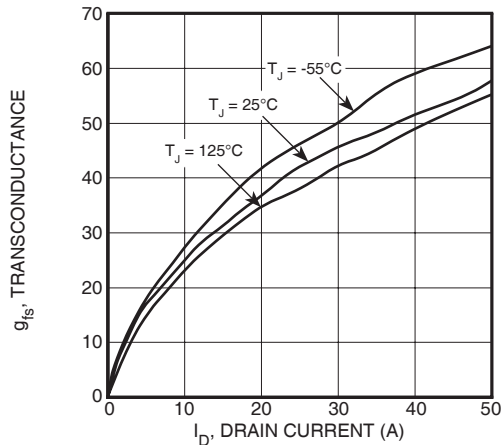**Figure 4, Transfer Characteristics**
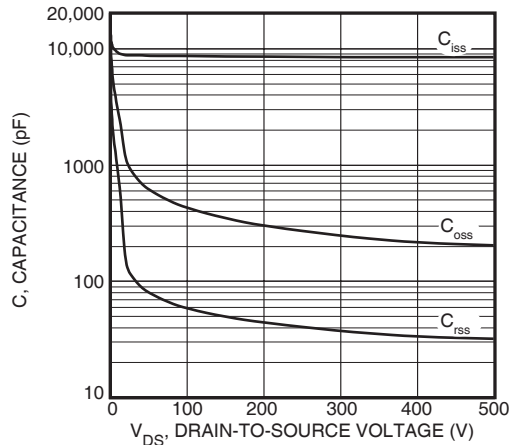

Figure 5, Gain vs Drain Current
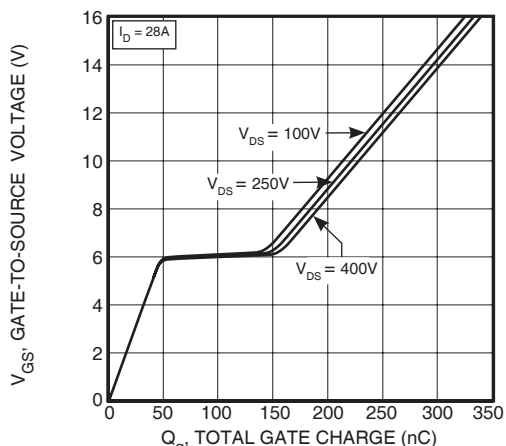

Figure 6, Capacitance vs Drain-to-Source Voltage
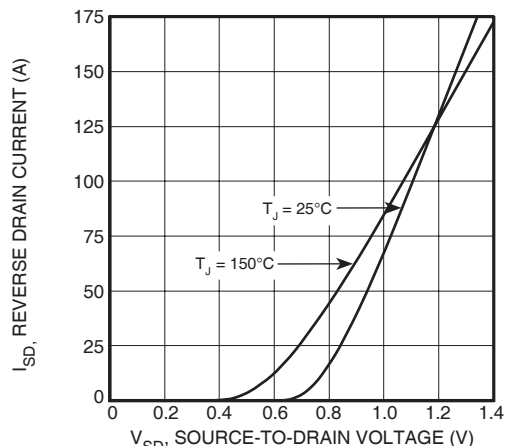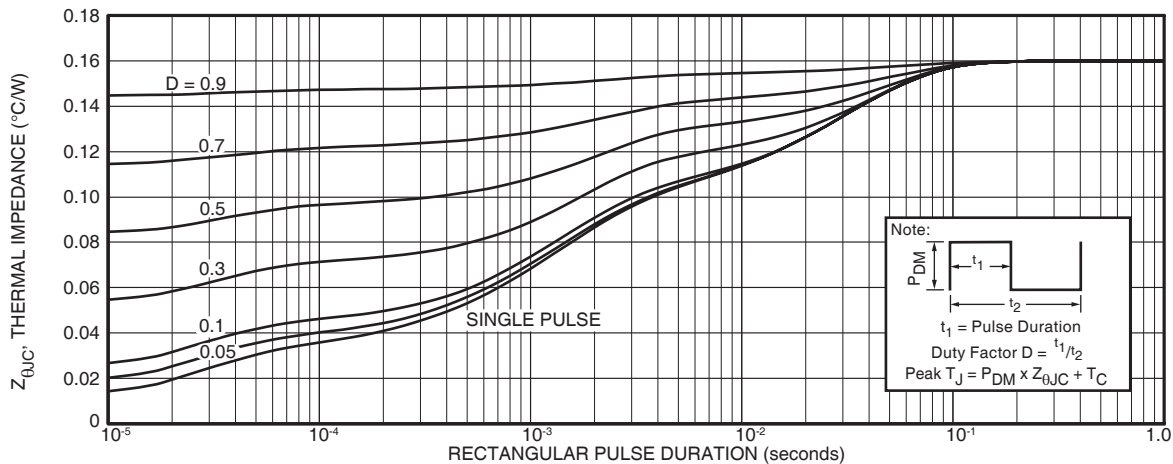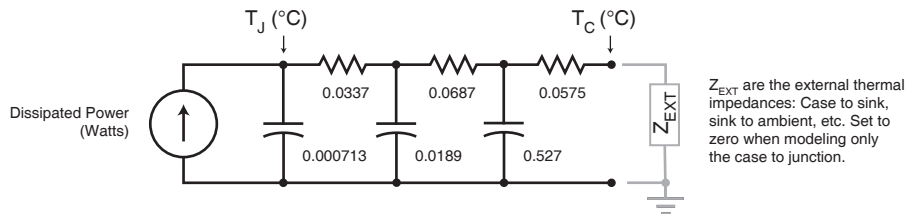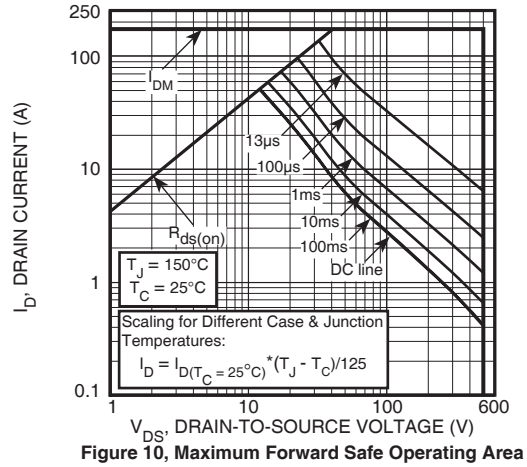

Figure 7, Gate Charge vs Gate-to-Source Voltage

Figure 8, Reverse Drain Current vs Source-to-Drain Voltage

Figure 9, Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

I_{DM}

13µs

100µs

1ms

10ms

100ms

DC line

$R_{ds(on)}$

$T_J = 125°C$
$T_C = 75°C$

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

Figure 10, Maximum Forward Safe Operating Area

I_D, DRAIN CURRENT (A)

I_{DM}

13µs

100µs

1ms

10ms

100ms

DC line

$R_{ds(on)}$

$T_J = 150°C$
$T_C = 25°C$

Scaling for Different Case & Junction Temperatures:

$$I_D = I_{D(T_C = 25°C)} {}^*(T_J - T_C)/125$$

V_{DS}, DRAIN-TO-SOURCE VOLTAGE (V)

T_J (°C) T_C (°C)

0.0337   0.0687   0.0575

Dissipated Power (Watts)

Z_{EXT}

0.000713   0.0189   0.527

Z_{EXT} are the external thermal impedances: Case to sink, sink to ambient, etc. Set to zero when modeling only the case to junction.

Figure 11, Transient Thermal Impedance Model

$Z_{\theta JC}$, THERMAL IMPEDANCE (°C/W)

D = 0.9
0.7
0.5
0.3
0.1
0.05

SINGLE PULSE

Note:

P_{DM}

t_1

t_2

t_1 = Pulse Duration

Duty Factor D = ${}^{t_1}/t_2$

Peak $T_J = P_{DM} \times Z_{\theta JC} + T_C$

RECTANGULAR PULSE DURATION (seconds)

Figure 12. Maximum Effective Transient Thermal Impedance Junction-to-Case vs Pulse Duration

T-MAX™ (B2) Package Outline

TO-264 (L) Package Outline

(e3) 100% Sn Plated

T-MAX™ (B2) Package Outline

Drain

4.69 (.185)
5.31 (.209)

1.49 (.059)
2.49 (.098)

15.49 (.610)
16.26 (.640)

5.38 (.212)
6.20 (.244)

20.80 (.819)
21.46 (.845)

2.87 (.113)
3.12 (.123)

1.65 (.065)
2.13 (.084)

4.50 (.177) Max.

0.40 (.016)
0.79 (.031)

19.81 (.780)
20.32 (.800)

1.01 (.040)
1.40 (.055)

Gate
Drain
Source

2.21 (.087)
2.59 (.102)

5.45 (.215) BSC
2-Plcs.

These dimensions are equal to the TO-247 without the mounting hole.

Dimensions in Millimeters and (Inches)

TO-264 (L) Package Outline

Drain

4.60 (.181)
5.21 (.205)

1.80 (.071)
2.01 (.079)

19.51 (.768)
20.50 (.807)

3.10 (.122)
3.48 (.137)

5.79 (.228)
6.20 (.244)

25.48 (1.003)
26.49 (1.043)

2.29 (.090)
2.69 (.106)

2.29 (.090)
2.69 (.106)

0.48 (.019)
0.84 (.033)
2.59 (.102)
3.00 (.118)

19.81 (.780)
21.39 (.842)

0.76 (.030)
1.30 (.051)
2.79 (.110)
3.18 (.125)

Gate
Drain
Source

5.45 (.215) BSC
2-Plcs.

Dimensions in Millimeters and (Inches)