

# APW6021



## Advanced PWM and Triple Linear Power Controllers

### Functional

- 4 Regulated Voltages are provided
  - Microprocessor Core (1.3V to 3.5V)
  - AGP Bus (1.5V or 3.3V)
  - Memory (1.8V)
  - GTL Bus (1.5V)
- Linear Controllers Drives with both MOSFET and Bipolar Series Pass Transistors
- Fixed or Externally Resistor-Adjustable Linear Outputs (FIX Pin)
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast PWM Converter Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Ratio
- Excellent Output Voltage Regulation
  - Core PWM Output:  $\pm 1\%$  Over Temperature
  - Other Outputs:  $\pm 3\%$  Over Temperature
- TTL-Compatible 5- Bit DAC Microprocessor Core Output Voltage Selection
  - Wide Range -  $1.3V_{DC}$  to  $3.5V_{DC}$
- Power-Good Output Voltage Monitor
- Over-Voltage and Over-Current Fault Monitors
  - Switching Regulator Does Not Require Extra Current Sensing Element, Uses MOSFET's  $r_{DS(ON)}$
- Small Converter Size
  - Constant Frequency Operation
  - 200kHz Free-Running Oscillator; Programmable From 50kHz to Over 1MHz

### Applications

- Motherboard Power Regulation for Computers

### General Description

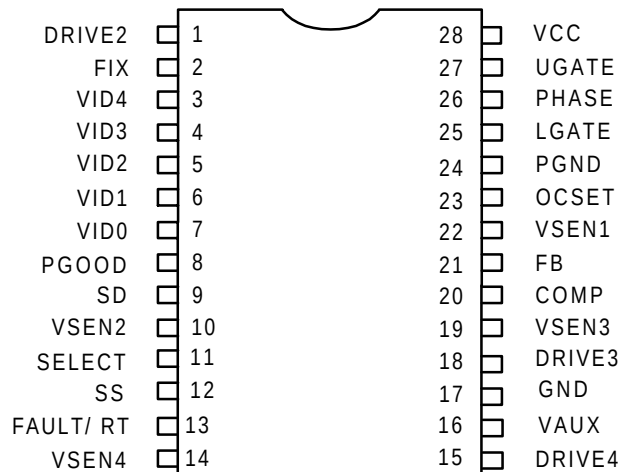
The APW6021 provides the power control and protection for four output voltages in high-performance, graphics intensive microprocessor and computer applications. The IC integrates voltage-mode PWM controller and three linear controllers, as well as the monitoring and protection functions into a 28-pin SOIC package. The PWM controller regulates the microprocessor core voltage with a synchronous-rectified buck converter. The linear controllers regulate the computer system's AGP 1.5V or 3.3V bus power, the 1.5V GTL bus power, and the 1.8V power for the North/South Bridge core voltage and/or cache memory circuits. The APW6021 includes an Intel-compatible, TTL 5-input digital-to-analog converter (DAC) that adjusts the core PWM output voltage from  $1.3V_{DC}$  to  $2.05V_{DC}$  in 0.05V steps and from  $2.1V_{DC}$  to  $3.5V_{DC}$  in 0.1V increments. The precision reference and voltage-mode control provide  $\pm 1\%$  static regulation. The AGP bus power linear controller's output ( $V_{OUT2}$ ) is user-selectable, through a TTL-compatible signal applied at the SELECT pin, for levels of 1.5V or 3.3V with  $\pm 3\%$  accuracy. Based on the status of the FIX pin, the other two linear regulators provide either fixed output voltages of  $1.5V \pm 3\%$  ( $V_{OUT3}$ ) and  $1.8V \pm 3\%$  ( $V_{OUT4}$ ), or user-adjustable by means of an external resistor divider. All linear controllers can employ either N-channel MOSFETs or bipolar NPNs for the pass transistor.

The APW6021 monitors all the output voltages. A single Power Good signal is issued when the core is within  $\pm 10\%$  of the DAC setting and all other outputs are above their under-voltage levels. Additional built-in over-voltage protection for the core output uses the lower MOSFET to prevent output voltages above 115% of the DAC setting. The PWM controller's over-current function monitors the output current by using the voltage drop across the upper MOSFET's  $r_{DS(ON)}$ .

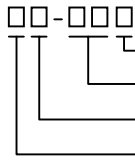
ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.



## Pin Description



## Ordering Information

|                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                             |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>APW 6021</p>  <p>             □□-□□□<br/>             Lead Free Code<br/>             Handling Code<br/>             Temp. Range<br/>             Package Code         </p> | <p>             Package Code<br/>             K : SOP - 28<br/>             Temp. Range<br/>             C : 0 to 70 °C<br/>             Handling Code<br/>             TU : Tube      TR : Tape &amp; Reel<br/>             Lead Free Code<br/>             L : Lead Free Device      Blank : Original Device         </p> |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

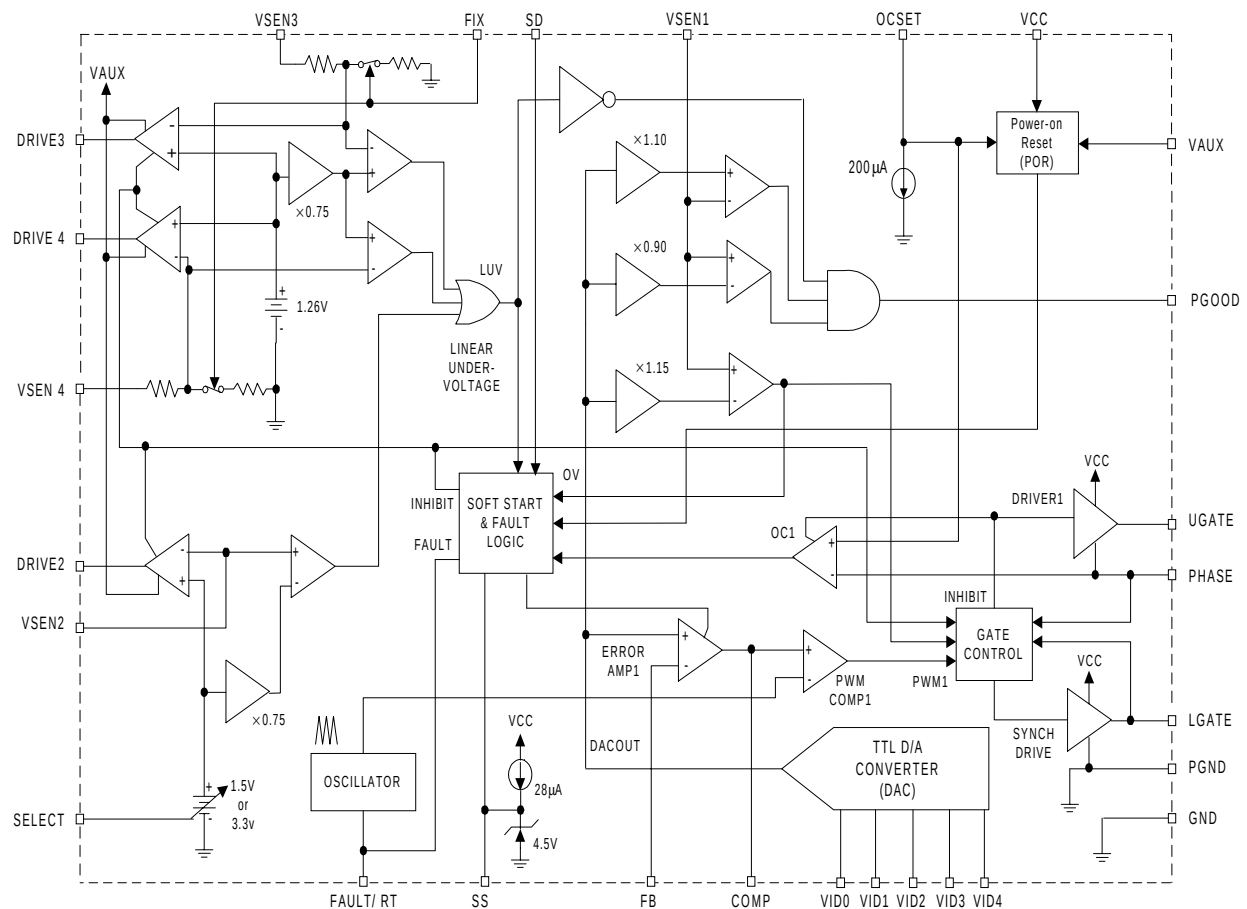
## Absolute Maximum Ratings

| Symbol                 | Parameter                           | Rating                      | Unit |
|------------------------|-------------------------------------|-----------------------------|------|
| $V_{CC}$               | Supply Voltage                      | 15                          | V    |
| $V_{BOOT} - V_{PHASE}$ | Boot Voltage                        | 15                          | V    |
| $V_I, V_O$             | Input , Output or I/O Voltage       | GND -0.3 V to $V_{CC} +0.3$ | V    |
| $T_A$                  | Operating Ambient Temperature Range | 0 to 70                     | °C   |
| $T_J$                  | Junction Temperature Range          | 0 to 125                    | °C   |
| $T_{STG}$              | Storage Temperature Range           | -65 to +150                 | °C   |
| $T_S$                  | Soldering Temperature               | 300 ,10 seconds             | °C   |

## Thermal Characteristics

| Symbol          | Parameter                                                                        | Value    | Unit |
|-----------------|----------------------------------------------------------------------------------|----------|------|
| $R_{\theta JA}$ | Thermal Resistance in Free Air<br>SOIC<br>SOIC (with 3in <sup>2</sup> of Copper) | 75<br>65 | °C/W |

## Block Diagram



## Electrical Characteristics

(Recommended operating conditions, Unless otherwise noted) Refer to Block and Simplified Power System Diagrams, and Typical Application Schematic

| Symbol                                   | Parameter                             | Test Conditions                               | APW6021 |       |      | Unit             |
|------------------------------------------|---------------------------------------|-----------------------------------------------|---------|-------|------|------------------|
|                                          |                                       |                                               | Min.    | Typ.  | Max. |                  |
| V <sub>CC</sub> Supply Current           |                                       |                                               |         |       |      |                  |
| I <sub>CC</sub>                          | Nominal Supply Current                | UGATE, LGATE, DRIVE2, DRIVE3, and DRIVE4 open |         | 9     |      | mA               |
| Power-on Reset                           |                                       |                                               |         |       |      |                  |
|                                          | Rising VCC Threshold                  | Vocset=4.5V                                   |         |       | 10.4 | V                |
|                                          | Falling VCC Threshold                 | Vocset=4.5V                                   | 8.2     |       |      | V                |
|                                          | Rising VAUX Threshold                 | Vocset=4.5V                                   |         | 2.5   |      | V                |
|                                          | VAUX Threshold Hysteresis             | Vocset=4.5V                                   |         | 0.5   |      | V                |
|                                          | Rising V <sub>OCSET</sub> Threshold   |                                               |         | 1.26  |      | V                |
| Oscillator                               |                                       |                                               |         |       |      |                  |
| F <sub>OCS</sub>                         | Free Running Frequency                | RT= Open                                      | 185     | 200   | 215  | kHz              |
| ΔV <sub>OSC</sub>                        | Ramp Amplitude                        | RT= Open                                      |         | 1.9   |      | V <sub>P-P</sub> |
| DAC and Bandgap Reference                |                                       |                                               |         |       |      |                  |
|                                          | DAC(VID0-VID4) Input Low Voltage      |                                               |         |       | 0.8  | V                |
|                                          | DAC(VID0-VID4) Input High Voltage     |                                               | 2.0     |       | 0.8  | V                |
|                                          | DACOUT Voltage accuracy               |                                               | -1.0    |       | +1.0 | %                |
| V <sub>BG</sub>                          | Bandgap Reference Voltage             |                                               |         | 1.265 |      | V                |
|                                          | Bandgap Reference Tolerance           |                                               | -2.5    |       | +2.5 | %                |
| Linear Regulators (OUT2, OUT3, and OUT4) |                                       |                                               |         |       |      |                  |
|                                          | Regulation (All Linears)              |                                               |         | 3     |      | %                |
| VREG <sub>2</sub>                        | VSEN2 Regulation Voltage              | Select < 0.8V                                 |         | 1.5   |      | V                |
| VREG <sub>2</sub>                        | VSEN2 Regulation Voltage              | Select > 2.0V                                 |         | 3.3   |      | V                |
| VREG <sub>3</sub>                        | VSEN3 Regulation Voltage              |                                               |         | 1.5   |      | V                |
| VREG <sub>4</sub>                        | VSEN4 Regulation Voltage              |                                               |         | 1.8   |      | V                |
| VREN <sub>UV</sub>                       | Under-Voltage Level (VSEN/ VREG)      | VSEN Rising                                   |         | 75    |      | %                |
|                                          | Under-Voltage Hysteresis (VSEN/ VREG) | VSEN Falling                                  |         | 7     |      | %                |
|                                          | Output Drive Current (All Liners)     | VAUX-V <sub>DRIVE</sub> >0.6V                 | 20      | 40    |      | mA               |

## Electrical Characteristics Cont.

| Symbol                                     | Parameter                            | Test Conditions                              | APW6021 |      |      | Unit |
|--------------------------------------------|--------------------------------------|----------------------------------------------|---------|------|------|------|
|                                            |                                      |                                              | Min.    | Typ. | Max. |      |
| Synchronous PWM Controller Error Amplifier |                                      |                                              |         |      |      |      |
|                                            | DC Gain                              |                                              |         | 88   |      | dB   |
| GBWP                                       | Gain-Bandwidth Product               |                                              |         | 15   |      | MHz  |
| SR                                         | Slew Rate                            | COMP=10pF                                    |         | 6    |      | V/μs |
| PWM Controller Gate Driver                 |                                      |                                              |         |      |      |      |
| I <sub>UGATE</sub>                         | UGATE Source                         | V <sub>CC</sub> =12V, V <sub>UGATE</sub> =6V |         | 1    |      | A    |
| R <sub>UGATE</sub>                         | UGATE Sink                           | V <sub>UGATE1-PHASE</sub> =1V                |         |      | 3.5  | Ω    |
| I <sub>LGATE</sub>                         | LGATE Source                         | V <sub>CC</sub> =12V, V <sub>LGATE</sub> =1V |         | 1    |      | A    |
| R <sub>LGATE</sub>                         | LGATE Sink                           | V <sub>LGATE</sub> = 1V                      |         |      | 3    | Ω    |
| Protection                                 |                                      |                                              |         |      |      |      |
|                                            | VSEN1 Over-Voltage (VSEN1/DACOUT)    | VSEN1 Rising                                 |         | 115  | 120  | %    |
| I <sub>OVP</sub>                           | FAULT Souring Current                | V <sub>FAULT/RT</sub> =2.0V                  |         | 8.5  |      | mA   |
| I <sub>OCSET</sub>                         | OCSET1 Current Source                | V <sub>OCSET</sub> = 4.5V <sub>DC</sub>      | 170     | 200  | 230  | μA   |
| I <sub>SS</sub>                            | Soft Start Current                   |                                              |         | 28   |      | μA   |
| Power Good                                 |                                      |                                              |         |      |      |      |
|                                            | VSEN1 Upper Threshold (VSEN1/DACOUT) | VSEN1 Rising                                 | 108     |      | 110  | %    |
|                                            | VSEN1 Under Voltage (VSEN1/DACOUT)   | VSEN1 Rising                                 | 92      |      | 94   | %    |
|                                            | VSEN1 Hysteresis (VSEN1 /DACOUT)     | Upper /Lower Threshold                       |         | 2    |      | %    |
| V <sub>PGOOD</sub>                         | PGOOD Voltage Low                    | I <sub>PGOOD</sub> = -4mA                    |         |      | 0.8  | V    |

## Functional Pin Description

### DRIVE2 (Pin 1)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the AGP regulator's pass transistor.

nal resistor divider connected at the corresponding VSEN pin. The new output voltage set by the external resistor divider can be determined using the following formula:

$$V_{OUT} = 1.265V \times [1 + R_{OUT} / R_{GND}]$$

### FIX (Pin 2)

Grounding this pin bypasses the internal resistor dividers that set the output voltage of the 1.5V and 1.8V linear regulators. This way, the output voltage of the two regulators can be adjusted from 1.26V up to the input voltage (+3.3V or +5V) by way of an exter-

where R<sub>OUT</sub> is the resistor connected from VSEN to the output of the regulator, and R<sub>GND</sub> is the resistor connected from VSEN to ground. Left open, the FIX pin is pulled high, enabling fixed output voltage operation.

## Functional Pin Description Cont.

### VID4, VID3, VID2, VID1, VID0 (Pins 3, 4, 5, 6 and 7)

VID0-4 are the TTL-compatible input pins to the 5-bit DAC. The logic states of these five pins program the internal voltage reference (DACOUT). The level of DACOUT sets the microprocessor core converter output voltage, as well as the corresponding PGOOD and OVP thresholds.

### PGOOD (Pin 8)

PGOOD is an open collector output used to indicate the status of the output voltages. This pin is pulled low when the synchronous regulator output is not within  $\pm 10\%$  of the DACOUT reference voltage or when any of the other outputs are below their under-voltage thresholds.

The PGOOD output is open for "11111" VID code.

### SD (Pin 9)

This pin shuts down all the outputs. A TTL-compatible, logic level high signal applied at this pin immediately discharges the soft-start capacitor, disabling all the outputs. Dedicated internal circuitry insures the core output voltage does not go negative during this process. When re-enabled, the IC undergoes a new soft-start cycle. Left open, this pin is pulled low by an internal pull-down resistor, enabling operation.

### VSEN2 (Pin 10)

Connect this pin to the output of the AGP linear regulator. The voltage at this pin is regulated to the level predetermined by the logic-level status of the SELECT pin. This pin is also monitored for under-voltage events.

### SELECT (Pin 11)

This pin determines the output voltage of the AGP bus linear regulator. A low TTL input sets the output voltage to 1.5V, while a high input sets the output voltage to 3.3V.

### SS (Pin 12)

Connect a capacitor from this pin to ground. This capacitor, along with an internal 28 $\mu$ A current source, sets the soft-start interval of the converter.

### FAULT / RT (Pin 13)

This pin provides oscillator switching frequency adjustment. By placing a resistor ( $R_T$ ) from this pin to GND, the nominal 200kHz switching frequency is increased according to the following equation:

$$F_s = 200\text{kHz} + 5 \times 10^6 / R_T \text{ (k}\Omega\text{)} \quad (R_T \text{ to GND})$$

Conversely, connecting a resistor from this pin to VCC reduces the switching frequency according to the following equation:

$$F_s = 200\text{kHz} + 4 \times 10^7 / R_T \text{ (k}\Omega\text{)} \quad (R_T \text{ to 12V})$$

Nominally, the voltage at this pin is 1.26V. In the event of an over-voltage or over-current condition, this pin is internally pulled to VCC.

### VSEN4 (Pin 14)

Connect this pin to the output of the linear 1.8V regulator. This pin is monitored for undervoltage events.

### DRIVE4 (Pin 15)

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.8V regulator's pass transistor.

### VAUX (Pin 16)

This pin provides boost current for the linear regulators' output drives in the event bipolar NPN transistors (instead of N-channel MOSFETs) are employed as pass elements. The voltage at this pin is monitored for power-on reset (POR) purposes.

### GND (Pin 17)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

## **Functional Pin Description Cont.**

### **DRIVE3 (Pin 18)**

Connect this pin to the gate of an external MOSFET. This pin provides the drive for the 1.5V regulator's pass transistor.

### **VSEN3 (Pin 19)**

Connect this pin to the output of the 1.5V linear regulator. This pin is monitored for under-voltage events.

### **COMP and FB (Pin 20, and 21)**

COMP and FB are the available external pins of the PWM converter error amplifier. The FB pin is the inverting input of the error amplifier. Similarly, the COMP pin is the error amplifier output. These pins are used to compensate the voltage-mode control feedback loop of the synchronous PWM converter.

### **VSEN1 (Pin 22)**

This pin is connected to the PWM converter's output voltage. The PGOOD and OVP comparator circuits use this signal to report output voltage status and for over-voltage protection.

### **OCSET (Pin 23)**

Connect a resistor from this pin to the drain of the respective upper MOSFET. This resistor, an internal 200 $\mu$ A current source, and the upper MOSFET's on-resistance set the converter over-current trip point. An over-current trip cycles the soft-start function.

The voltage at this pin is monitored for power-on reset (POR) purposes and pulling this pin low with an open drain device will shutdown the IC.

### **PGND (Pin 24)**

This is the power ground connection. Tie the synchronous PWM converter's lower MOSFET source to this pin.

### **LGATE (Pin 25)**

Connect LGATE to the PWM converter's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.

### **PHASE (Pin 26)**

Connect the PHASE pin to the PWM converter's upper MOSFET source. This pin represents the gate drive return current path and is used to monitor the voltage drop across the upper MOSFET for over-current protection.

### **UGATE (Pin 27)**

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

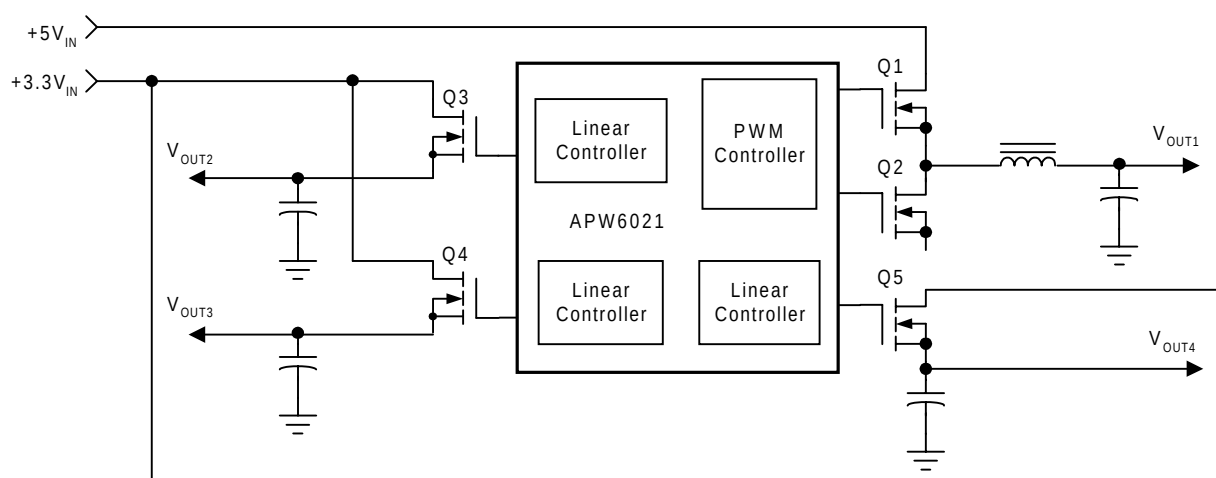
### **VCC (Pin 28)**

Provide a 12V bias supply for the IC to this pin. This pin also provides the gate bias charge for all the MOSFETs controlled by the IC. The voltage at this pin is monitored for Power-On Reset (POR) purposes.

## Table 1 Output Voltage Program

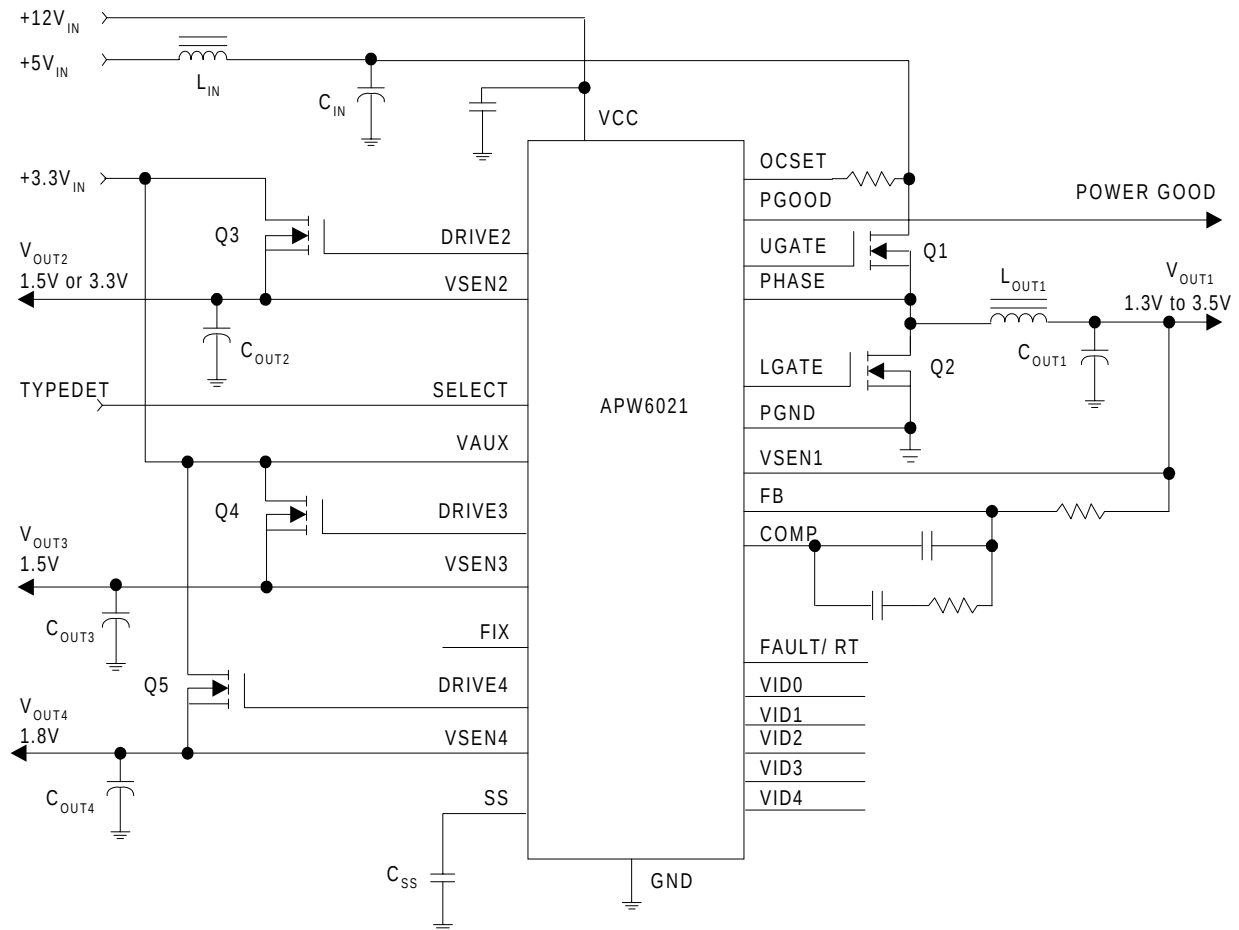
| Pin Name |      |      |      |      | Nominal Output<br>Voltage Dacout | Pin Name |      |      |      |      | Nominal Output<br>Voltage Dacout |
|----------|------|------|------|------|----------------------------------|----------|------|------|------|------|----------------------------------|
| VID4     | VID3 | VID2 | VID1 | VID0 |                                  | VID4     | VID3 | VID2 | VID1 | VID0 |                                  |
| 0        | 1    | 1    | 1    | 1    | 1.3                              | 1        | 1    | 1    | 1    | 1    | 0                                |
| 0        | 1    | 1    | 1    | 0    | 1.35                             | 1        | 1    | 1    | 1    | 0    | 2.1                              |
| 0        | 1    | 1    | 0    | 1    | 1.4                              | 1        | 1    | 1    | 0    | 1    | 2.2                              |
| 0        | 1    | 1    | 0    | 0    | 1.45                             | 1        | 1    | 1    | 0    | 0    | 2.3                              |
| 0        | 1    | 0    | 1    | 1    | 1.5                              | 1        | 1    | 0    | 1    | 1    | 2.4                              |
| 0        | 1    | 0    | 1    | 0    | 1.55                             | 1        | 1    | 0    | 1    | 0    | 2.5                              |
| 0        | 1    | 0    | 0    | 1    | 1.6                              | 1        | 1    | 0    | 0    | 1    | 2.6                              |
| 0        | 1    | 0    | 0    | 0    | 1.65                             | 1        | 1    | 0    | 0    | 0    | 2.7                              |
| 0        | 0    | 1    | 1    | 1    | 1.7                              | 1        | 0    | 1    | 1    | 1    | 2.8                              |
| 0        | 0    | 1    | 1    | 0    | 1.75                             | 1        | 0    | 1    | 1    | 0    | 2.9                              |
| 0        | 0    | 1    | 0    | 1    | 1.8                              | 1        | 0    | 1    | 0    | 1    | 3.0                              |
| 0        | 0    | 1    | 0    | 0    | 1.85                             | 1        | 0    | 1    | 0    | 0    | 3.1                              |
| 0        | 0    | 0    | 1    | 1    | 1.90                             | 1        | 0    | 0    | 1    | 1    | 3.2                              |
| 0        | 0    | 0    | 1    | 0    | 1.95                             | 1        | 0    | 0    | 1    | 0    | 3.3                              |
| 0        | 0    | 0    | 0    | 1    | 2.00                             | 1        | 0    | 0    | 0    | 1    | 3.4                              |
| 0        | 0    | 0    | 0    | 0    | 2.05                             | 1        | 0    | 0    | 0    | 0    | 3.5                              |

## Simplified Power System Diagram



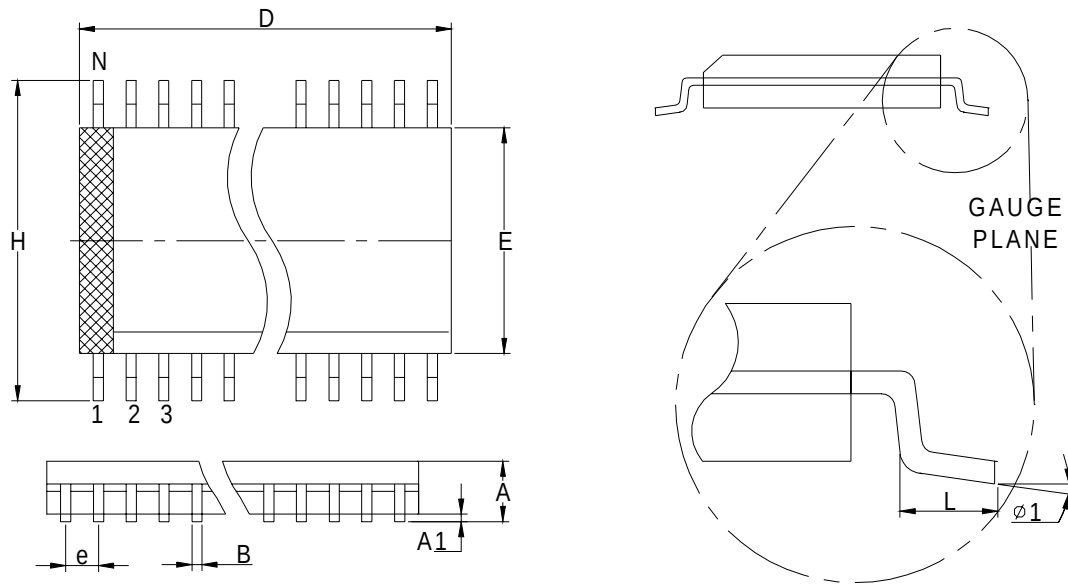


## Typical Application



## Package Information

SO – 300mil ( Reference JEDEC Registration MS-013)

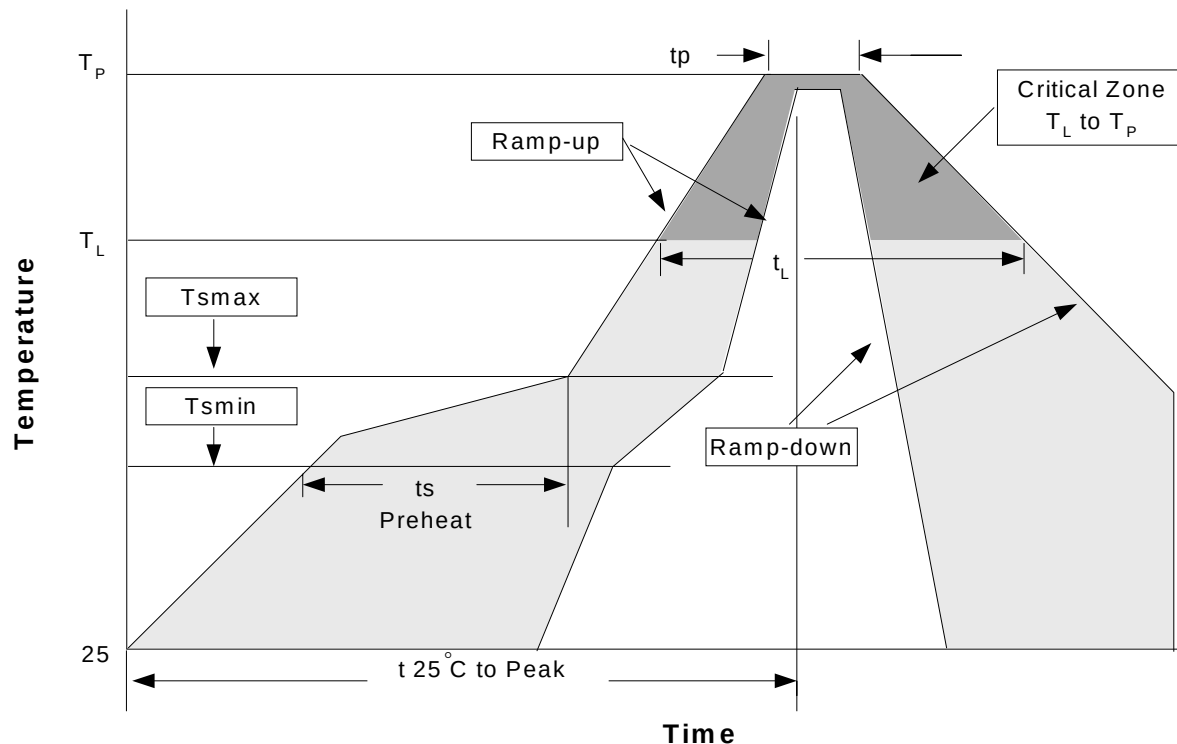


| Dim | Millimeters    |       | Variations- D |       |       | Dim | Inches         |        | Variations- D |       |       |
|-----|----------------|-------|---------------|-------|-------|-----|----------------|--------|---------------|-------|-------|
|     | Min.           | Max.  | Variations    | Min.  | Max.  |     | Min.           | Max.   | Variations    | Min.  | Max.  |
| A   | 2.35           | 2.65  | SO-16         | 10.10 | 10.50 | A   | 0.093          | 0.1043 | SO-16         | 0.398 | 0.413 |
| A1  | 0.10           | 0.30  | SO-18         | 11.35 | 11.76 | A1  | 0.004          | 0.0120 | SO-18         | 0.447 | 0.463 |
| B   | 0.33           | 0.51  | SO-20         | 12.60 | 13    | B   | 0.013          | 0.020  | SO-20         | 0.496 | 0.512 |
| D   | See variations |       | SO-24         | 15.20 | 15.60 | D   | See variations |        | SO-24         | 0.599 | 0.614 |
| E   | 7.40           | 7.60  | SO-28         | 17.70 | 18.11 | E   | 0.2914         | 0.2992 | SO-28         | 0.697 | 0.713 |
| e   | 1.27BSC        |       | SO-14         | 8.80  | 9.20  | e   | 0.050BSC       |        | SO-14         | 0.347 | 0.362 |
| H   | 10             | 10.65 |               |       |       | H   | 0.394          | 0.419  |               |       |       |
| L   | 0.40           | 1.27  |               |       |       | L   | 0.016          | 0.050  |               |       |       |
| N   | See variations |       |               |       |       | N   | See variations |        |               |       |       |
| φ 1 | 0°             | 8°    |               |       |       | φ 1 | 0°             | 8°     |               |       |       |

## Physical Specifications

|                    |                                                                      |
|--------------------|----------------------------------------------------------------------|
| Terminal Material  | Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn |
| Lead Solderability | Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.         |

## Reflow Condition (IR/Convection or VPR Reflow)



## Classification Reflow Profiles

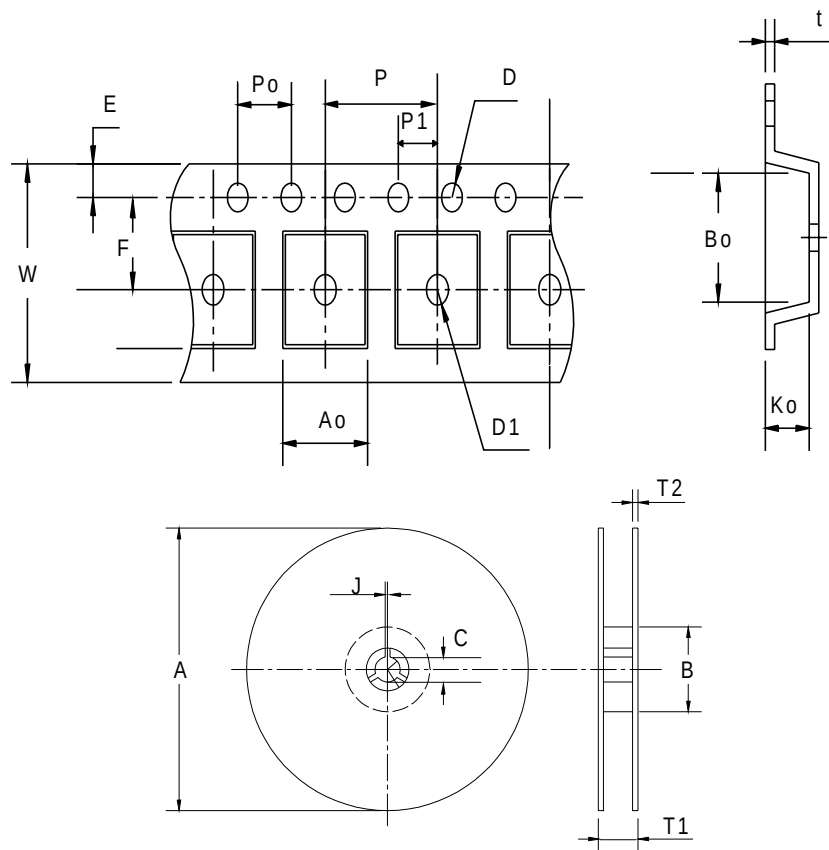
| Profile Feature                                     | Sn-Pb Eutectic Assembly |               | Pb-Free Assembly |               |
|-----------------------------------------------------|-------------------------|---------------|------------------|---------------|
|                                                     | Large Body              | Small Body    | Large Body       | Small Body    |
| Average ramp-up rate ( $T_L$ to $T_P$ )             | 3°C/second max.         |               | 3°C/second max.  |               |
| Preheat                                             |                         |               |                  |               |
| - Temperature Min ( $T_{smin}$ )                    | 100°C                   |               | 150°C            |               |
| - Temperature Mix ( $T_{smax}$ )                    | 150°C                   |               | 200°C            |               |
| - Time (min to max)( $t_s$ )                        | 60-120 seconds          |               | 60-180 seconds   |               |
| $T_{smax}$ to $T_L$                                 |                         |               | 3°C/second max   |               |
| - Ramp-up Rate                                      |                         |               |                  |               |
| $T_{smax}$ to $T_L$                                 |                         |               |                  |               |
| - Temperature( $T_L$ )                              | 183°C                   |               | 217°C            |               |
| - Time ( $t_L$ )                                    | 60-150 seconds          |               | 60-150 seconds   |               |
| Peak Temperature( $T_p$ )                           | 225 +0/-5°C             | 240 +0/-5°C   | 245 +0/-5°C      | 250 +0/-5°C   |
| Time within 5°C of actual Peak Temperature( $t_p$ ) | 10-30 seconds           | 10-30 seconds | 10-30 seconds    | 20-40 seconds |
| Ramp-down Rate                                      | 6°C/second max.         |               | 6°C/second max.  |               |
| Time 25°C to Peak Temperature                       | 6 minutes max.          |               | 8 minutes max.   |               |

Note: All temperatures refer to topside of the package. Measured on the body surface.

## Reliability test program

| Test item     | Method              | Description               |
|---------------|---------------------|---------------------------|
| SOLDERABILITY | MIL-STD-883D-2003   | 245°C , 5 SEC             |
| HOLT          | MIL-STD-883D-1005.7 | 1000 Hrs Bias @ 125 °C    |
| PCT           | JESD-22-B, A102     | 168 Hrs, 100 % RH , 121°C |
| TST           | MIL-STD-883D-1011.9 | -65°C ~ 150°C, 200 Cycles |
| ESD           | MIL-STD-883D-3015.7 | VHBM > 2KV, VMM > 200V    |
| Latch-Up      | JESD 78             | 10ms , $I_{tr} > 100mA$   |

## Tape & Reel Dimensions



| Application | A          | B        | C           | J         | T1         | T2          | W          | P         | E         |
|-------------|------------|----------|-------------|-----------|------------|-------------|------------|-----------|-----------|
| SOP- 28     | 330±1      | 62 ±1.5  | 12.75 ± 0.5 | 2 ± 0.6   | 24.4 ± 0.2 | 2± 0.2      | 24 ± 0.3   | 12 ± 0.1  | 1.75± 0.1 |
| Application | F          | D        | D1          | Po        | P1         | Ao          | Bo         | Ko        | t         |
| SOP- 28     | 11.5 ± 0.1 | 1.5 +0.1 | 1.5+ 0.25   | 4.0 ± 0.1 | 2.0 ± 0.1  | 10.85 ± 0.1 | 18.34± 0.1 | 2.97± 0.1 | 0.35±0.01 |

(mm)

## Cover Tape Dimensions

| Application | Carrier Width | Cover Tape Width | Devices Per Reel |
|-------------|---------------|------------------|------------------|
| SOP- 28     | 24            | 21.3             | 1000             |

## Customer Service

### Anpec Electronics Corp.

Head Office :

5F, No. 2 Li-Hsin Road, SBIP,

Hsin-Chu, Taiwan, R.O.C.

Tel : 886-3-5642000

Fax : 886-3-5642050

Taipei Branch :

7F, No. 137, Lane 235, Pac Chiao Rd.,

Hsin Tien City, Taipei Hsien, Taiwan, R. O. C.

Tel : 886-2-89191368

Fax : 886-2-89191369