

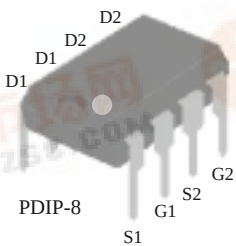
AP2030SD



Advanced Power
Electronics Corp.

N AND P-CHANNEL ENHANCEMENT
MODE POWER MOSFET

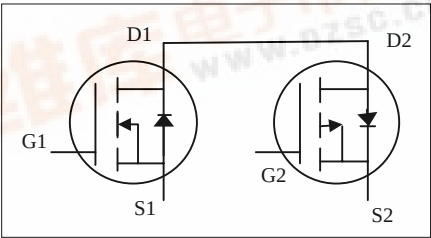
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching



Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

N-CH	BV_{DSS}	20V
	$R_{DS(ON)}$	60mΩ
	I_D	2.6A
P-CH	BV_{DSS}	-20V
	$R_{DS(ON)}$	80mΩ
	I_D	-2.3A



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±12	±12	V
$I_D@T_A=25^{\circ}C$	Continuous Drain Current ³	2.6	-2.3	A
$I_D@T_A=70^{\circ}C$	Continuous Drain Current ³	2.1	-1.8	A
I_{DM}	Pulsed Drain Current ¹	15	-10	A
$P_D@T_A=25^{\circ}C$	Total Power Dissipation	2		W
	Linear Derating Factor	0.016		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	Max. 62.5	°C/W



AP2030SD

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.037	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =4.5V, I _D =2.6A	-	-	60	mΩ
		V _{GS} =2.5V, I _D =1.8A	-	-	90	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	0.5	-	1.2	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =2.6A	-	3.6	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =20V, V _{GS} =0V	-	-	1	uA
	Drain-Source Leakage Current (T _j =150°C)	V _{DS} =16V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±12V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =2.6A	-	9	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =10V	-	1	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	4	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =10V	-	6.5	-	ns
t _r	Rise Time	I _D =1A	-	14	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =4.5V	-	20	-	ns
t _f	Fall Time	R _D =10Ω	-	15	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	300	-	pF
C _{oss}	Output Capacitance	V _{DS} =8V	-	255	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	115	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V, V _S =1.2V	-	-	1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =1.7A, V _{GS} =0V	-	-	1.2	V

**P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	-20	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =-1mA	-	-0.037	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-4.5V, I _D =-2.2A	-	-	80	mΩ
		V _{GS} =-2.5V, I _D =-1.8A	-	-	135	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-0.5	-	-1	V
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-2.2A	-	2.7	-	S
I _{DSS}	Drain-Source Leakage Current (T=25°C)	V _{DS} =-20V, V _{GS} =0V	-	-	-1	uA
	Drain-Source Leakage Current (T=150°C)	V _{DS} =-16V, V _{GS} =0V	-	-	-25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±12V	-	-	±100	nA
Q _g	Total Gate Charge ²	I _D =-2.2A	-	11.5	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =-6V	-	3.2	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =-4.5V	-	1.5	-	nC
t _{d(on)}	Turn-on Delay Time ²	V _{DS} =-10V	-	-	10	ns
t _r	Rise Time	I _D =-2.2A	-	-	25	ns
t _{d(off)}	Turn-off Delay Time	R _G =6Ω, V _{GS} =-4.5V	-	-	50	ns
t _f	Fall Time	R _D =4.5Ω	-	-	30	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	940	-	pF
C _{oss}	Output Capacitance	V _{DS} =-15V	-	440	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	130	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =-1.2V	-	-	-1.7	A
V _{SD}	Forward On Voltage ²	T _j =25°C, I _S =-1.8A, V _{GS} =0V	-	-0.75	-1.2	V

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse width ≤300us , duty cycle ≤2%.

3.Mounted on 1 in² copper pad of FR4 board ; 90°C/W when mounted on Min. copper pad.



N-Channel

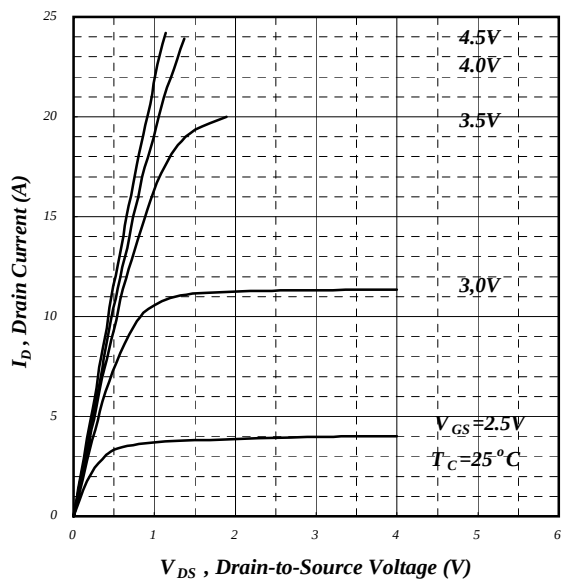


Fig 1. Typical Output Characteristics

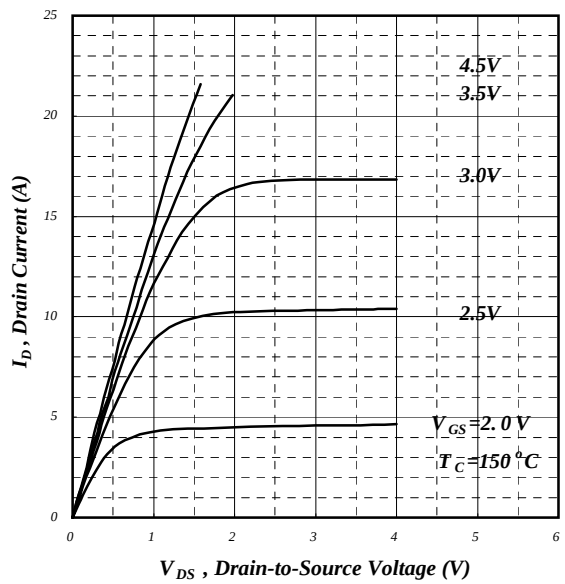


Fig 2. Typical Output Characteristics

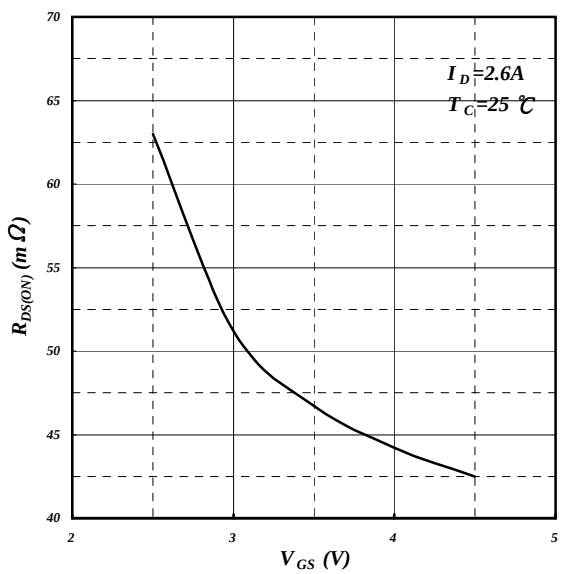


Fig 3. On-Resistance v.s. Gate Voltage

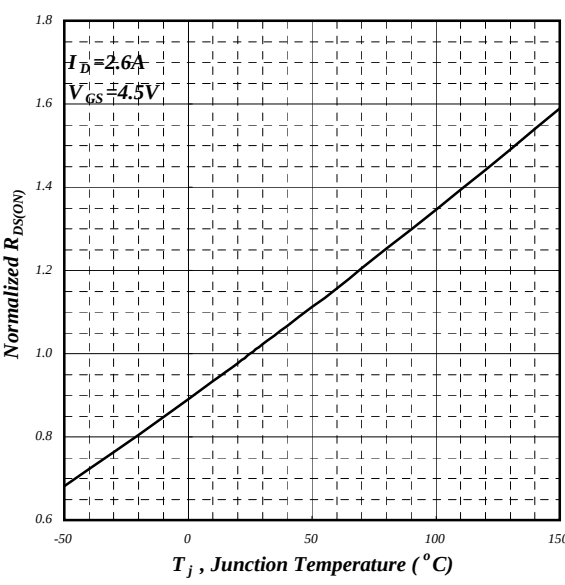


Fig 4. Normalized On-Resistance v.s. Junction Temperature



N-Channel

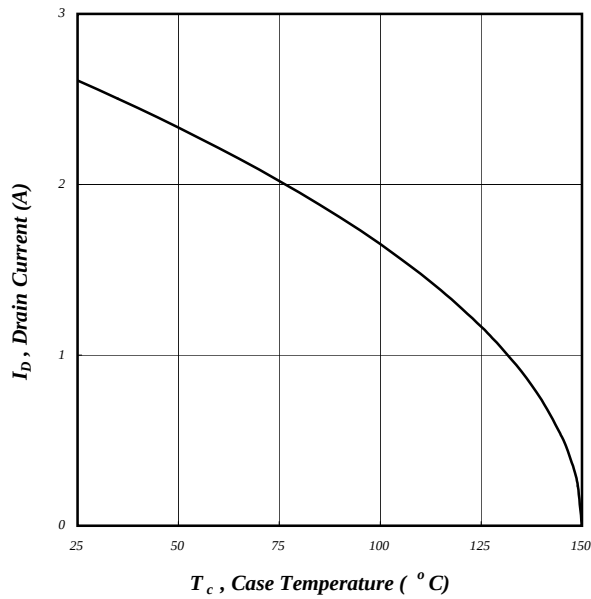


Fig 5. Maximum Drain Current v.s. Case Temperature

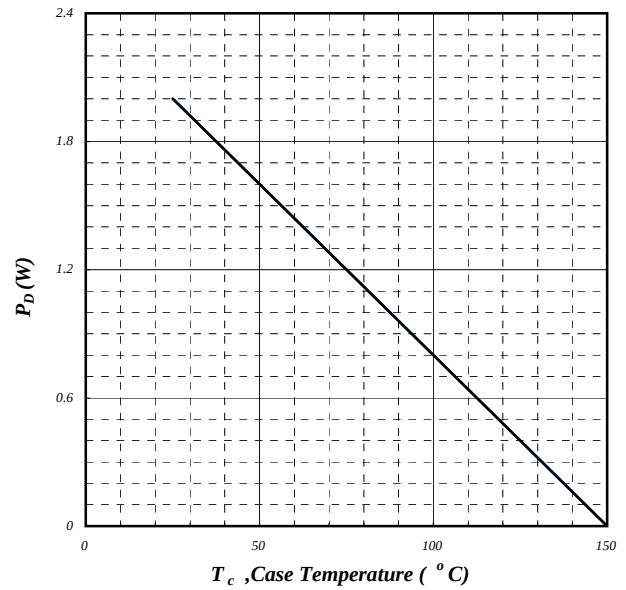


Fig 6. Typical Power Dissipation

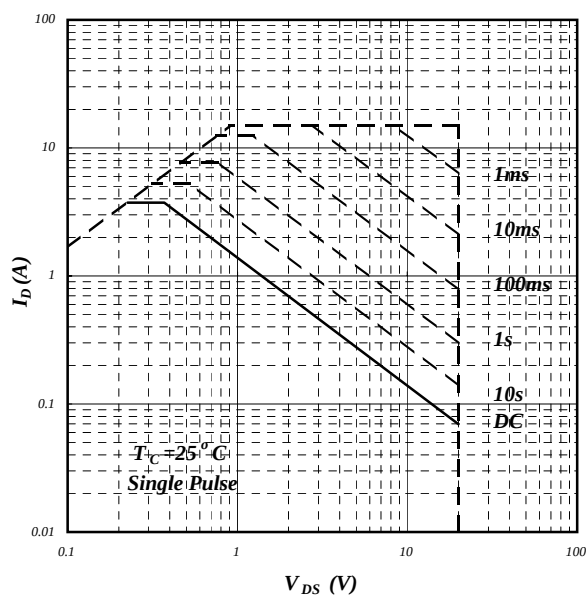


Fig 7. Maximum Safe Operating Area

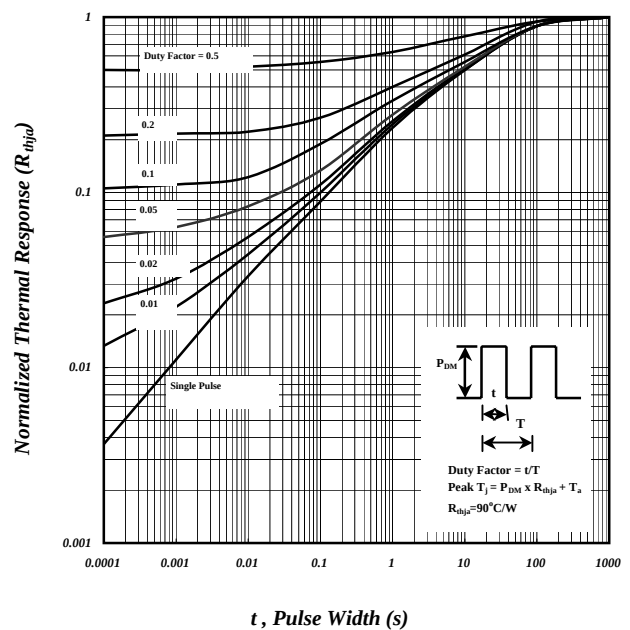


Fig 8. Effective Transient Thermal Impedance



N-Channel

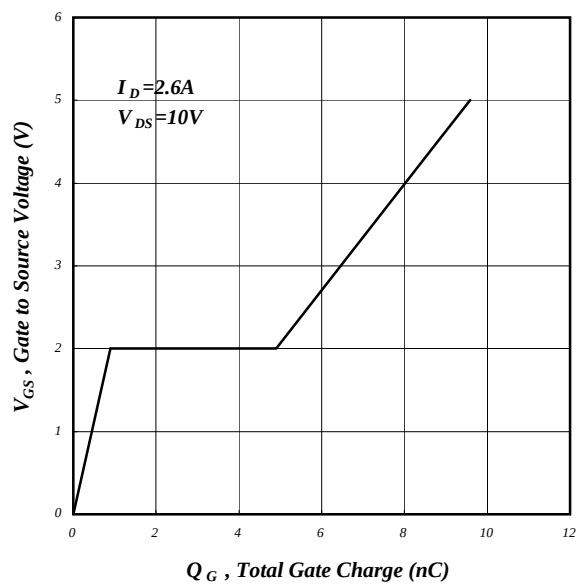


Fig 9. Gate Charge Characteristics

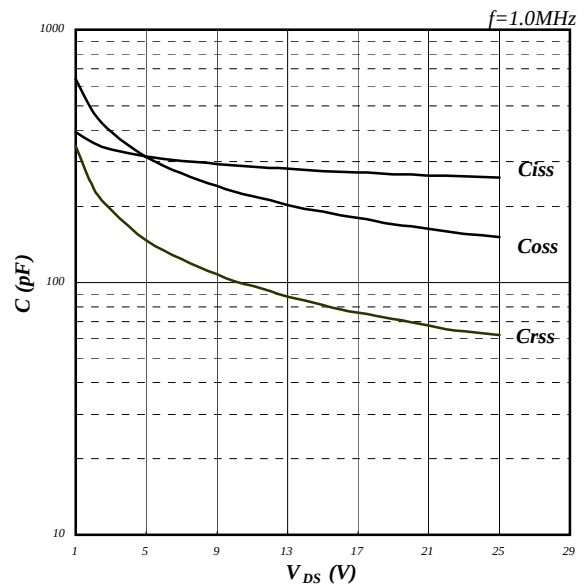


Fig 10. Typical Capacitance Characteristics

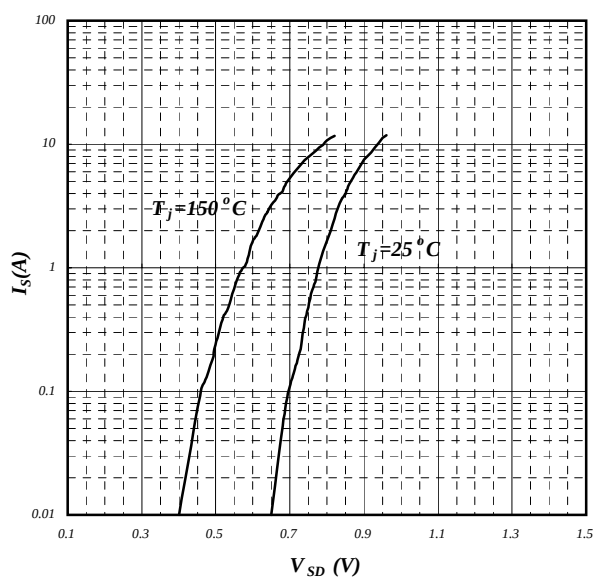


Fig 11. Forward Characteristic of Reverse Diode

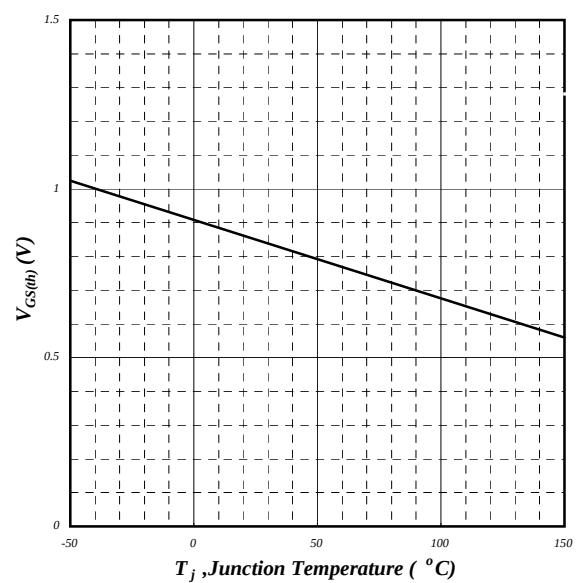


Fig 12. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

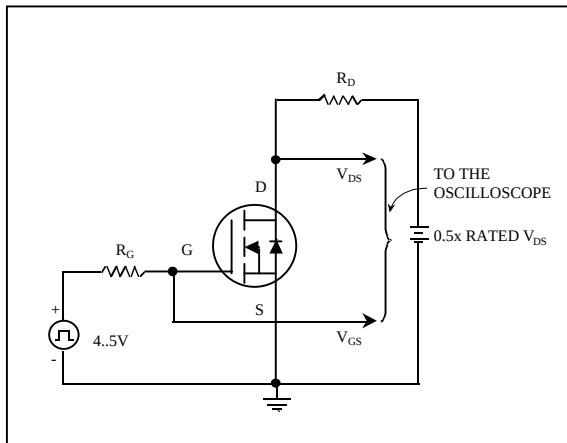


Fig 13. Switching Time Circuit

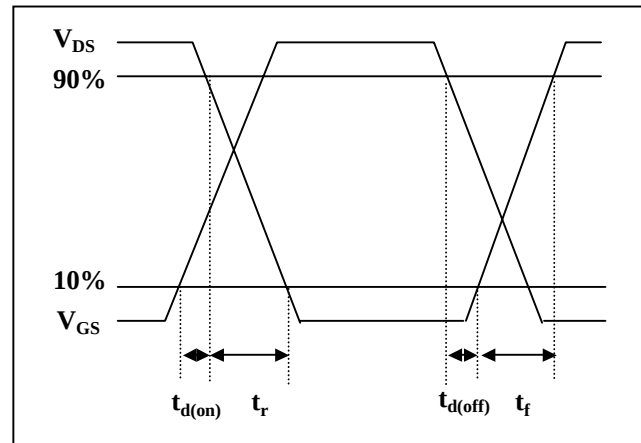


Fig 14. Switching Time Waveform

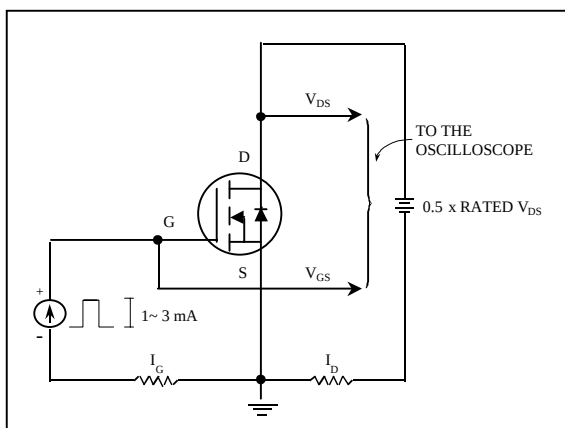


Fig 15. Gate Charge Circuit

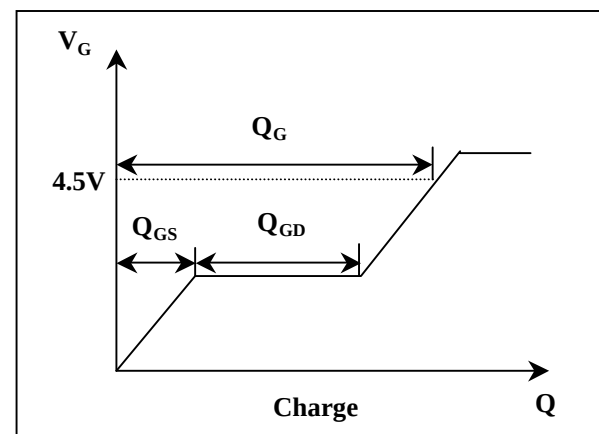


Fig 16. Gate Charge Waveform



P-Channel

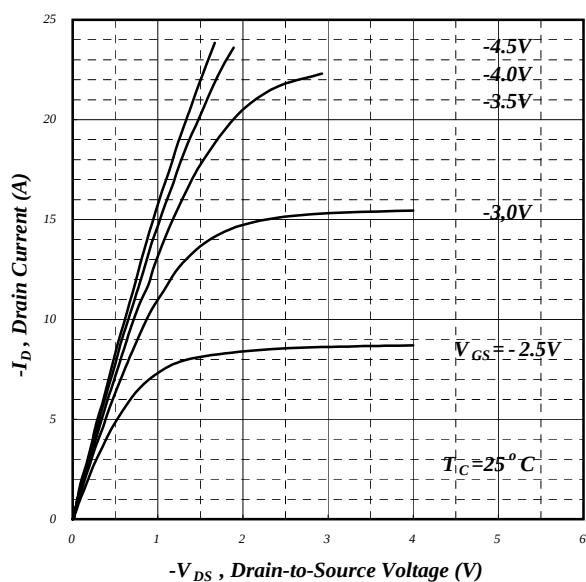


Fig 1. Typical Output Characteristics

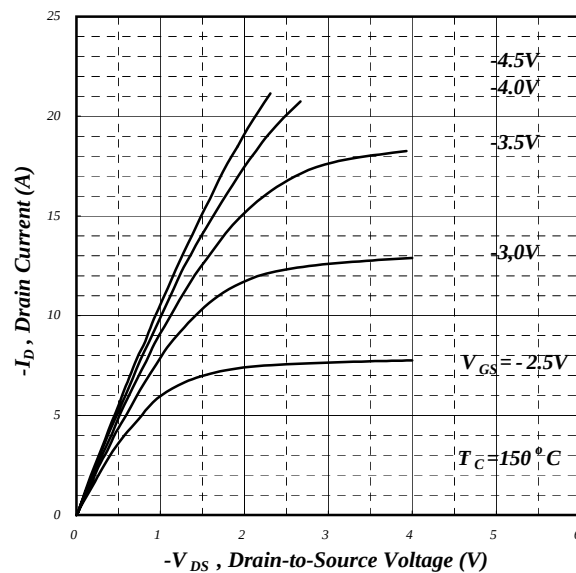


Fig 2. Typical Output Characteristics

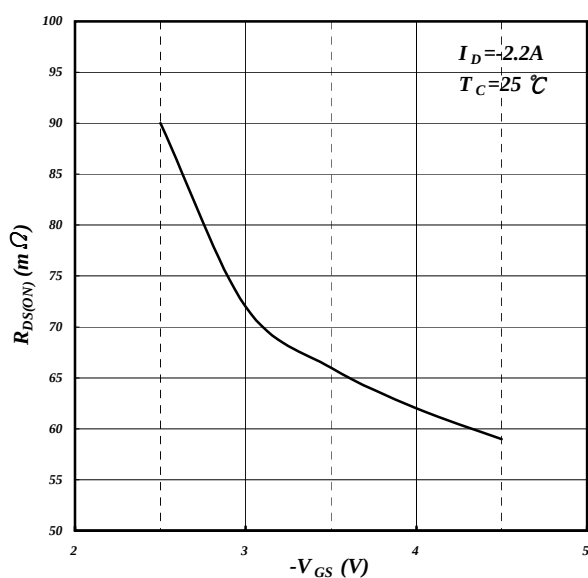


Fig 3. On-Resistance v.s. Gate Voltage

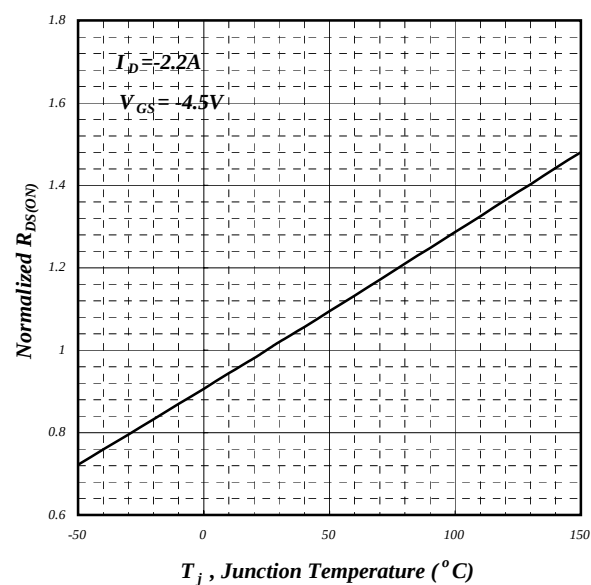


Fig 4. Normalized On-Resistance
v.s. Junction Temperature



P-Channel

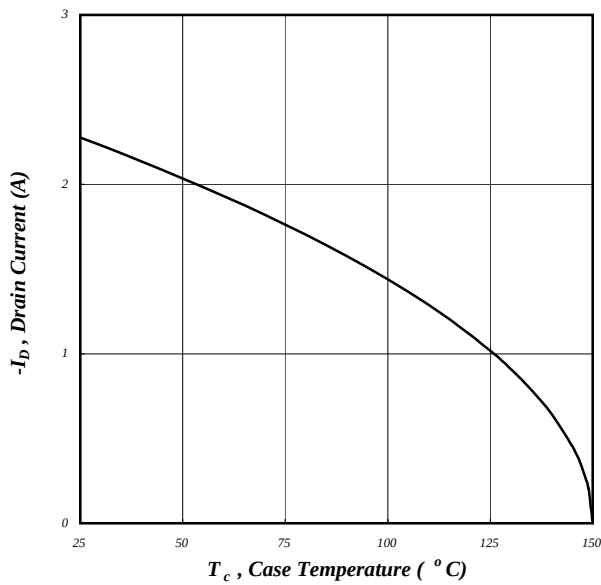


Fig 5. Maximum Drain Current v.s. Case Temperature

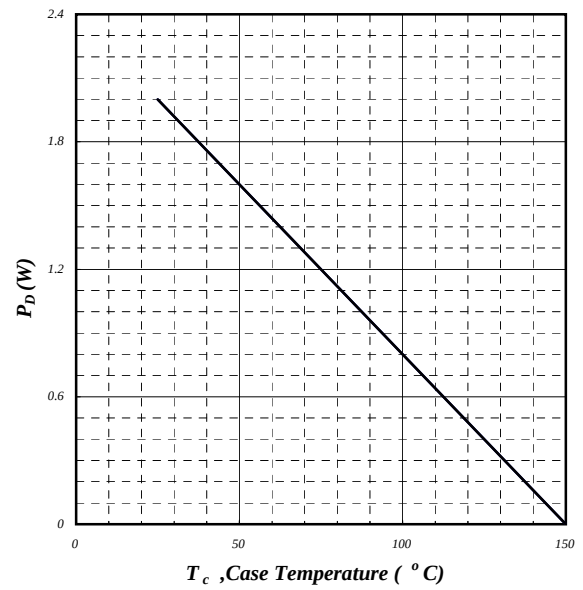


Fig 6. Typical Power Dissipation

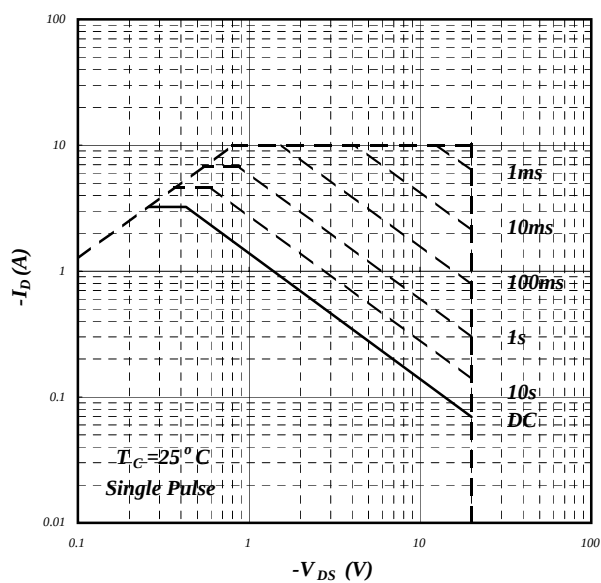


Fig 7. Maximum Safe Operating Area

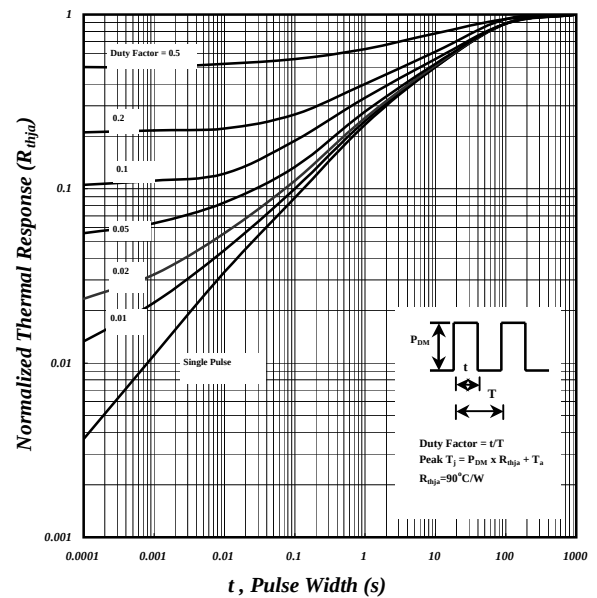


Fig 8. Effective Transient Thermal Impedance



P-Channel

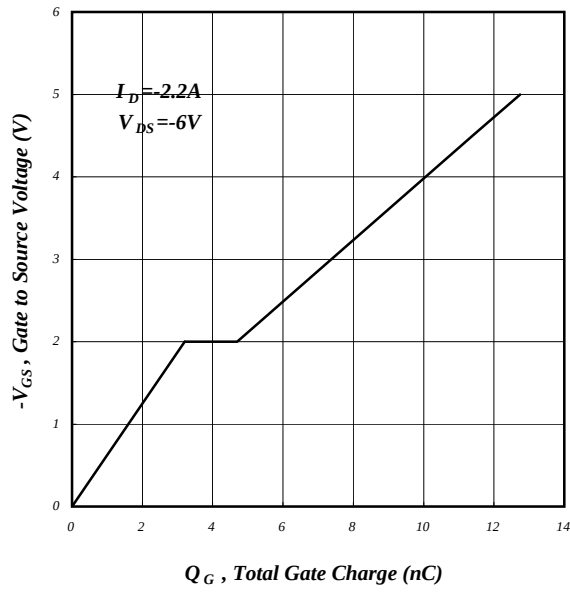


Fig 9. Gate Charge Characteristics

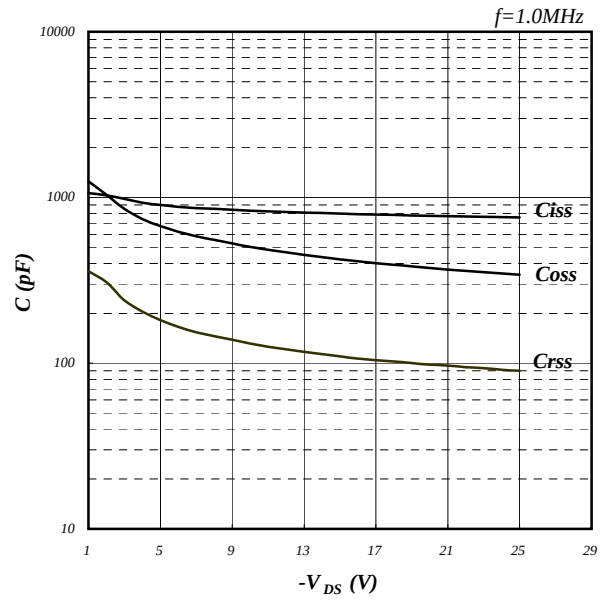


Fig 10. Typical Capacitance Characteristics

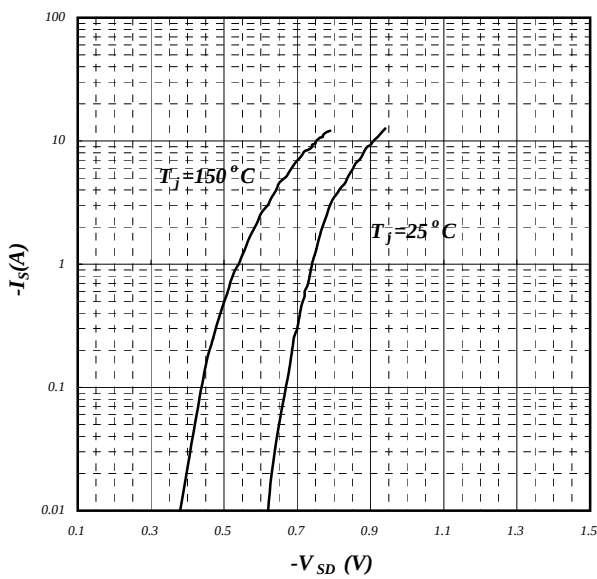


Fig 11. Forward Characteristic of Reverse Diode

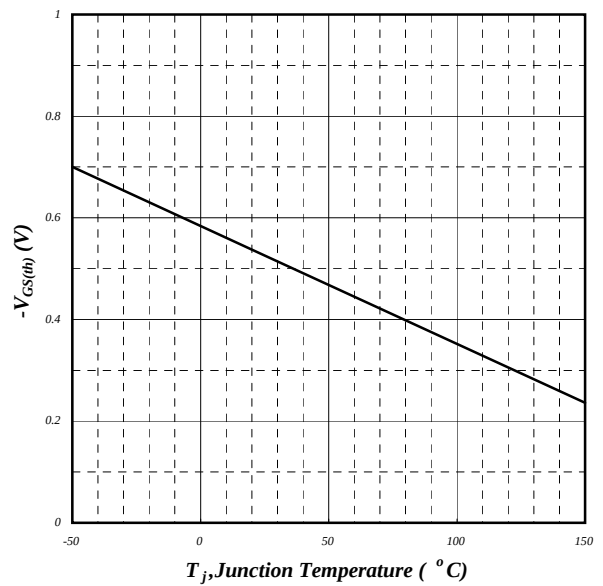


Fig 12. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

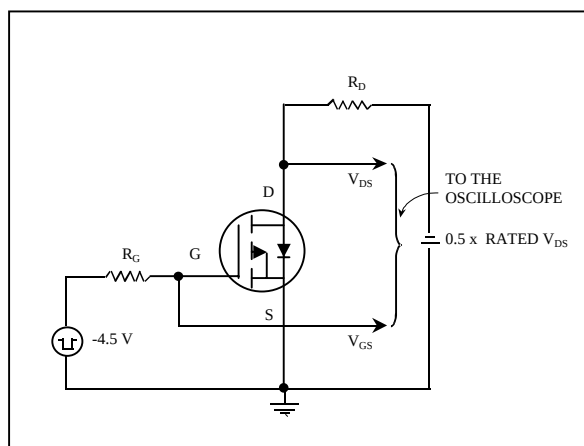


Fig 13. Switching Time Circuit

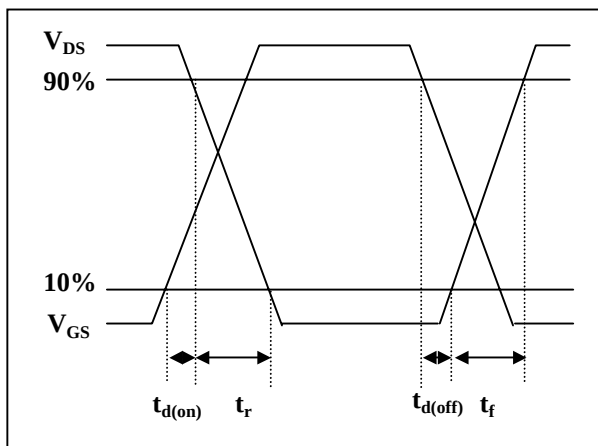


Fig 14. Switching Time Waveform

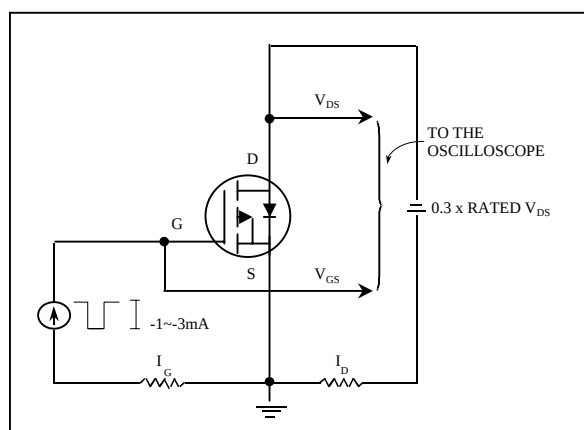


Fig 15. Gate Charge Circuit

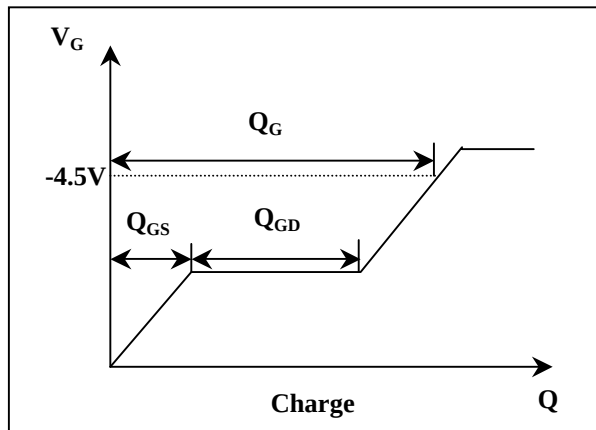


Fig 16. Gate Charge Waveform