



AP34063

UNIVERSAL DC/DC CONVERTER

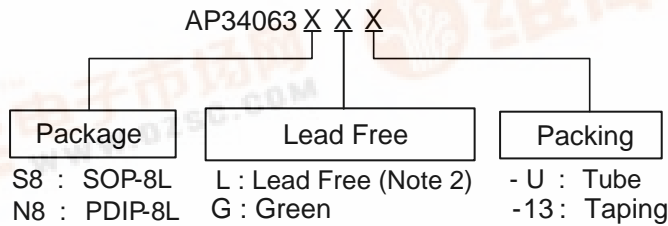
Features

- Operation from 3.0V to 40V Input
- Low Standby Current
- Current Limiting
- Output Switch Current to 1.6A
- Output Voltage Adjustable
- Frequency Operation to 100 kHz
- Precision 2% Reference
- 8-pin SOP, PDIP package
- Lead Free Finish/RoHS Compliant for Lead Free and "Green" products (Note 1)
- SOP-8L: Available in "Green" Molding Compound (No Br, Sb)

Description

The AP34063 Series is a monolithic control circuit containing the primary functions required for DC-to-DC converters. These devices consist of an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active current limit circuit, driver and high current output switch. This series is specifically designed for incorporating in Step-Down and Step-Up and Voltage-Inverting applications with a minimum number of external components.

Ordering Information



Note: 1. RoHS revision 13.2.2003. Glass and High Temperature Solder Exemptions Applied, see *EU Directive Annex Notes 5 and 7*.
 2. PDIP-8L is available in "Lead Free" only.

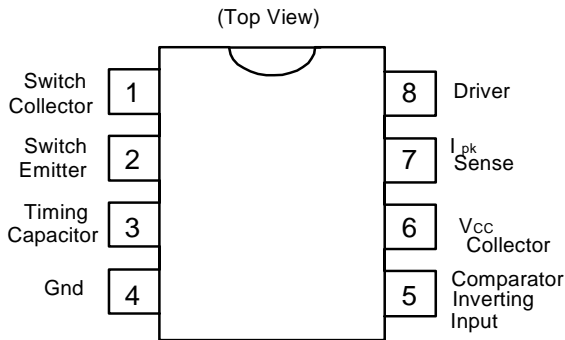
Device	Package Code	Packaging (Note 3)	Tube/Bulk		13" Tape and Reel	
			Quantity	Part Number Suffix	Quantity	Part Number Suffix
AP34063S8	S8	SOP-8L	100	- U	2500/Tape & Reel	-13
AP34063N8	N8	PDIP-8L	60	- U	NA	NA

Note: 3. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

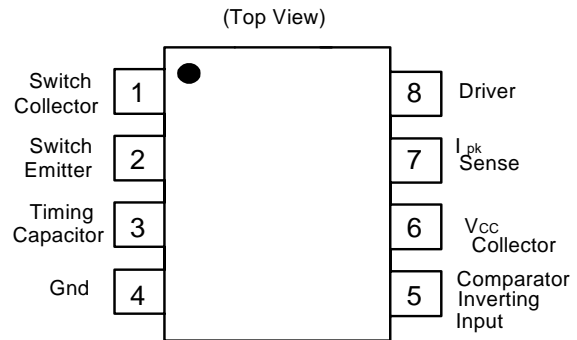


Pin Assignment

(1) PDIP-8L



(2) SOP-8L



Maximum Ratings

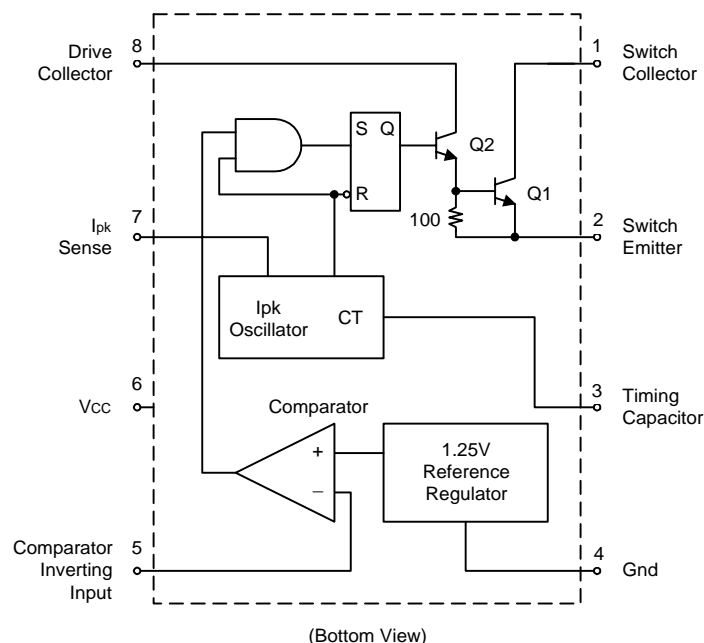
Parameter	Symbol	Value	Unit	
Power Supply Voltage	V_{CC}	40	V	
Comparator Input Voltage Range	V_{IR}	-0.3 ~ +40	V	
Switch Collector Voltage	V_C (switch)	40	V	
Switch Emitter Voltage ($V_{Pin\ 1} = 40V$)	V_E (switch)	40	V	
Switch Collector to Emitter Voltage	V_{CE} (switch)	40	V	
Driver Collector Voltage	V_C (driver)	40	V	
Driver Collector Current	I_C (driver)	100	mA	
Switch Current	I_{SW}	1.6	A	
Power Dissipation and Thermal Characteristics	SOP: $T_A = 25^\circ C$	P_D	600	mW
	PDIP: $T_A = 25^\circ C$	P_D	1.25	W
	Thermal Resistance	θ_{JA}	160	$^\circ C/W$
Maximum Junction Temperature	T_{MJ}	+150	$^\circ C$	
Operating Junction Temperature Range	T_{OP}	0 ~ +105	$^\circ C$	
Storage Temperature Range	T_{stg}	-65 ~ +150	$^\circ C$	

Note: 4. Maximum package power dissipation limits must be observed.
 5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

Electrical Characteristics ($V_{CC} = 5.0V$, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency ($V_{Pin\ 5} = 0V$, $C_T = 1.0nF$, $T_A = 25^\circ C$)	f_{osc}	24	33	42	kHz
Charge Current ($V_{CC} = 5.0V$ to $40V$, $T_A = 25^\circ C$)	I_{chg}	24	30	42	μA
Discharge Current ($V_{CC} = 5.0V$ to $40V$, $T_A = 25^\circ C$)	I_{dischg}	140	200	260	μA
Discharge to Charge Current Ratio (Pin 7 to V_{CC} , $T_A = 25^\circ C$)	I_{dischg} / I_{chg}	5.2	6.5	7.5	-
Current Limit Sense Voltage ($I_{chg} = I_{dischg}$, $T_A = 25^\circ C$)	$V_{ipk(sense)}$	300	400	450	mV
OUTPUT SWITCH (Note 3)					
Saturation Voltage, Darlington Connection ($I_{SW} = 1.0A$, Pins 1,8 connected)	$V_{CE(sat)}$	-	1.0	1.3	V
Saturation Voltage, Darlington Connection ($I_{SW} = 1.0A$, $I_D = 50mA$, Forced $\beta \approx 20$)	$V_{CE(sat)}$	-	0.45	0.7	V
DC Current Gain ($I_{SW} = 1.0A$, $V_{CE} = 5.0V$, $T_A = 25^\circ C$)	h_{FE}	50	75	-	-
Collector Off-State Current ($V_{CE} = 40V$)	$I_{C(off)}$	-	0.01	100	μA
COMPARATOR					
Threshold Voltage $T_A = 25^\circ C$ $T_A = 0^\circ C \sim 70^\circ C$	V_{th}	-	-	-	V
	-	1.225	1.25	1.275	-
	-	1.21	-	1.29	-
Threshold Voltage Line Regulation ($V_{CC} = 3.0V$ to $40V$)	Reg_{line}	-	1.4	6.0	mV
TOTAL DEVICE					
Supply Current ($V_{CC} = 5.0V$ to $40V$, $C_T = 1.0nF$, Pin 7 = V_{CC} , $V_{Pin\ 5} > V_{th}$ Pin 2 = Gnd, remaining pins open)	I_{CC}	-	-	3.5	mA

Representative Schematic Diagram



Typical Performance Characteristics

Figure 1. Vce(sat) versus Ie

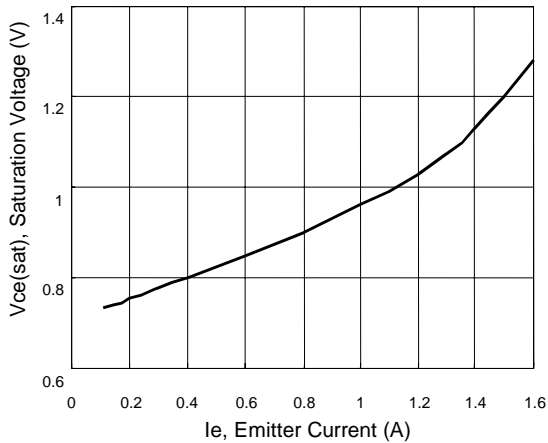


Figure 2. Reference Voltage versus Temp.

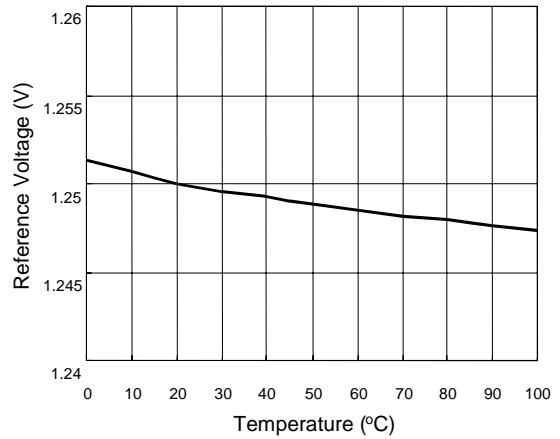


Figure 3. Current Limit Sense Voltage versus Temperature

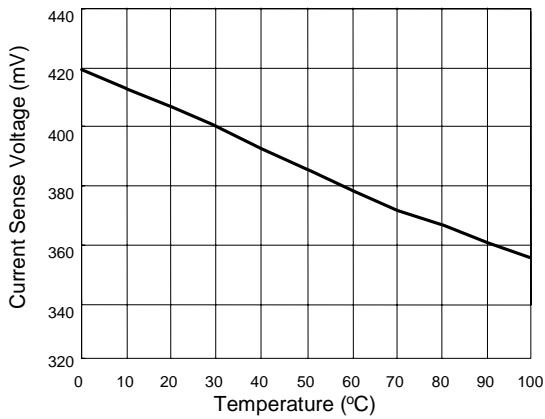


Figure 4. Standby Supply Current versus Supply Voltage

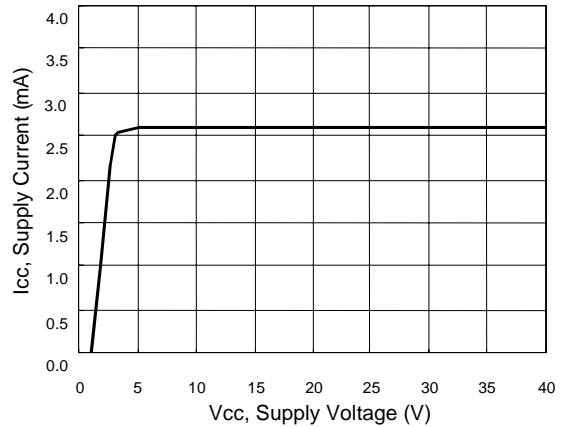


Figure 5. Emitter Follower Configuration Output Saturation Voltage vs. Emitter Current

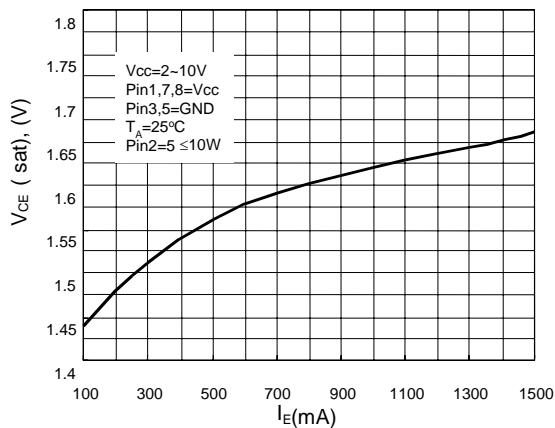
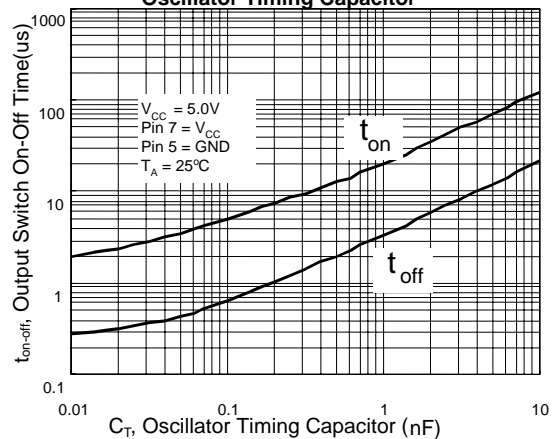
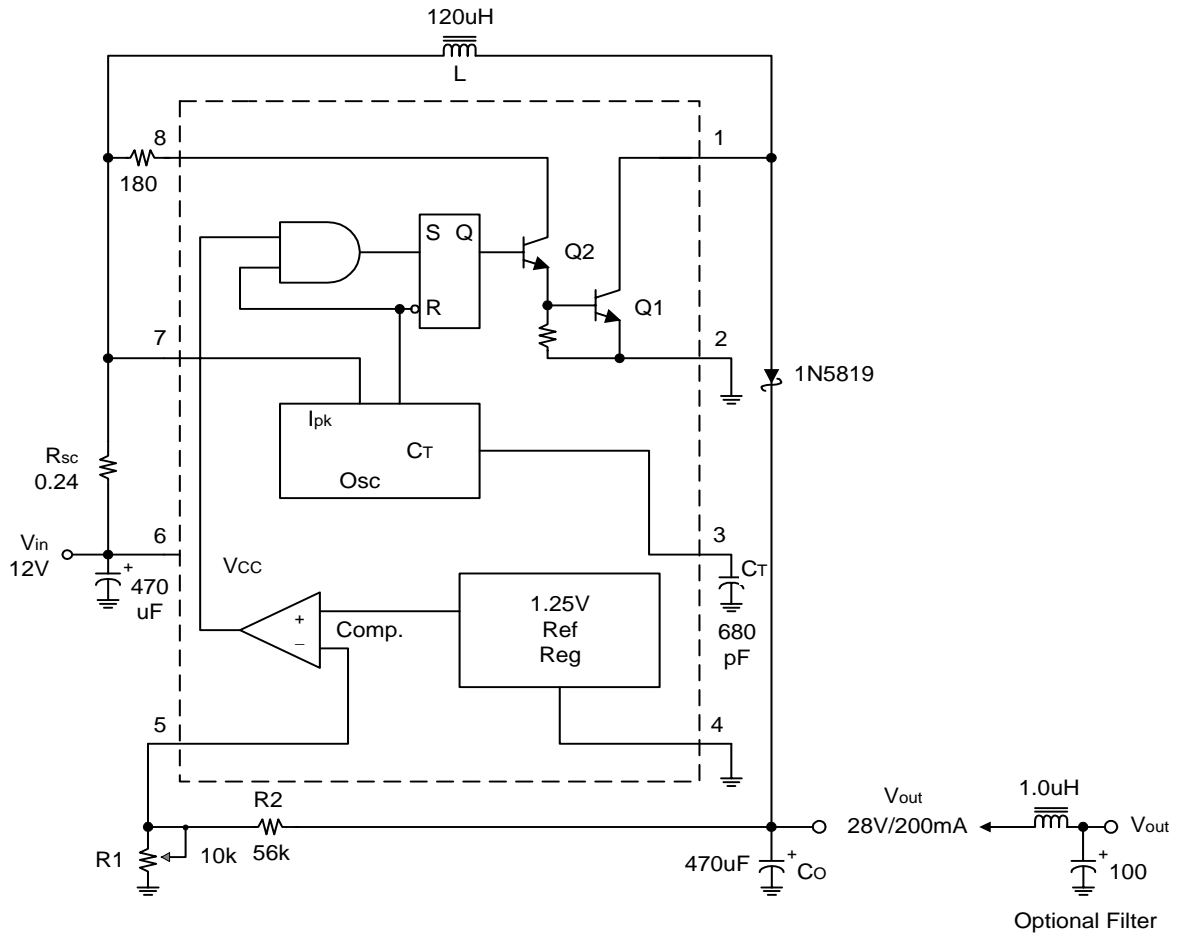


Figure 6. Output Switch On-Off Time versus Oscillator Timing Capacitor



Application Circuit

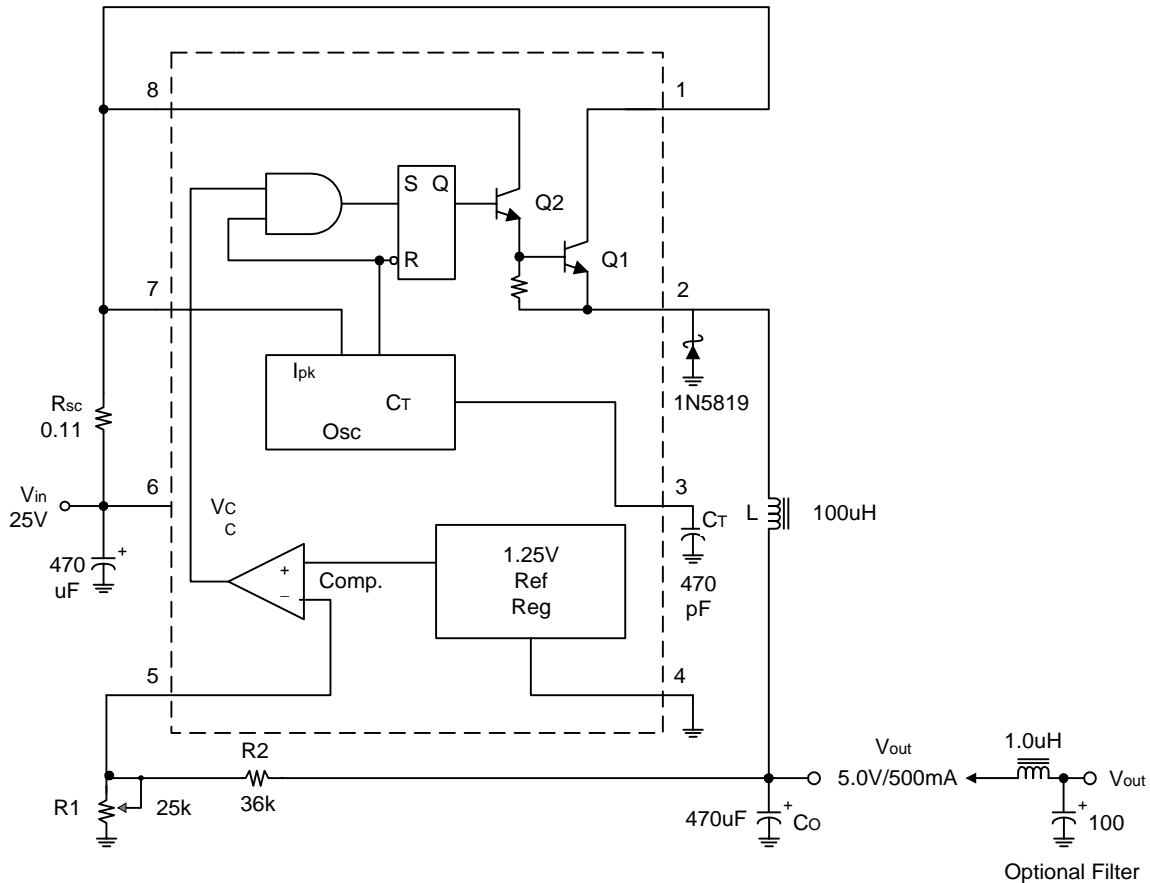
(1) Step-Up Converter



Test	Conditions	Results
Line Regulation	$V_{in} = 9V \text{ to } 12V, I_o = 200mA$	$20mV = \pm 0.035\%$
Load Regulation	$V_{in} = 12V, I_o = 50mA \text{ to } 200mA$	$15mV = \pm 0.035\%$
Output Ripple	$V_{in} = 12V, I_o = 200mA$	$500mV_{PP}$
Efficiency	$V_{in} = 12V, I_o = 200mA$	80%

Application Circuit (Continued)

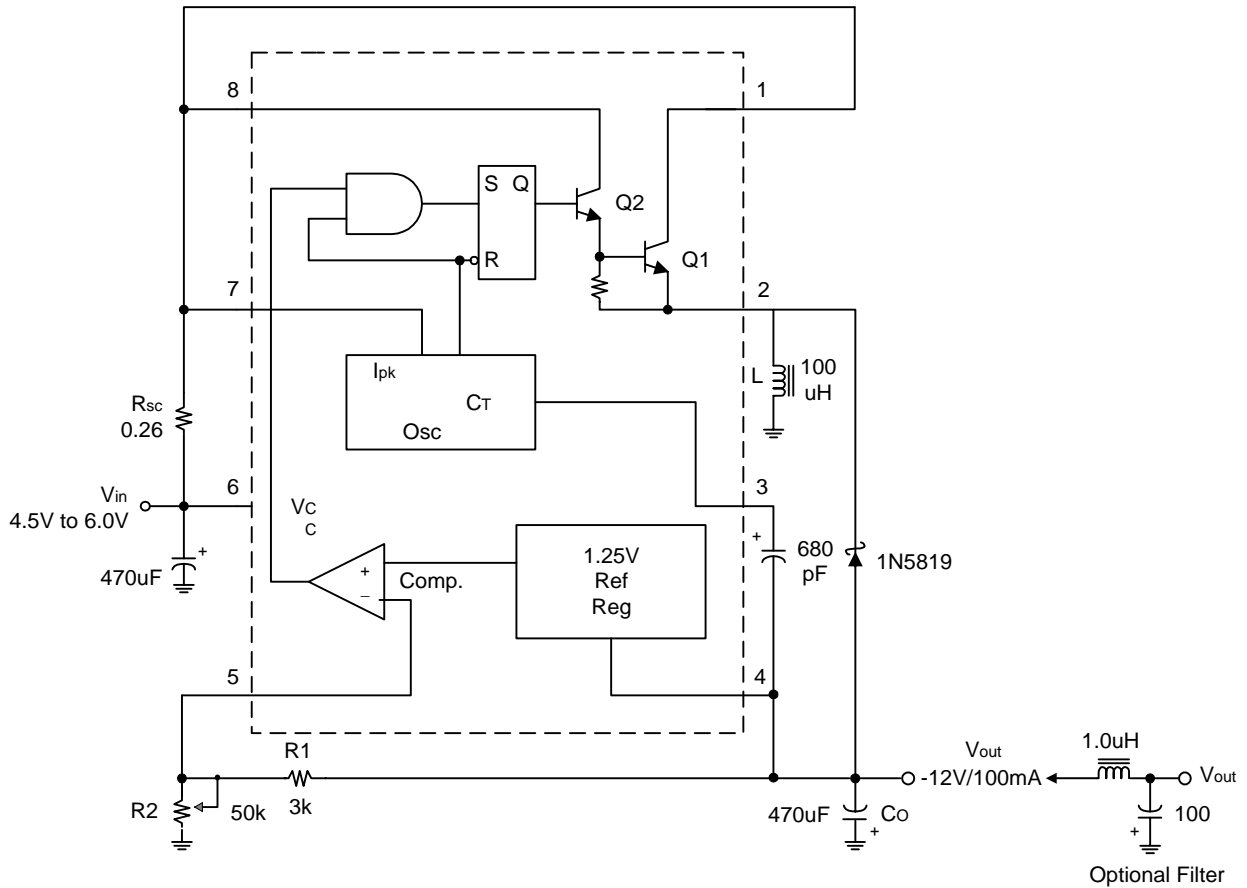
(2) Step-Down Converter



Test	Conditions	Results
Line Regulation	$V_{in} = 12V \text{ to } 24V, I_o = 500mA$	$20mV = \pm 0.2\%$
Load Regulation	$V_{in} = 24V, I_o = 50mA \text{ to } 500mA$	$5mV = \pm 0.05\%$
Output Ripple	$V_{in} = 24V, I_o = 500mA$	$160mV_{PP}$
Efficiency	$V_{in} = 24V, I_o = 500mA$	82%

Application Circuit (Continued)

(3) Voltage Inverting Converter



Test	Conditions	Results
Line Regulation	$V_{in} = 4.5V \text{ to } 6.0V, I_O = 100mA$	$20mV = \pm 0.08\%$
Load Regulation	$V_{in} = 5.0V, I_O = 20mA \text{ to } 100mA$	$30mV = \pm 0.12\%$
Output Ripple	$V_{in} = 5.0V, I_O = 100mA$	$500mV_{PP}$
Efficiency	$V_{in} = 5.0V, I_O = 100mA$	60%

Design Formula Table

Calculation	Step-Up	Step-Down	Voltage-Inverting
t_{on} / t_{off}	$\frac{V_{out} + V_F - V_{in (min)}}{V_{in (min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{ V_{out} + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$1/f$	$1/f$	$1/f$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$	$4.0 \times 10^{-5} t_{on}$
$I_{pk} (switch)$	$2I_{out (max)} (t_{on} / t_{off} + 1)$	$2I_{out (max)}$	$2I_{out (max)} (t_{on} / t_{off} + 1)$
R_{sc}	$0.3 / I_{pk} (switch)$	$0.3 / I_{pk} (switch)$	$0.3 / I_{pk} (switch)$
$L (min)$	$\frac{(V_{in (min)} - V_{sat})}{I_{pk} (switch)} t_{on (max)}$	$\frac{(V_{in (min)} - V_{sat} - V_{out})}{I_{pk} (switch)} t_{on (max)}$	$\frac{(V_{in (min)} - V_{sat})}{I_{pk} (switch)} t_{on (max)}$
C_O	$9 \frac{I_{out} t_{on}}{V_{ripple (pp)}}$	$\frac{I_{pk} (switch) (t_{off} + t_{on})}{8V_{ripple (pp)}}$	$9 \frac{I_{out} t_{on}}{V_{ripple (pp)}}$

V_{sat} = Saturation voltage of the output switch.
 V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} - Nominal input voltage.

V_{out} - Desired output voltage, $|V_{out}| = 1.25 (1+R2/R1)$

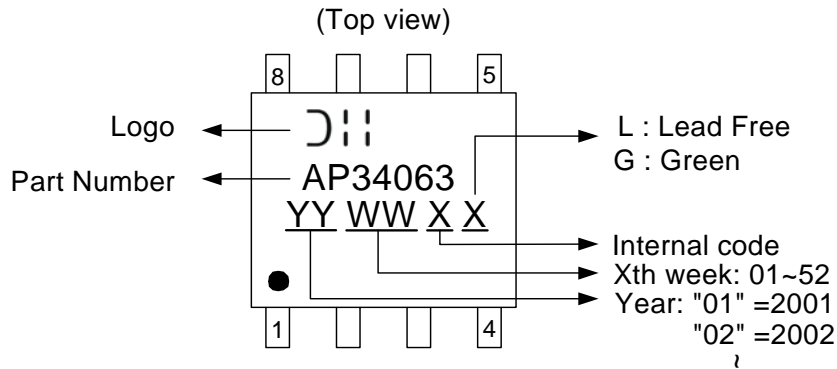
I_{out} - Desired output current.

f_{min} - Minimum desired output switching frequency at the selected values of V_{in} and I_o .

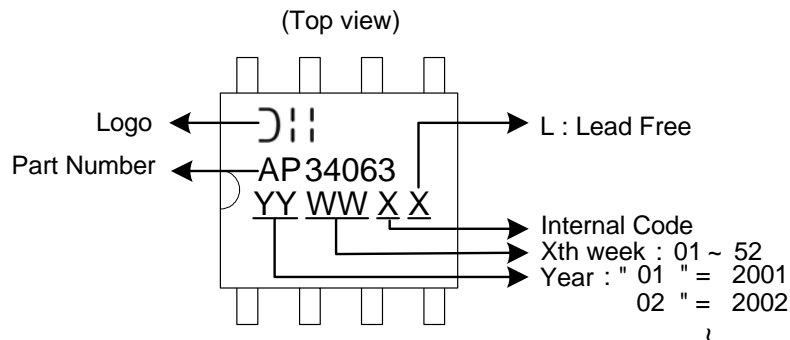
$V_{ripple(pp)}$ - Desired peak-to-peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

Marking Information

(1) SOP-8L



(2) PDIP-8L



Marking Code Table

Device	Package	Marking Code	Date Code
AP34063	SOP-8L	AP34063	YYWW
AP34063	PDIP-8L	AP34063	YYWW

IMPORTANT NOTICE

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