



**Advanced Power
Electronics Corp.**

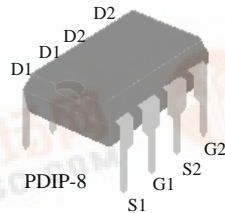
AP4511GED

Pb Free Plating Product

N AND P-CHANNEL ENHANCEMENT

MODE POWER MOSFET

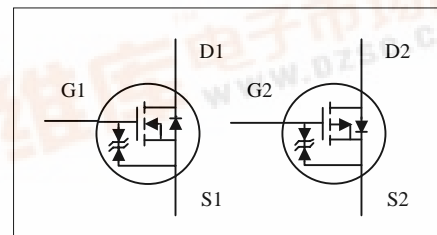
- ▼ Simple Drive Requirement
- ▼ Lower Gate Charge
- ▼ Fast Switching Performance
- ▼ RoHS Compliant



N-CH	BV_{DSS}	40V
	$R_{DS(ON)}$	28mΩ
	I_D	6A
P-CH	BV_{DSS}	-40V
	$R_{DS(ON)}$	42mΩ
	I_D	-5A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	40	-40	V
V_{GS}	Gate-Source Voltage	±16	±16	V
$I_D@T_A=25^\circ C$	Continuous Drain Current ³	6.0	-5.0	A
$I_D@T_A=70^\circ C$	Continuous Drain Current ³	5.0	-4.0	A
I_{DM}	Pulsed Drain Current ¹	30	-30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
T_{STG}	Storage Temperature Range	-55 to 150		°C
T_J	Operating Junction Temperature Range	-55 to 150		°C

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient ³	Max.	62.5 °C/W



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N-CH Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^{\circ}\text{C}, I_D=1\text{mA}$	-	0.03	-	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6A$	-	-	28	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=4A$	-	-	36	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=6A$	-	6	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^{\circ}\text{C}$)	$V_{DS}=40V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^{\circ}\text{C}$)	$V_{DS}=32V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 16V$	-	-	± 30	μA
Q_g	Total Gate Charge ²	$I_D=6A$	-	8.2	13	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=20V$	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	3.6	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=20V$	-	7	-	ns
t_r	Rise Time	$I_D=6A$	-	20	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3\Omega, V_{GS}=10V$	-	20	-	ns
t_f	Fall Time	$R_D=3.3\Omega$	-	4	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	590	940	pF
C_{oss}	Output Capacitance	$V_{DS}=20V$	-	110	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	80	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	2	3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1.25A, V_{GS}=0V$	-	-	1.6	V
t_{rr}	Reverse Recovery Time ²	$I_S=6A, V_{GS}=0V$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	12	-	nC

**P-CH Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D=-1\text{mA}$	-	-0.03	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-5A$	-	-	42	$\text{m}\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	-	-	60	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8	-	-2.5	V
g_{fs}	Forward Transconductance	$V_{DS}=-10V, I_D=-5A$	-	5	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{DS}=-40V, V_{GS}=0V$	-	-	-1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{DS}=-32V, V_{GS}=0V$	-	-	-25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 16V$	-	-	± 30	μA
Q_g	Total Gate Charge ²	$I_D=-5A$	-	9	24	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=-20V$	-	2	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	5	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=-20V$	-	8.5	-	ns
t_r	Rise Time	$I_D=-5A$	-	15	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3\Omega, V_{GS}=-10V$	-	27	-	ns
t_f	Fall Time	$R_D=4\Omega$	-	25	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	770	1230	pF
C_{oss}	Output Capacitance	$V_{DS}=-20V$	-	165	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	115	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	6	9	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=-1.25A, V_{GS}=0V$	-	-	-1.6	V
t_{rr}	Reverse Recovery Time ²	$I_S=-5A, V_{GS}=0V$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=-100A/\mu s$	-	16	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in^2 copper pad of FR4 board, $t \leq 10\text{sec}$; 90°C/W when mounted on min. copper pad.



N-Channel

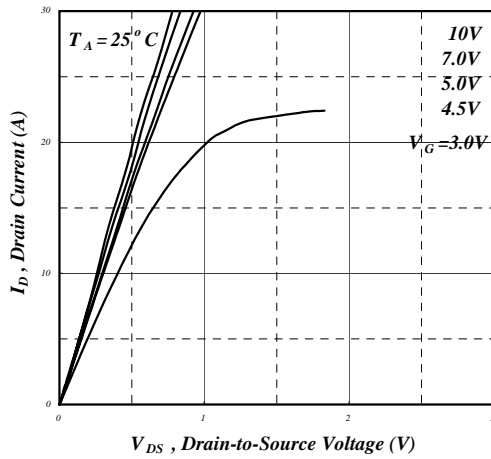


Fig 1. Typical Output Characteristics

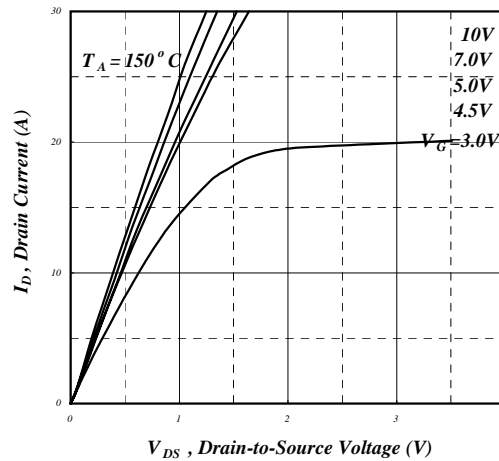


Fig 2. Typical Output Characteristics

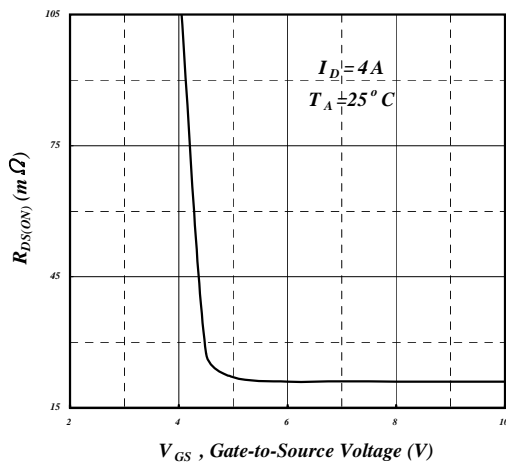


Fig 3. On-Resistance v.s. Gate Voltage

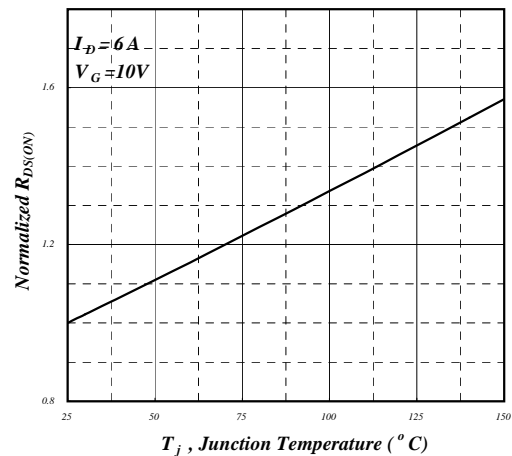


Fig 4. Normalized On-Resistance v.s. Junction Temperature

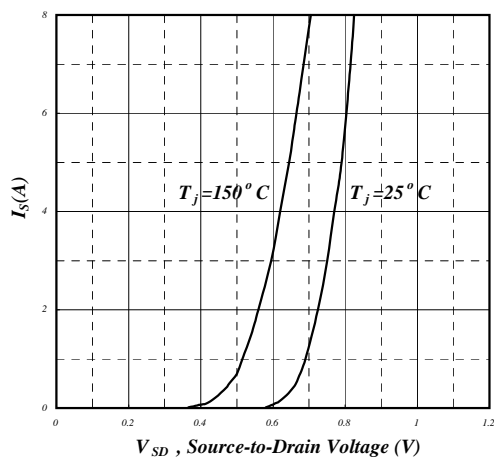


Fig 5. Forward Characteristic of Reverse Diode

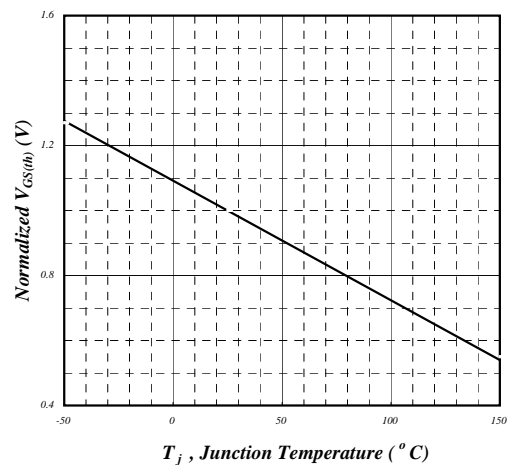


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



N-Channel

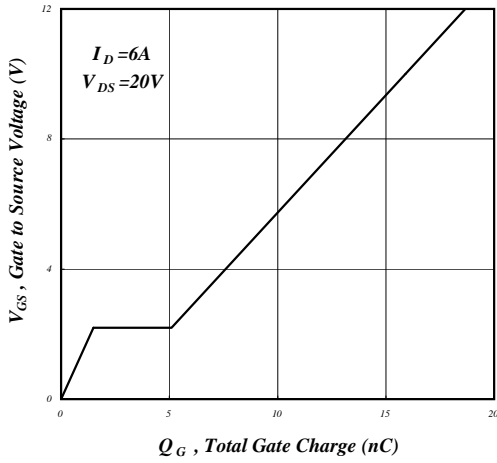


Fig 7. Gate Charge Characteristics

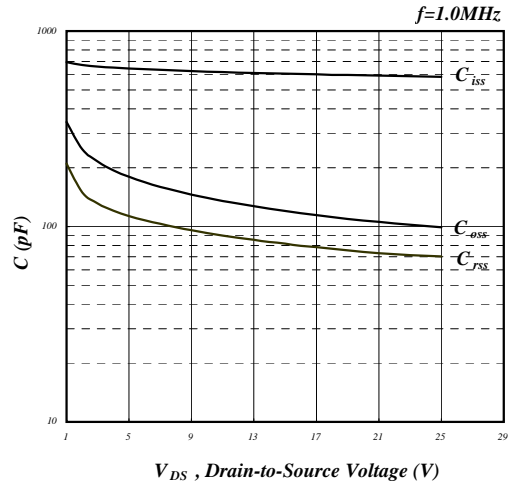


Fig 8. Typical Capacitance Characteristics

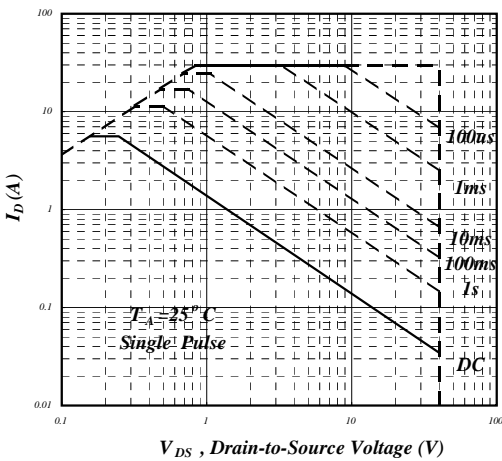


Fig 9. Maximum Safe Operating Area

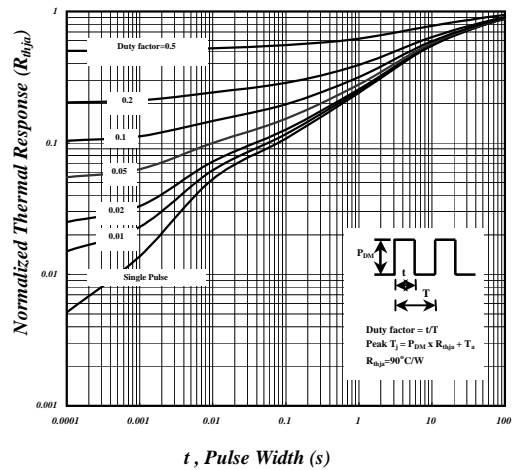


Fig 10. Effective Transient Thermal Impedance

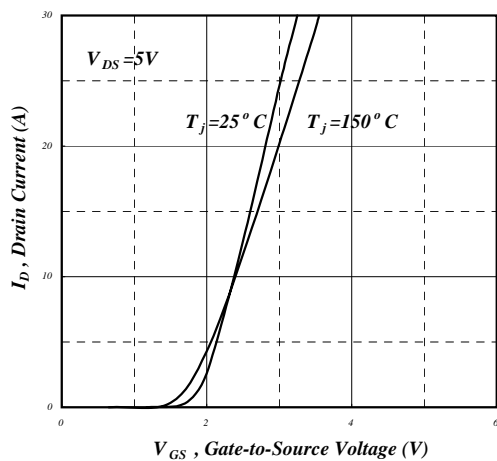


Fig 11. Transfer Characteristics

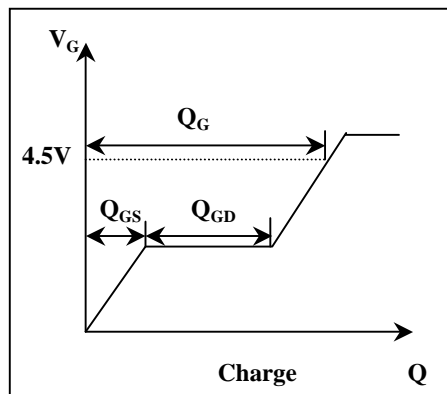


Fig 12. Gate Charge Waveform



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P-Channel

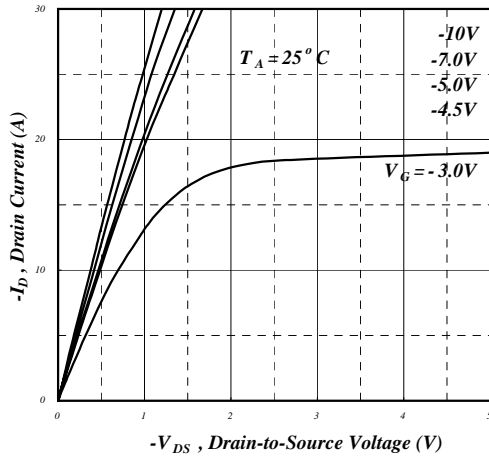


Fig 1. Typical Output Characteristics

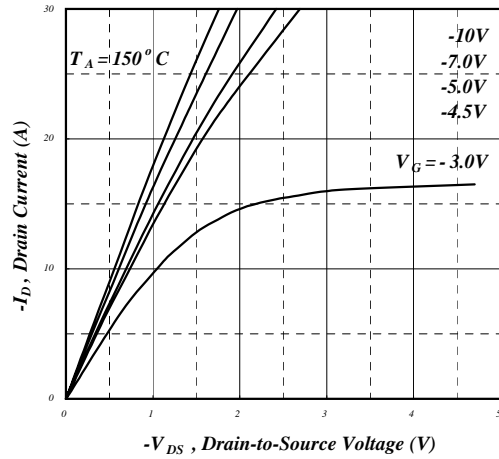


Fig 2. Typical Output Characteristics

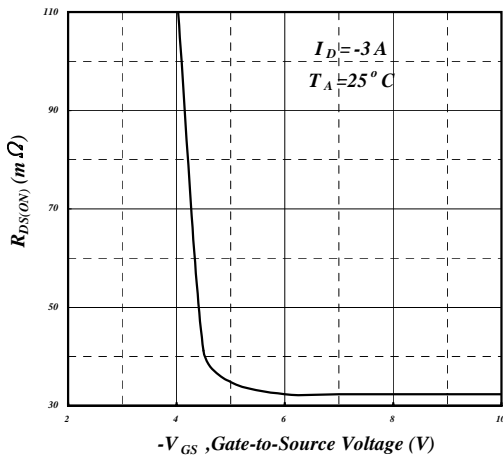


Fig 3. On-Resistance v.s. Gate Voltage

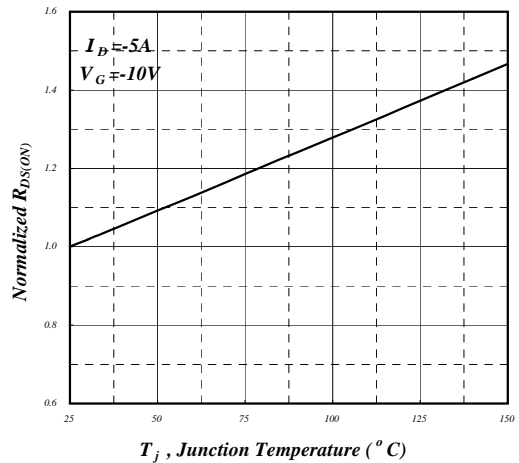


Fig 4. Normalized On-Resistance v.s. Junction Temperature

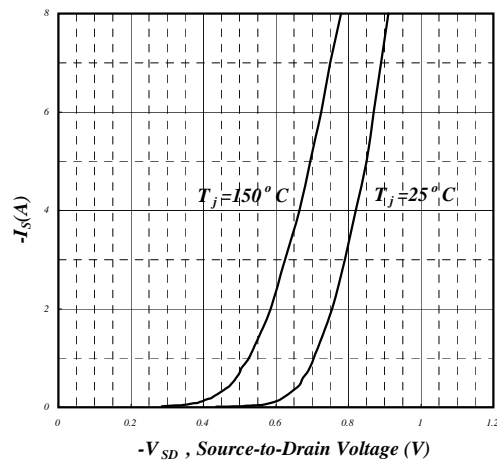


Fig 5. Forward Characteristic of Reverse Diode

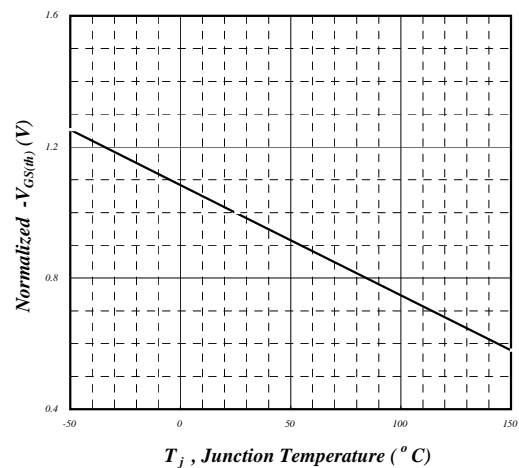


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



P-Channel

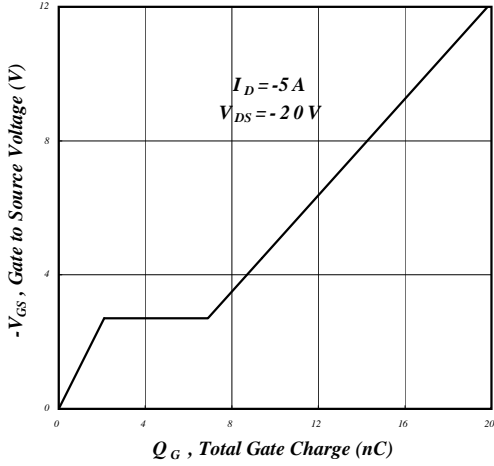


Fig 7. Gate Charge Characteristics

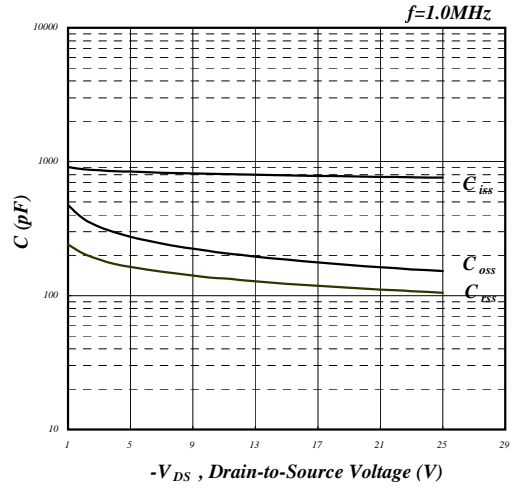


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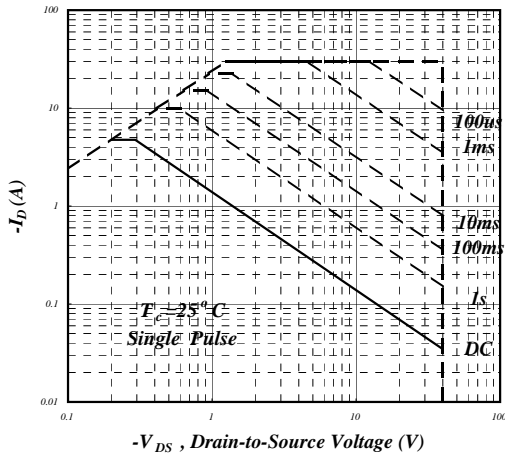


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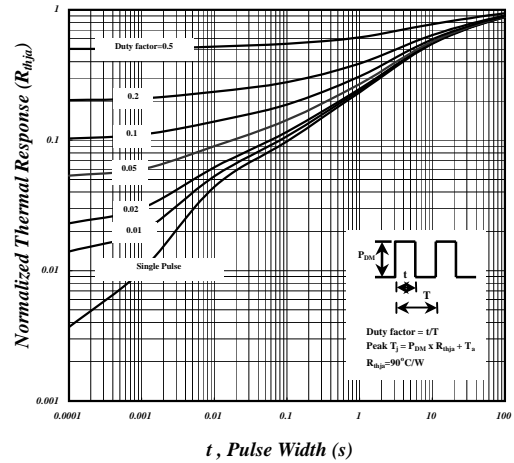


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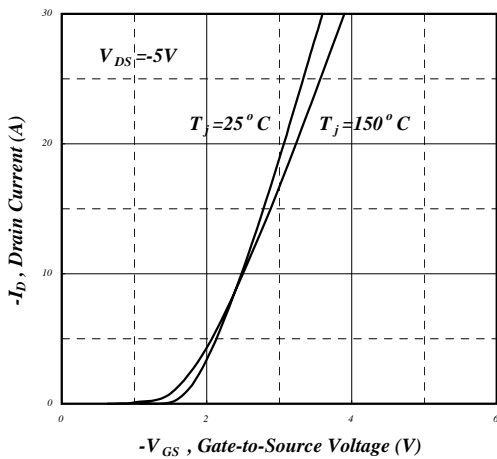


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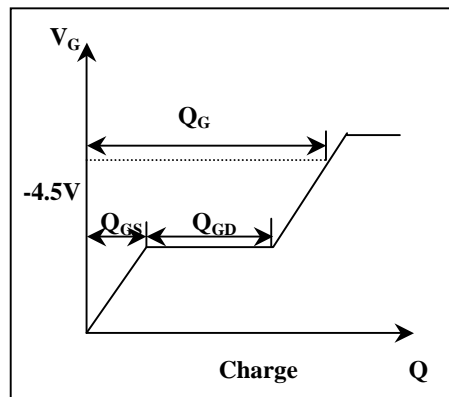


Fig 12. Gate Charge Waveform