



**Advanced Power
Electronics Corp.**

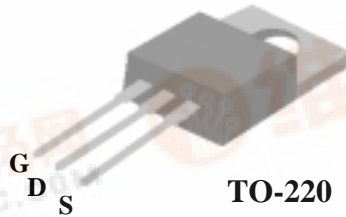
AP630GP

Pb Free Plating Product

N-CHANNEL ENHANCEMENT MODE

POWER MOSFET

- ▼ Dynamic dv/dt Rating
- ▼ Repetitive Avalanche Rated
- ▼ Fast Switching
- ▼ Simple Drive Requirement

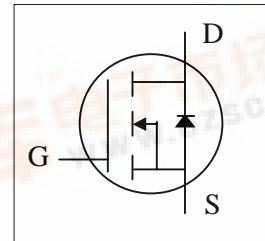


BV_{DSS}	200V
$R_{DS(ON)}$	400mΩ
I_D	9A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The through-hole version (AP630GP) is available for low-profile applications.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	200	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, V_{GS} @ 10V	9	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, V_{GS} @ 10V	5.7	A
I_{DM}	Pulsed Drain Current ¹	36	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation	74	W
	Linear Derating Factor	0.59	W/°C
E_{AS}	Single Pulse Avalanche Energy ²	240	mJ
I_{AR}	Avalanche Current	9	A
E_{AR}	Repetitive Avalanche Energy	7	mJ
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Thermal Resistance Junction-case	Max. 1.7	°C/W
Rthj-a	Thermal Resistance Junction-ambient	Max. 62	°C/W





AP630GP

Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	200	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.248	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =5A	-	-	400	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =5A	-	40	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =200V, V _{GS} =0V	-	-	10	uA
	Drain-Source Leakage Current (T _j =150°C)	V _{DS} =160V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Forward Leakage	V _{GS} = ± 30V	-	-	±100	nA
Q _g	Total Gate Charge ³	I _D = 9A	-	25	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =160V	-	3.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	14	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =100V	-	8	-	ns
t _r	Rise Time	I _D = 9A	-	26	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =10Ω, V _{GS} =10V	-	34	-	ns
t _f	Fall Time	R _D =11Ω	-	22	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	515	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	90	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	40	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =1.3V	-	-	9	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	36	A
V _{SD}	Forward On Voltage ³	T _j =25°C, I _S =9A, V _{GS} =0V	-	-	1.3	V

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Starting T_j=25°C , V_{DD}=50V , L=4.5mH , R_G=25Ω , I_{AS}=9A.
- 3.Pulse width ≤300us , duty cycle ≤2%.

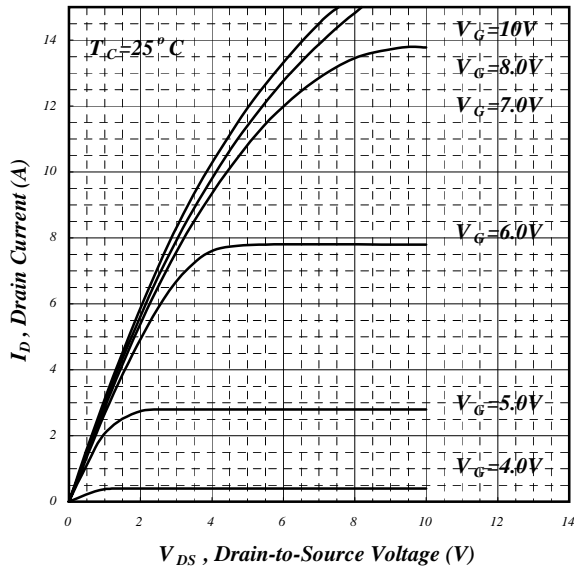


Fig 1. Typical Output Characteristics

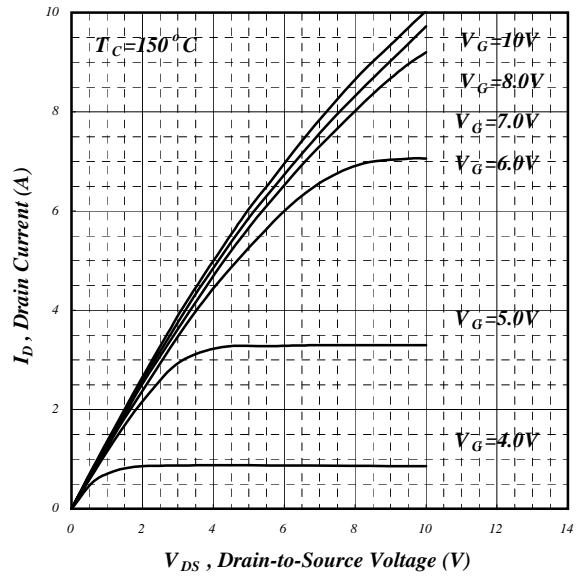


Fig 2. Typical Output Characteristics

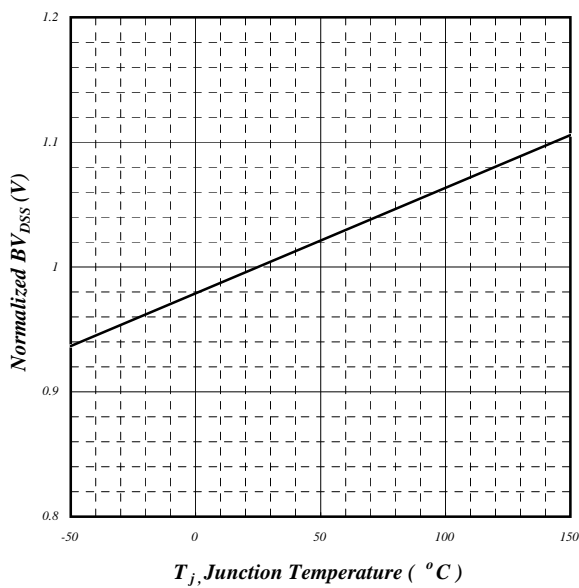


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

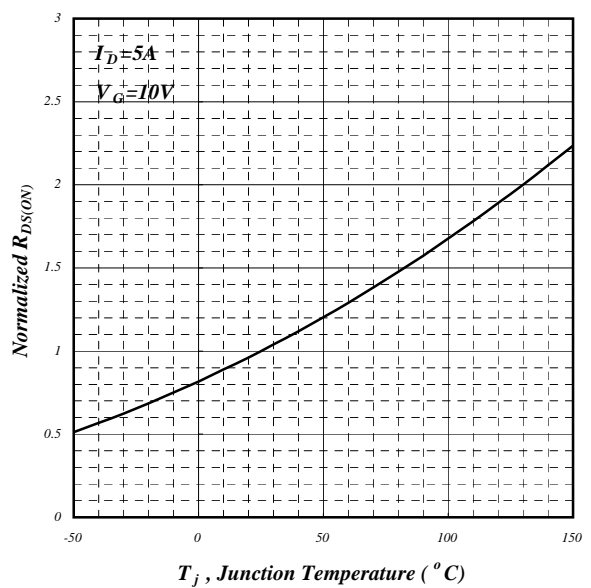


Fig 4. Normalized On-Resistance v.s. Junction Temperature

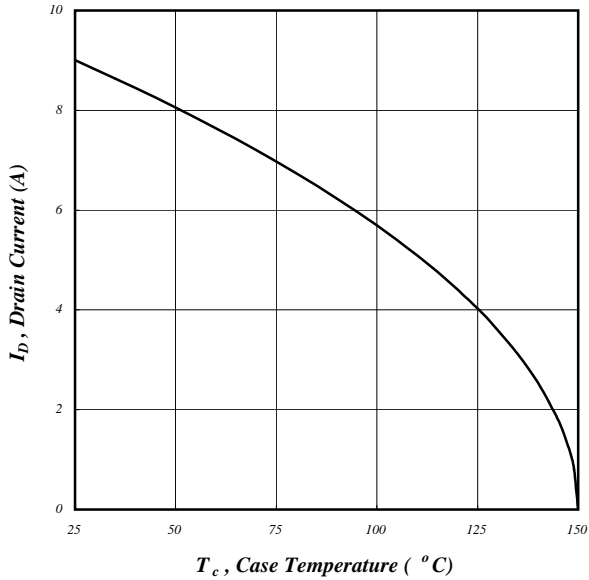


Fig 5. Maximum Drain Current v.s. Case Temperature

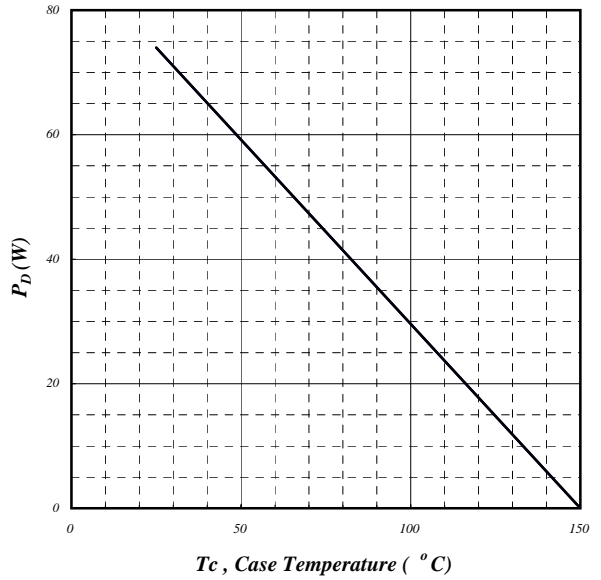


Fig 6. Typical Power Dissipation

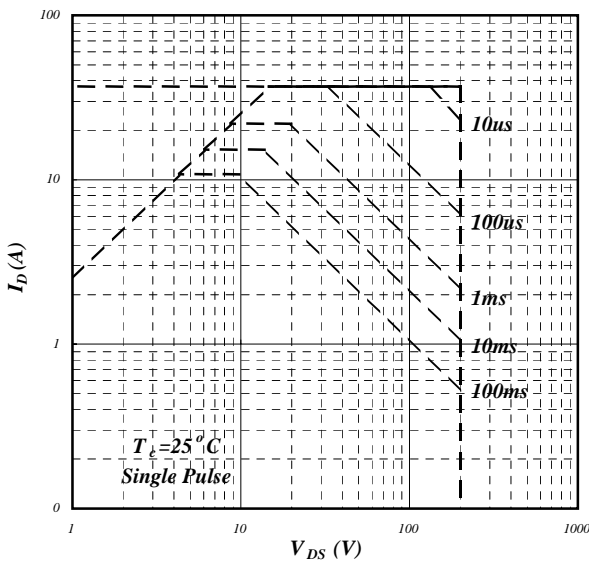


Fig 7. Maximum Safe Operating Area

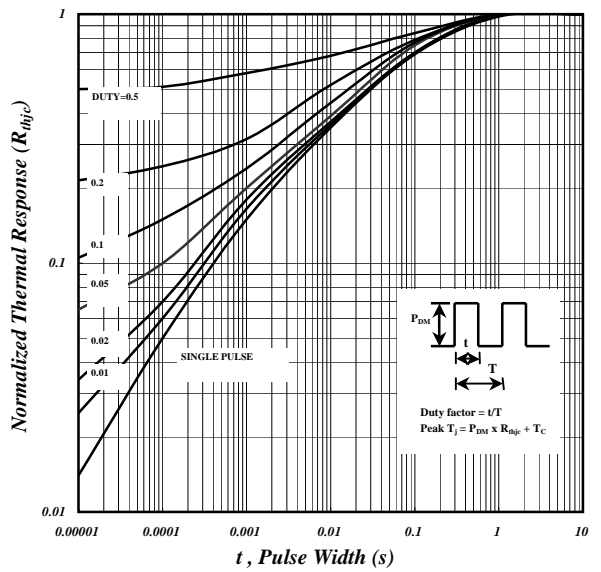


Fig 8. Effective Transient Thermal Impedance

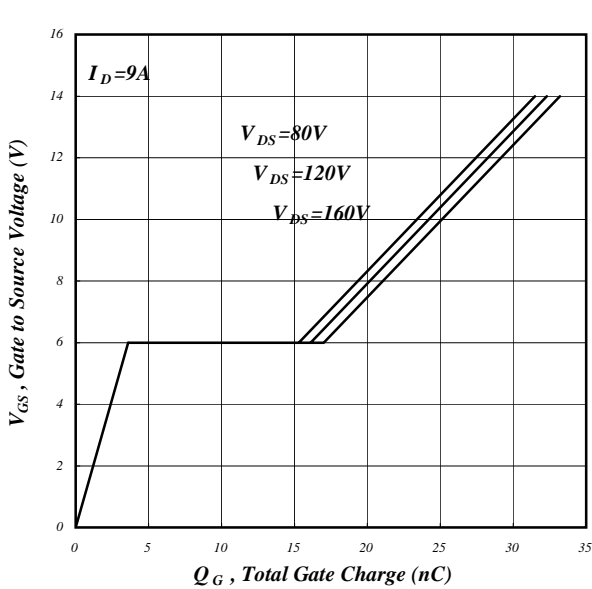


Fig 9. Gate Charge Characteristics

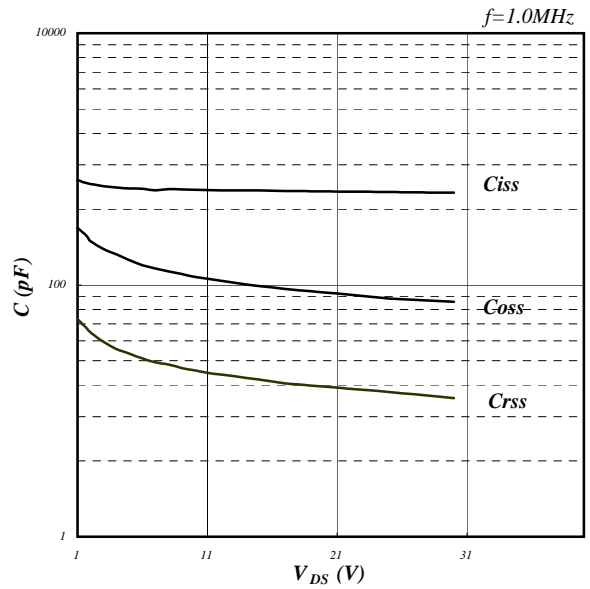


Fig 10. Typical Capacitance Characteristics

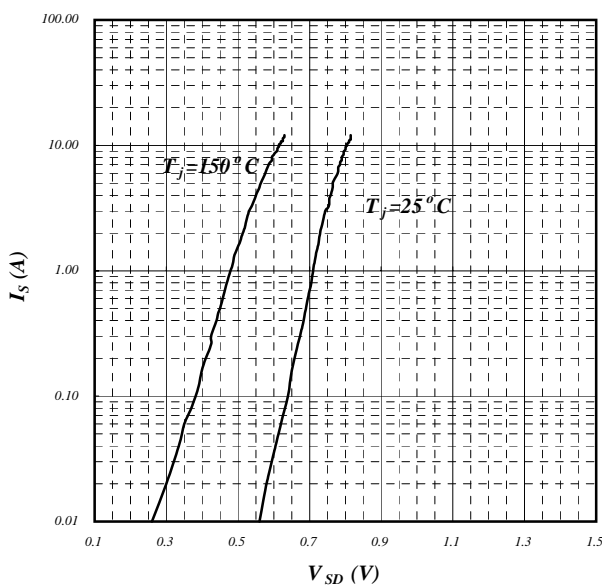


Fig 11. Forward Characteristic of Reverse Diode

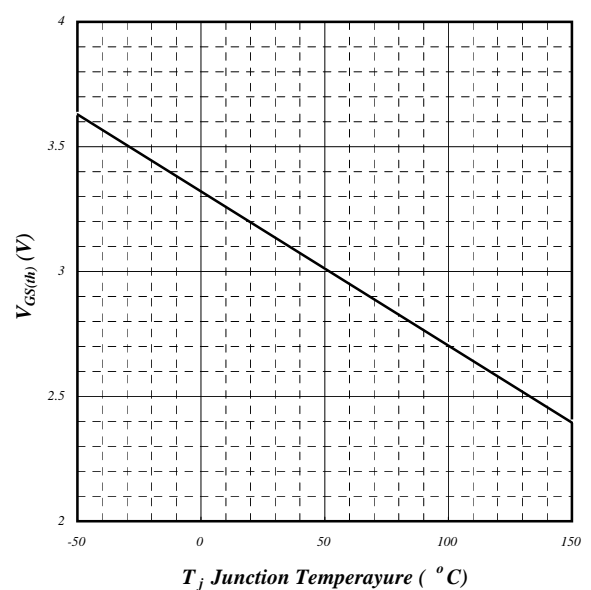


Fig 12. Gate Threshold Voltage v.s. Junction Temperature

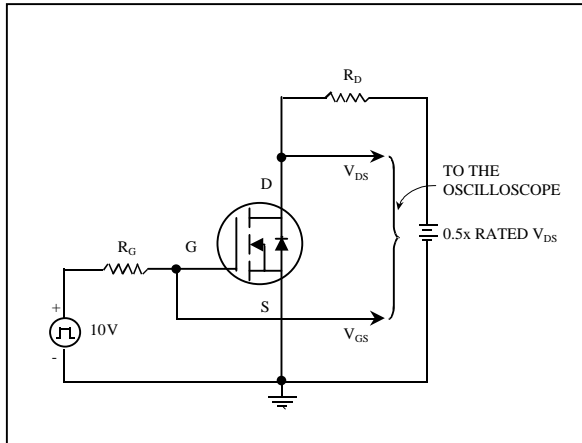


Fig 13. Switching Time Circuit

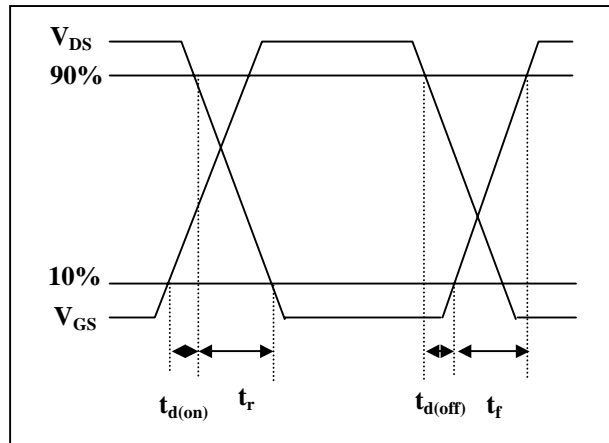


Fig 14. Switching Time Waveform

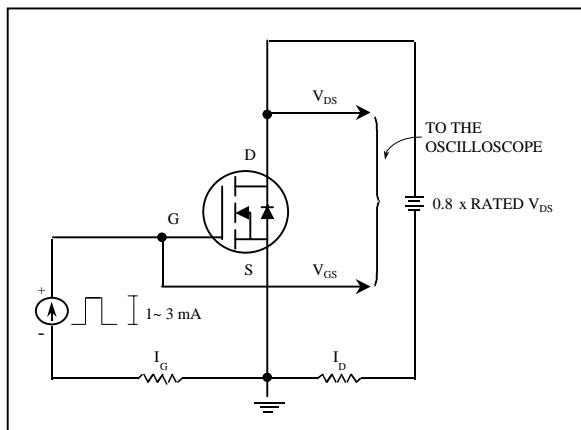


Fig 15. Gate Charge Circuit

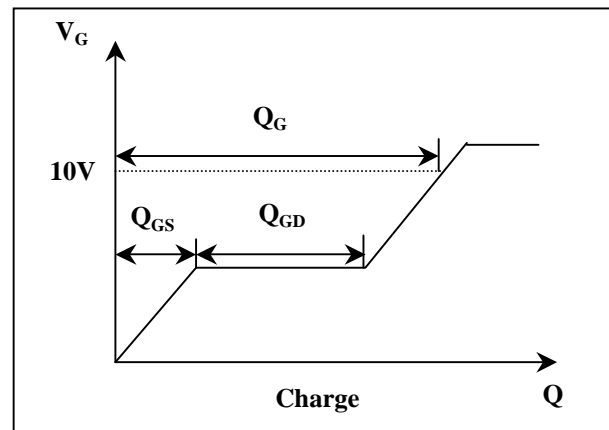


Fig 16. Gate Charge Waveform