AP7173

1.5A LOW DROPOUT LINEAR REGULATOR WITH PROGRAMMABLE SOFT-START

Features

- Low V_{IN} and wide V_{IN} range: 1.0V to 5.5V
- Bias voltage (V_{VCC}) range: 2.7V to 5.5V
- Low V_{OUT} range: 0.8V to 3.3V
- Low dropout: 165mV typical at 1.5A, V_{VCC} = 5V
- 2% accuracy over line, load and temperature range
- Power-Good (PG) output for supply monitoring and for sequencing of other supplies
- Programmable soft-start provides linear voltage startup
- Bias supply permits low V_{IN} operation with good transient response
- Stable with any output capacitor ≥ 2.2µF
- DFN3030-10 and SOP-8L-EP: available in “Green” molding compound (No Br, Sb)
- Lead-free finish/ RoHS Compliant (Note 1)

General Description

The AP7173 is a 1.5A low-dropout (LDO) linear regulator that features a user-programmable soft-start, an enable input and a power-good output.

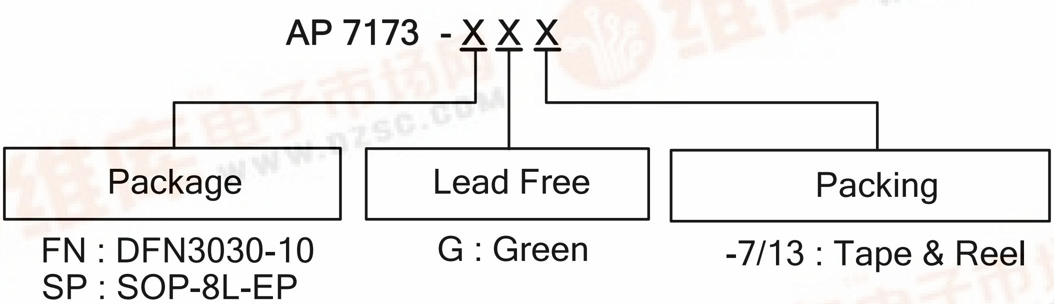
The soft-start reduces inrush current of the load capacitors and minimizes stress on the input power source during start-up. The enable input and power-good output allow users to configure power management solutions that can meet the sequencing requirements of FPGAs, DSPs, and other applications with different start-up and power-down requirements.

The AP7173 is stable with any type of output capacitor of 2.2µF or more. A precision reference and feedback control deliver 2% accuracy over load, line, and operating temperature ranges. The AP7173 is available in both DFN3030-10 and SOP-8L-EP packages.

Applications

- PCs, Servers, Modems, and Set-Top-Boxes
- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications With Sequencing Requirements

Ordering Information

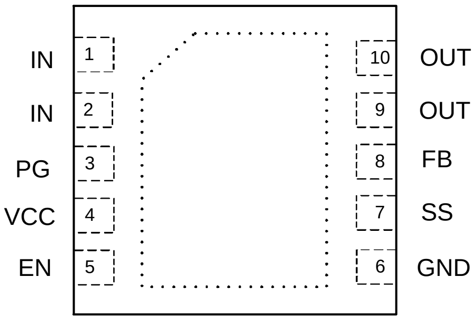


Device	Package Code	Packaging (Note 2)	7”/13” Tape and Reel	
			Quantity	Part Number Suffix
AP7173-FN	FN	DFN3030-10	3000/Tape & Reel	-7
AP7173-SP	SP	SOP-8L-EP	2500/Tape & Reel	-13

Notes: 1. RoHS revision 13.2.2003. Glass and high temperature solder exemptions applied, see *EU Directive Annex Notes 5 and 7.*
2. Pad layout as shown on Diodes Inc. suggested pad layout document can be found on our website at http://www.diodes.com/datasheets/ap02001.pdf.

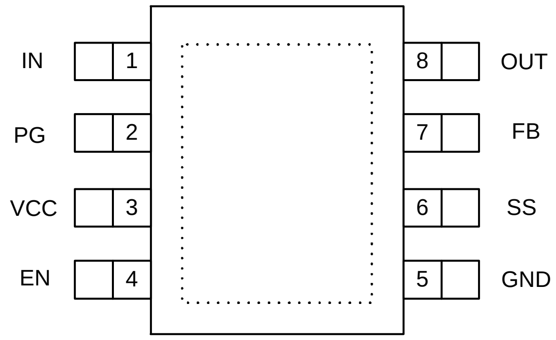
Pin Assignments

(Top View)



DFN3030-10

(Top View)

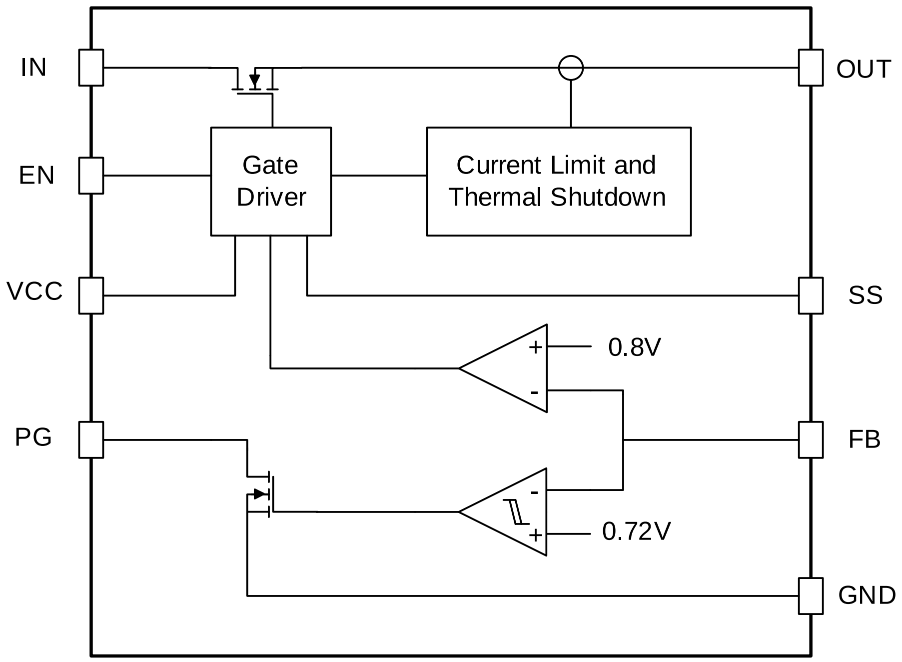


SOP-8L-EP

Pin Descriptions

Pin Name	PIN #		Description
	SOP-8L-EP	DFN3030-10	
IN	1	1, 2	Power Input pin.
PG	2	3	Power-Good pin, open-drain output. When the V_{OUT} is below the PG threshold the PG pin is driven low; when the V_{OUT} exceeds the threshold, the PG pin goes into a high-impedance state. To use the PG pin, use a 10kΩ to 1MΩ pull-up resistor to pull it up to a supply of up to 5.5V, which can be higher than the input voltage.
VCC	3	4	Bias Input pin, provides input voltage for internal control circuitry. This voltage should be higher than the V_{IN}.
EN	4	5	Enable pin. This pin should be driven either high or low and must not be floating. Driving this pin high enables the regulator, while pulling it low puts the regulator into shutdown mode.
GND	5	6	Ground.
SS	6	7	Soft-Start pin. Connect a capacitor between this pin and the ground to set the soft-start ramp time of the output voltage. If no capacitor is connected, the soft-start time is typically 100µS.
FB	7	8	Feedback pin. Connect this pin to an external voltage divider to set the output voltage.
OUT	8	9, 10	Regulated Output pin.
Thermal Pad	—	—	Solder this pad to large ground plane for increased thermal performance.

Block Diagram



Typical Application Circuit

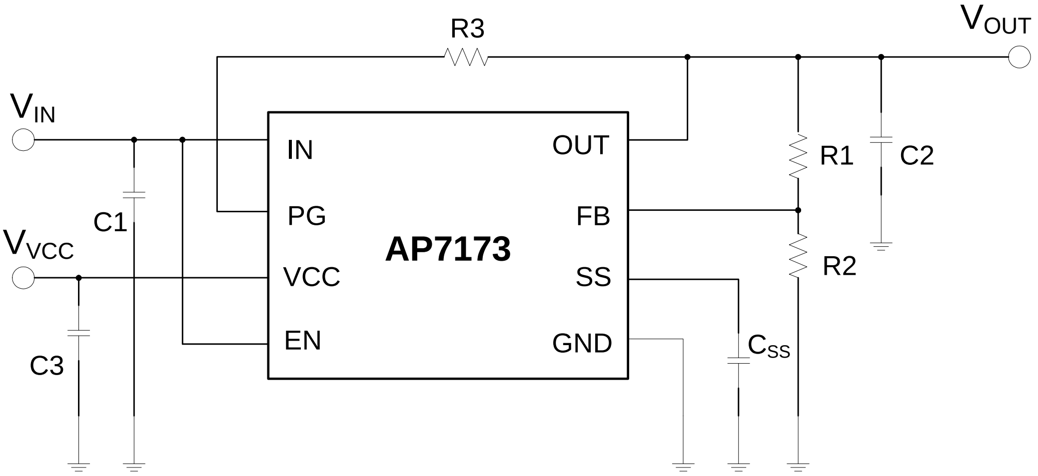


Figure 1. Typical Application Circuit (Adjustable Output)

Typical Application Circuit (Continued)

Table 1. Resistor Values for Programming the Output Voltage (Note 3)

R_1 (kΩ)	R_2 (kΩ)	V_{OUT} (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

(Note: 3) $V_{OUT} = 0.8 \times (1 + R_1 / R_2)$

Table 2. Capacitor Values for Programming the Soft-Start Time (Note 4)

CSS	SOFT-START TIME
Open	0.1ms
270pF	0.5ms
560pF	1ms
2.7nF	5ms
5.6nF	10ms
0.01µF	18ms

(Note: 4) $t_{SS}(s) = 0.8 \times C_{SS}(F) / (4.4 \times 10^{-7})$

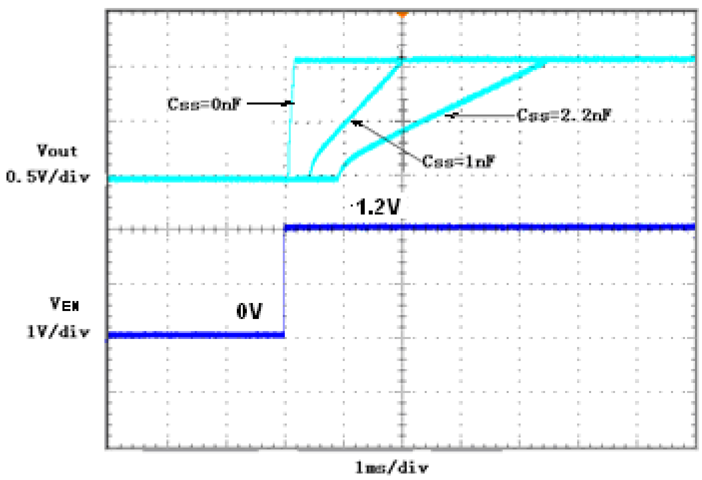


Figure 2. Turn-On Response

Absolute Maximum Ratings (Note 5)

Symbol	Parameter	Ratings	Unit
ESD HBM	Human Body Model ESD Protection	4000	V
ESD MM	Machine Model ESD Protection	350	V
V_{IN}, V_{VCC}	Input Voltage Range	-0.3 to +6	V
V_{EN}	Enable Voltage Range	-0.3 to +6	V
V_{PG}	Power-Good Voltage Range	-0.3 to +6	V
V_{SS}	Soft-Start Voltage Range	-0.3 to +6	V
V_{FB}	Feedback Voltage Range	-0.3 to +6	V
V_{OUT}	Output Voltage Range	-0.3 to V_{IN} +0.3	V
I_{OUT}	Maximum Output Current	Internally Limited	
T_J	Junction Temperature Range	-40 to +150	ºC
T_{ST}	Storage Junction Temperature Range	-65 to +150	ºC

Notes: 5. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Voltage (Note 6)	1.0	5.5	V
V_{VCC}	Bias Voltage	2.7	5.5	V
I_{OUT}	Output Current	0	1.5	A
T_A	Operating Ambient Temperature	-40	85	ºC

Notes 6. At V_{IN} =1V, the maximum load currents may be lower than 1.5A.

Electrical Characteristics

At V_{EN} = 1.1V, V_{IN} = V_{OUT} + 0.5V, C_{VCC} = 0.1uF, C_{IN} = C_{OUT} = 10uF, I_{OUT} = 50mA, V_{VCC} = 5.0V, and T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
V_{IN}	Input Voltage Range		V_{OUT} + V_{DO}		5.5	V
V_{VCC}	Bias Pin Voltage Range (Note 7)		2.7		5.5	V
V_{REF}	Internal Reference (Adj.)	T_A = +25 ºC	0.792	0.8	0.808	V
V_{OUT}	Output Voltage Range	V_{IN}= 5V, I_{OUT}= 1.5A	0.8		3.3	V
	Accuracy (Note 8)	2.97V $\leq V_{VCC} \leq$ 5.5V, 50mA $\leq I_{OUT} \leq$ 1.5A	–2	±0.5	2	%
$\Delta V_{OUT} / \Delta V_{IN} / V_{OUT}$	Line Regulation	$V_{OUT (NOM)}$ + 0.5 $\leq V_{IN}$, 5.5V		0.03		%/V
$\Delta V_{OUT} / V_{OUT} / \Delta I_{OUT}$	Load Regulation	50mA $\leq I_{OUT} \leq$ 1.5A		0.09		%/A
V_{DO}	Dropout Voltage (Note 9)	I_{OUT} = 1.5A, $V_{VCC}–V_{OUT(NOM)} \geq$ 3.25V		165	270	mV
		I_{OUT}= 1.5A, V_{IN} = V_{VCC}		1.5	1.7	V
I_{CL}	Current Limit	V_{OUT} = 80% x $V_{OUT (NOM)}$	2	3	4	A
I_{SHORT}	Short-Circuit Current	V_{OUT} < 0.2V	0.6	1		A
I_{VCC}	Bias Pin Current			1	2	mA
I_{SHDN}	Shutdown Supply Current (I_{GND})	$V_{EN} \leq$ 0.4V		1	50	µA
I_{FB}	Feedback Pin Current		–1	0.1	1	µA
PSRR	Power-Supply Rejection (V_{IN} to V_{OUT})	1KHz, I_{OUT}= 1A, V_{IN}= 1.8V, V_{OUT}= 1.5V		60		dB
		300KHz, I_{OUT} =1A, V_{IN}= 1.8V, V_{OUT} =1.5V		30		
	Power-SupplyRejection (V_{VCC} to V_{OUT})	1KHz, I_{OUT} = 1A, V_{IN}= 1.8V, V_{OUT} =1.5V		50		dB
		300KHz, I_{OUT} = 1A, V_{IN}= 1.8V, V_{OUT} =1.5V		30		
T_{ST}	Startup Time	R_{LOAD} for I_{OUT} = 1.0A, C_{SS} = open		100		µS
I_{SS}	Soft-Start Charging Current	V_{SS}= 0.4V		440		nA
$V_{EN, HI}$	Enable Input High Level		1.1		5.5	V
$V_{EN, LO}$	Enable Input Low Level		0		0.4	V
$V_{EN, HYS}$	Enable Pin Hysteresis			50		mV
I_{EN}	Enable Pin Current	V_{EN}= 5V		0.1	1	µA
$V_{PG, TH}$	PG Trip Threshold	V_{OUT} decreasing	85	90	94	$\%V_{OUT}$
$V_{PG, HYS}$	PG Trip Hysteresis			3		$\%V_{OUT}$
$V_{PG, LO}$	PG Output Low Voltage	I_{PG}= 1mA (sinking), V_{OUT}<$V_{PG, TH}$			0.3	V
$I_{PG, LKG}$	PG Leakage Current	V_{PG}= 5.25V, V_{OUT}>$V_{PG, TH}$		0.1	1	µA
T_{SD}	Thermal Shutdown Temperature	Shutdown, temperature increasing		+150		ºC
		Reset, temperature decreasing		+130		
θ_{JA}	Thermal Resistance Junction-to-Ambient	DFN3030-10 (Note 10)		38		ºC/W
		SOP-8L-EP (Note 11)		30		

Notes:
7. V_{VCC} should be higher or equal to V_{IN} in this chip.
8. Tested at 0.8V; resistor tolerance is not taken into account.
9. Dropout is defined as the voltage from V_{IN} to V_{OUT} when V_{OUT} is 3% below nominal.
10. Test condition for DFN3030-10: Device mounted on FR-4 substrate (2s2p), 2"*2" PCB, with 2oz copper trace thickness and large pad pattern.
11. Test condition for SOP-8L-EP: Device mounted on FR-4 substrate (2s2p), 2"*2" PCB, with 2oz copper trace thickness and large pad pattern.

Typical Performance Characteristics

At T_A = +25℃, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{VCC} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{VCC} = 4.7µF, and C_{OUT} = 10µF, unless otherwise noted.

V_{IN} LINE REGULATION

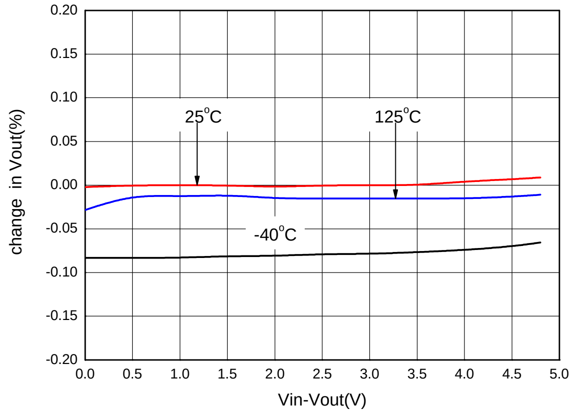


Figure 3

V_{VCC} LINE REGULATION

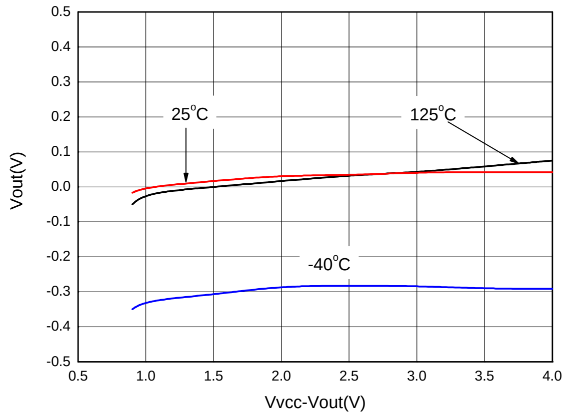


Figure 4

LOAD REGULATION

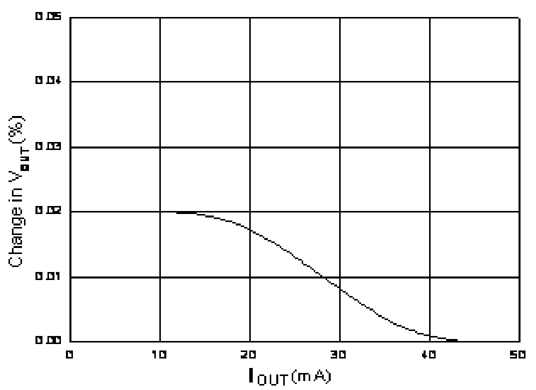


Figure 5

LOAD REGULATION

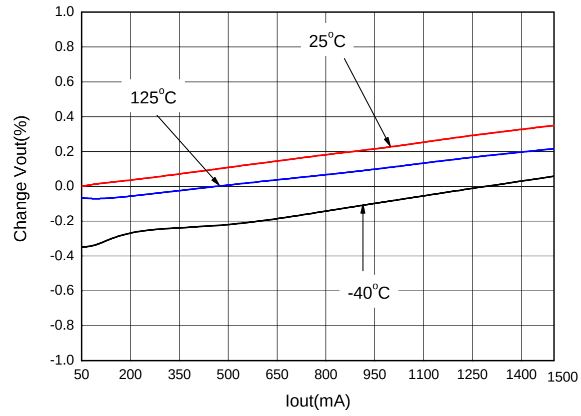


Figure 6

V_{IN} DROPOUT VOLTAGE vs. I_{OUT} AND TEMPERATURE(T_A)

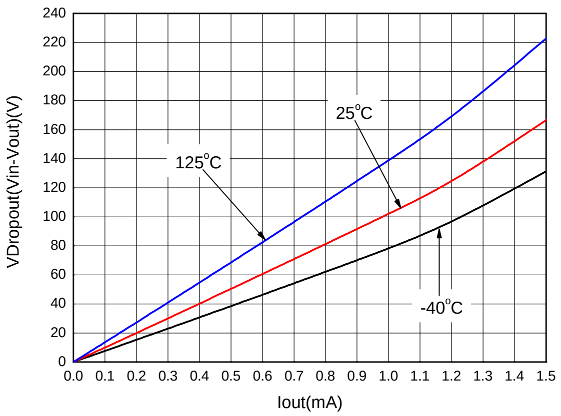


Figure 7

V_{IN} DROPOUT VOLTAGE vs. (V_{VCC}-V_{OUT}) AND TEMPERATURE(T_A)

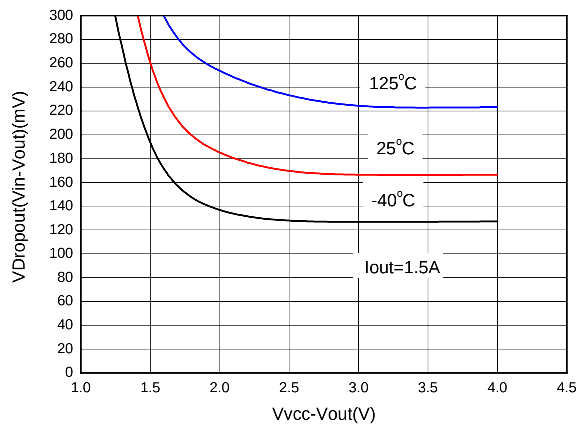


Figure 8

Typical Performance Characteristics (Continued)

At T_A = +25℃, $V_{IN} = V_{OUT(TYP)}$ + 0.3V, V_{VCC} = 5V, I_{OUT} = 50mA, $V_{EN} = V_{IN}$, C_{IN} = 1µF, C_{VCC} = 4.7µF, and C_{OUT} = 10µF, unless otherwise noted.

V_{IN} DROPOUT VOLTAGE vs. (V_{VCC}-V_{OUT}) AND TEMPERATURE(T_A)

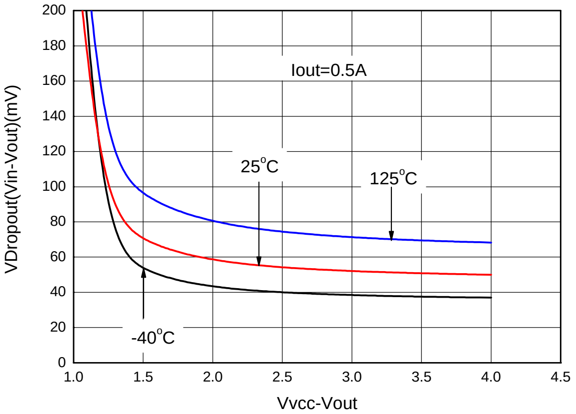


Figure 9

V_{VCC} DROPOUT VOLTAGE vs. I_{OUT} AND TEMPERATURE(T_A)

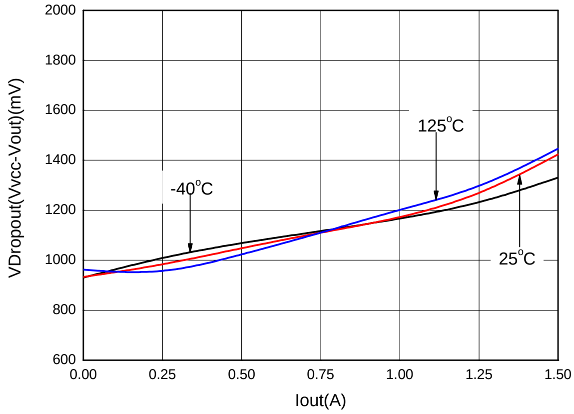


Figure 10

V_{IN} PSRR vs. FREQUENCY

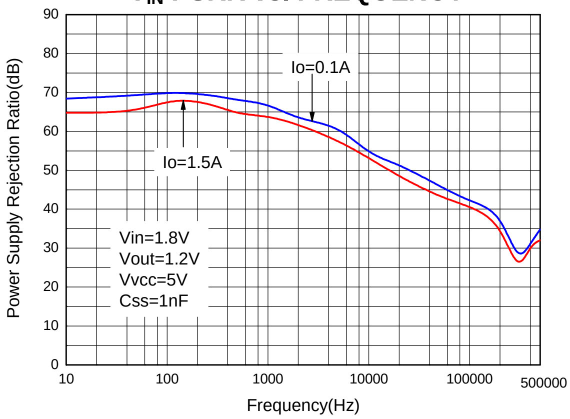


Figure 11

V_{VCC} PSRR vs. FREQUENCY

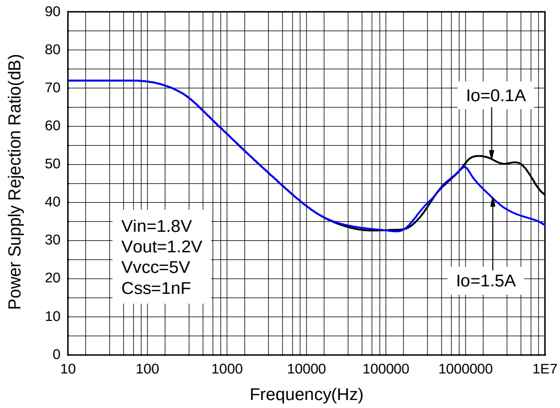


Figure 12

V_{IN} PSRR vs. (V_{IN}-V_{OUT})

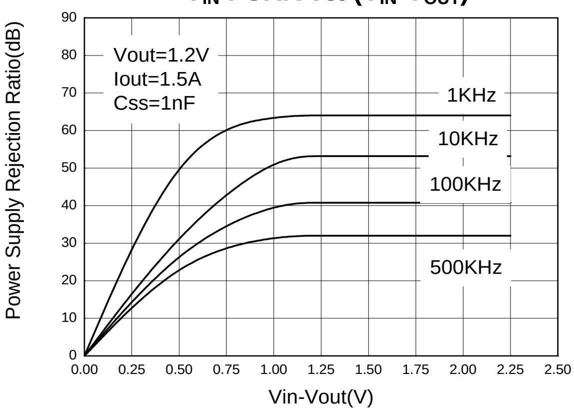


Figure 13

LOW-LEVEL PG VOLTAGE vs. CURRENT

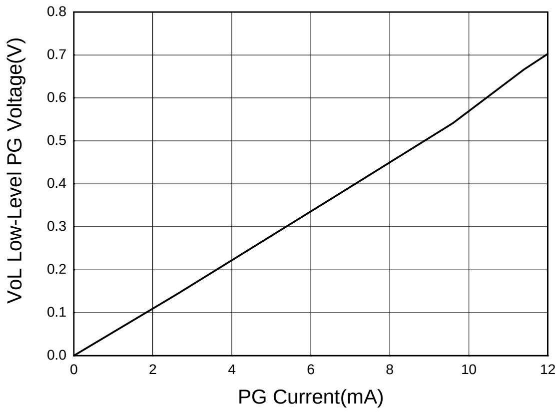


Figure 14

Typical Performance Characteristics (Continued)

At T_A = +25℃, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{VCC} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{VCC} = 4.7µF, and C_{OUT} = 10µF, unless otherwise noted.

V_{IN} LINE TRANSIENT

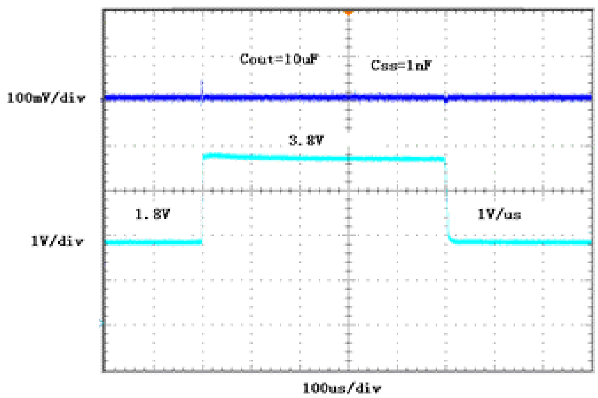


Figure 15

V_{VCC} LINE TRANSIENT

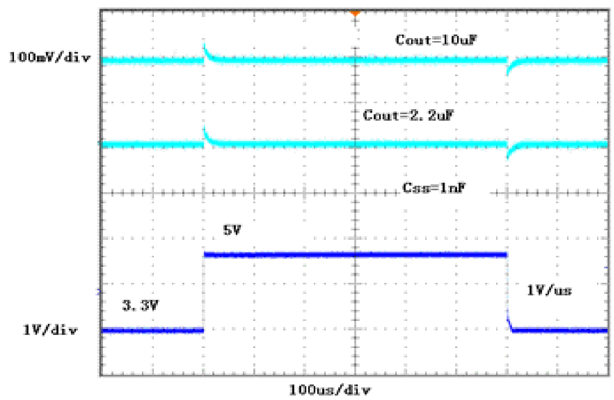


Figure 16

OUTPUT LOAD TRANSIENT

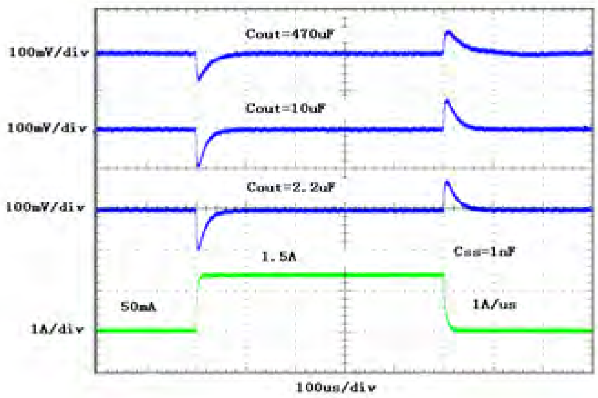


Figure 17

TURN-ON RESPONSE

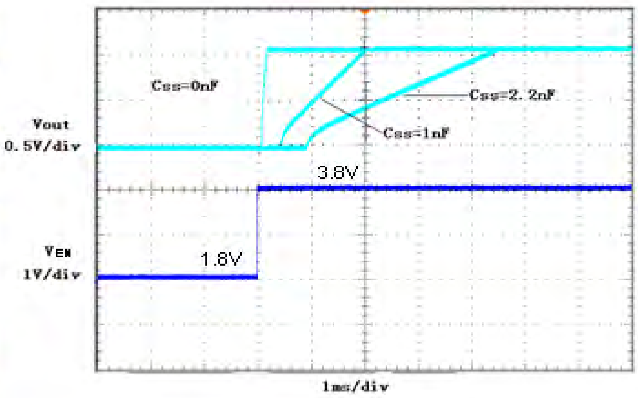


Figure 18

VCC PIN CURRENT vs. I_{OUT} AND TEMPERATURE (T_A)

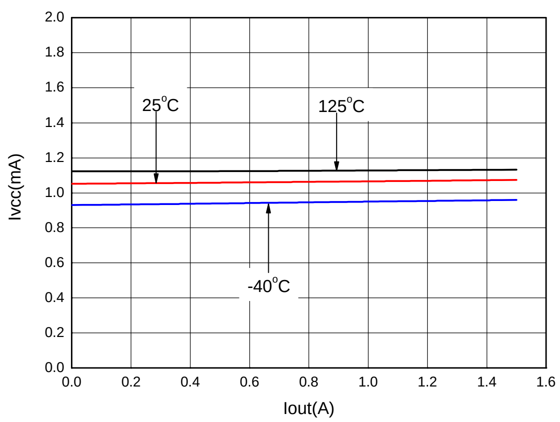


Figure 19

VCC PIN CURRENT vs. V_{VCC} AND TEMPERATURE (T_A)

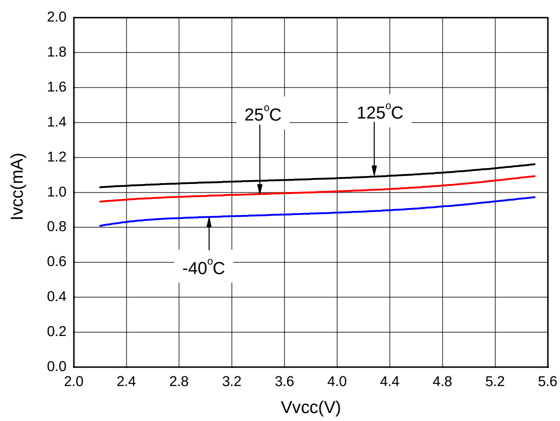


Figure 20

Typical Performance Characteristics (Continued)

At T_A = +25℃, V_{IN} = $V_{OUT(TYP)}$ + 0.3V, V_{VCC} = 5V, I_{OUT} = 50mA, V_{EN} = V_{IN}, C_{IN} = 1µF, C_{VCC} = 4.7µF, and C_{OUT} = 10µF, unless otherwise noted.

QUIESCENT CURRENT vs. I_{OUT}

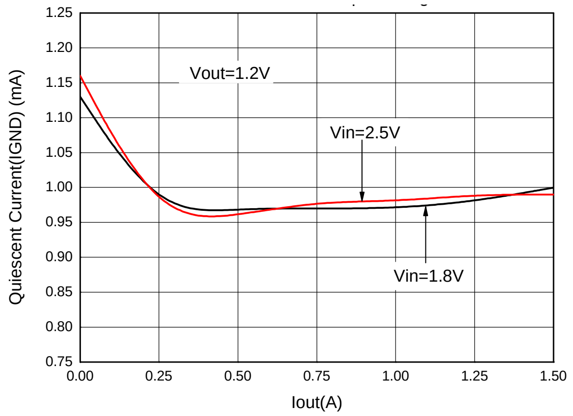


Figure 21

QUIESCENT CURRENT vs. V_{VCC}

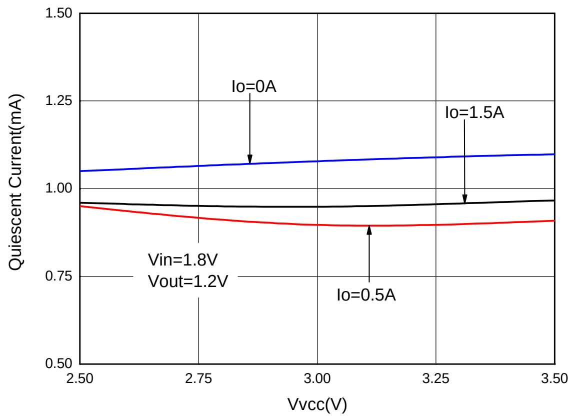


Figure 22

QUIESCENT CURRENT vs. TEMPERATURE

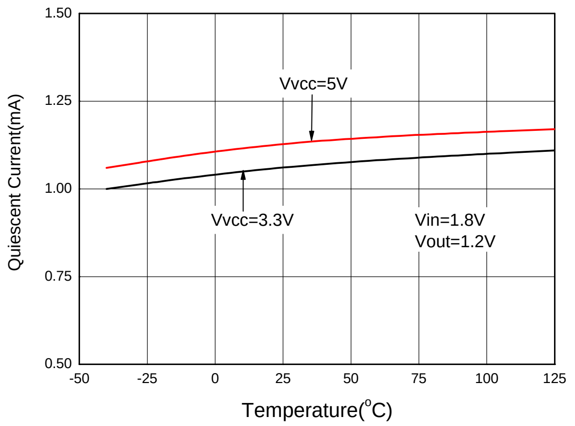


Figure 23

CURRENT LIMIT vs. (V_{VCC} – V_{OUT})

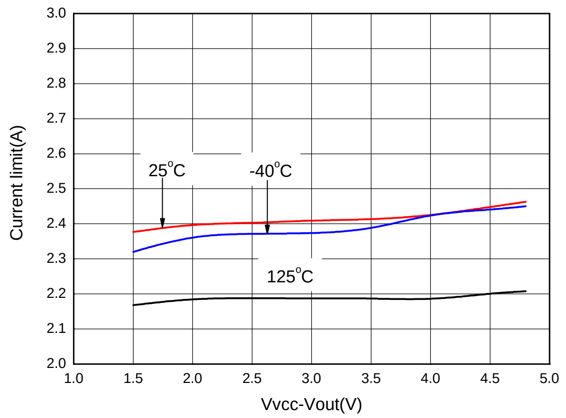


Figure 24

SOFT-START CHARGING CURRENT (I_{SS}) vs. TEMPERATURE

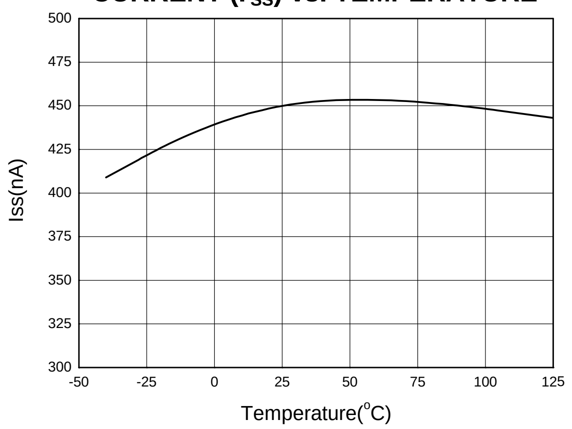


Figure 25

POWER-UP/POWER-DOWN

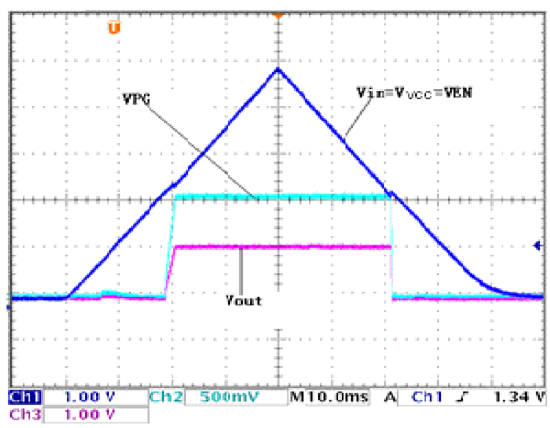


Figure 26

Application Note

BIAS VOLTAGE V_{VCC}

The AP7173 is a low V_{IN}, low dropout regulator that uses an NMOS pass FET. The VCC pin must be connected to a DC bias supply V_{VCC} for the internal control circuitry and the gate drive of the pass FET to function properly and to obtain low dropout. The V_{VCC} needs to be equal to or higher than the V_{IN} and in the range of 2.7V-5.5V. Figure 27 illustrates the typical application circuit for the AP7173.

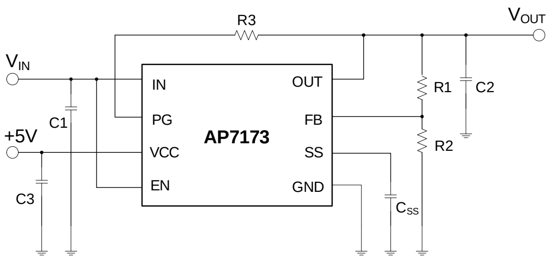


Figure 27. Typical Application Circuit for AP7173

ADJUSTABLE OUTPUT VOLTAGE

With an external voltage divider, the AP7173 can provide output voltage from 0.8V to 3.3V. R1 and R2 can be calculated for any output voltage using the following equation, where V_{REF}=0.8 is the AP7173's internal reference voltage. Refer to Table 1 for resistor combinations for commonly used output voltages. For maximum voltage accuracy, R2 should be ≤ 5kΩ.

$$V_{OUT} = V_{REF} \text{ x } (1 + R1/R2)$$

INPUT V_{IN} AND BIAS V_{VCC} CAPACITORS

It is important to keep the IN and VCC pins clear of large ripples, glitches and other noises by connecting capacitors to the IN and VCC pins. The required capacitance on these pins is strongly dependent on source and wiring impedance of the supplies.

To provide good decoupling for the input power supply V_{IN}, it is recommended that a ceramic capacitor with capacitance of at least 1μF is connected between the IN and GND pins at a location as close to them as possible. High quality, low ESR capacitors should be used for better performance.

It is critical to provide good decoupling to the VCC pin for the AP7173's internal control circuitry to function properly. The minimum recommended capacitance for the V_{VCC} is 1μF when the V_{VCC} and V_{IN} are separate supplies. If the V_{IN} and V_{VCC} are connected to the same supply, the recommended minimum capacitance for V_{VCC} is 4.7μF. Again good quality, low ESR capacitors should be used for optimum performance.

OUTPUT CAPACITOR

The output capacitor affects the stability and transient response of the LDO. The AP7173 is designed to be stable for all types of output capacitors ≥ 2.2μF, single or multiple in parallel. Using high-quality, low ESR capacitors and placing them close to the OUT and GND pins can improve perfomance.

DROPOUT VOLTAGE

The very low dropout makes the AP7173 well suited for high-current, low V_{IN}/low V_{OUT} applications. To achieve the specified low-dropout performance for such applications, the VCC pin should be connected to a separate supply of at least 3.25V higher than V_{OUT}. Figure 28 shows an application circuit where V_{VCC} is 5V and V_{OUT} is 1.2V.

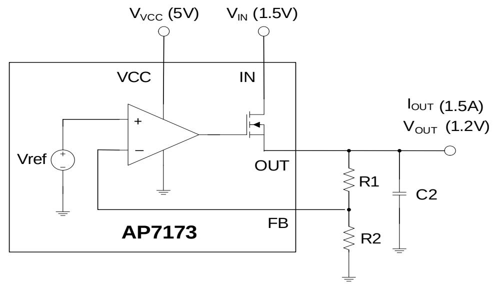


Figure 28. Typical Application Circuit for AP7173 Using Separate VCC and IN Rails

For applications where low dropout is not required or a separate V_{VCC} supply is not available, the IN and VCC pins can be tied together. In this situation, a voltage difference of at least 1.7V between the V_{VCC} and V_{OUT} has to be maintained for the V_{VCC} to provide enough gate drive to the pass FET. Therefore, the V_{OUT} needs to be 1.7V or more below V_{IN}, as shown in Figure 29.

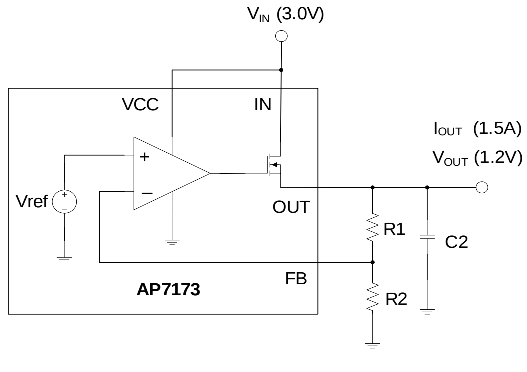


Figure 29. Typical Application Circuit for AP7173 Without an Auxiliary VCC Rail

PROGRAMMABLE SOFT-START

The AP7173 features a voltage-controlled soft-start that is programmable with an external capacitor (C_{SS}). The AP7173 achieves a monotonic soft-start by tracking the voltage ramp of the external soft-start capacitor until the ramp voltage reaches the internal reference voltage. The relationship between the soft-start time and the soft-start charging current (I_{SS}), soft-start capacitance (C_{SS}), and the internal reference voltage (V_{REF}) is

$$t_{SS} = (V_{REF} \text{ x } C_{SS}) / I_{SS}$$

Refer to Table 2 for suggested soft-start capacitor values.

Application Note (Continued)

ENABLE/SHUTDOWN

The EN pin can be used with standard digital signals or relatively slow-ramping analog signals. Pulling the V_{EN} below 0.4V turns the regulator off, while driving the V_{EN} above 1.1V turns the regulator on. Figure 30 shows an example where an RC circuit is used to delay start the AP7173.

If not used, the EN pin can be connected to the VCC or IN pin when the V_{IN} is greater than 1.1V, as long as good decoupling measures are taken for the EN pin.

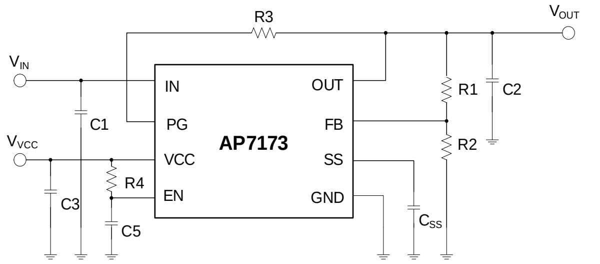


Figure 30. Delayed Start Using an RC Circuit to Enable AP7173

POWER-GOOD

The power-good (PG) pin is an open-drain output and can be pulled up through a resistor of 10kΩ to1MΩ to V_{IN}, V_{OUT} or any other rail that is 5.5V or lower. When the $V_{OUT} \geq V_{PG,TH}+V_{PG,HYS}$, the PG output is high-impedance; if the V_{OUT} drops to below $V_{PG,TH}$, $V_{VCC} \leq 1.9V$ or the device is disabled, the PG pin is pulled to low by an internal MOSFET.

OVER-CURRENT AND SHORT-CIRCUIT PROTECTION

The AP7173 features a factory-trimmed, temperature and supply voltage compensated internal current limit and an over-current protection circuitry to protect the device against overload conditions. It limits the device current to a typical value of 3A and reduces the V_{OUT} when the load tries to pull more current.

For more effective protection against short-circuit failure, the AP7173 also includes a short-circuit foldback mechanism that lowers the current limit to a typical value of 1.0A when the V_{FB} drops to below 0.2V.

THERMAL PROTECTION

Thermal shutdown limits the AP7173 junction temperature and protects the device from damage as a result of overheating.

Thermal protection turns off the V_{OUT} when the AP7173's junction temperature rises to approximately +150°C, allowing it to cool down. When the junction temperature drops to approximately +130°C, the output is re-enabled. Therefore, the thermal protection circuit may cycle on and off at a rate dependent on the power dissipation, thermal resistance, and ambient temperature.

POWER DISSIPATION

Thermal shutdown is intented to protect the AP7173 against abnormal overheating. For normal operation, excessive power dissipation should be avoided and good heatsinking should be provided. Power dissipation in the device is the product of the device dropout voltage and the load current,

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

As can be seen, power dissipation can be minimized by using the lowest input voltage necessary to achieve the required output voltage regulation.

To ensure that the device junction temperature does not exceed the specified limit of 125°C, an application should provide heat conduction paths that have junction-to-ambient thermal resistance lower than the calculated value here:

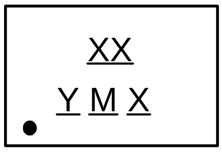
$$R_{\theta JA} = (125°C - T_A) / P_D$$

For the DFN package with exposed pad, the primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad should be attached to an appropriate amount of copper PCB area to ensure that the device does not overheat.

Marking Information

(1) DFN3030-10

(Top View)

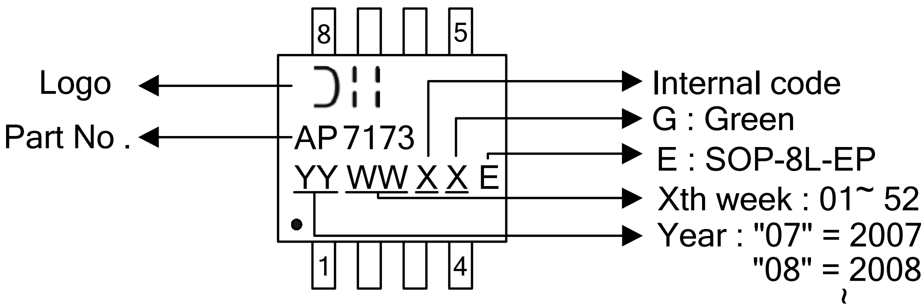


XX : BA : AP7173
Y : Year 0~9
M : Month A~L
X : A~Z : Green

Part Number	Package	Identification Code
AP7173	DFN3030-10	BA

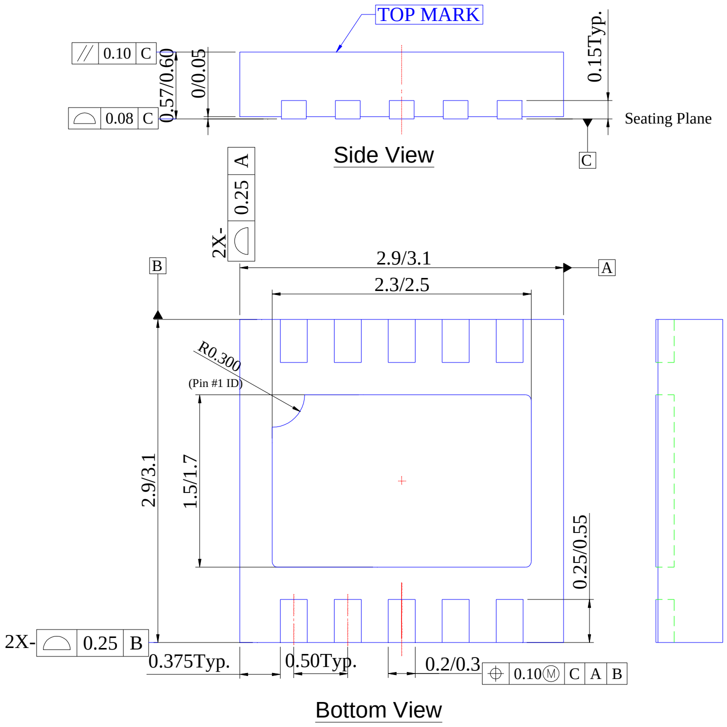
(2) SOP-8L-EP

(Top View)

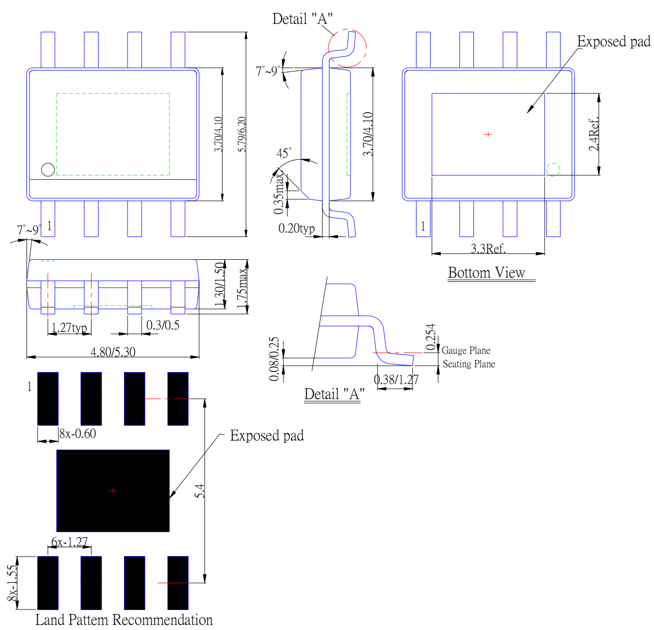


Package Information (All Dimensions in mm)

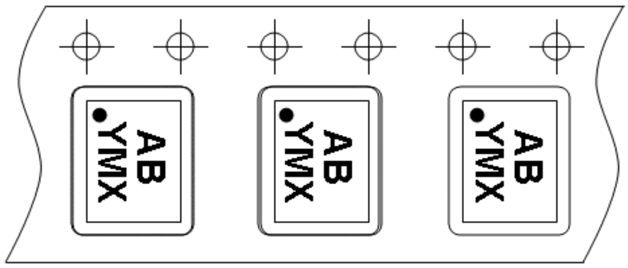
(1) DFN3030-10

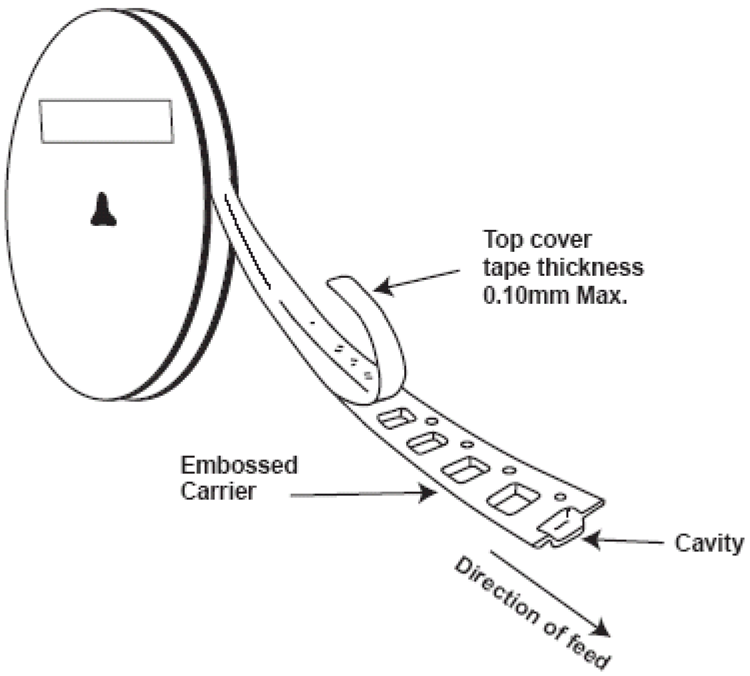


(2) SOP-8L-EP



Taping Orientation





Notes: 12. The taping orientation of the other package type can be found on our website at http://www.diodes.com/datasheets/ap02007.pdf