



## AS3336G

## Precision Multiple Analog Switches

### ■ General Description

The AS3336 consist of four independently controlled single-pole double-throw analog switches along with several logic gates. This precision multiple analog switch is designed to control, multiplex & de-multiplex analog signals with a high degree of accuracy. An improved charge injection compensation design minimizes switching transients. AS3336 is designed on an HV CMOS process, resulting in higher speed and lower power consumption. Each switch conducts equally well in both directions when on. When off, they block voltages up to the power-supply levels.

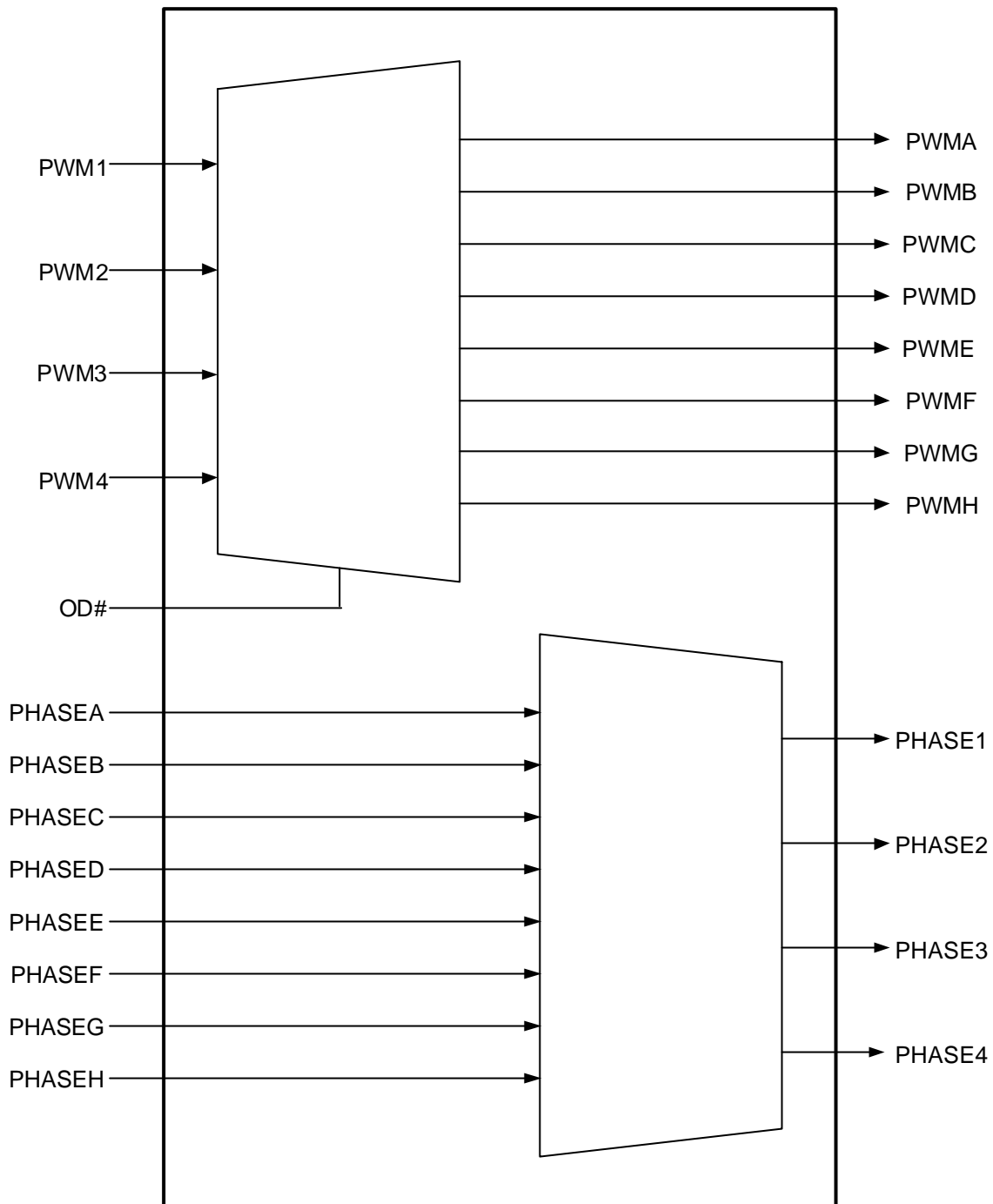
### ■ Features

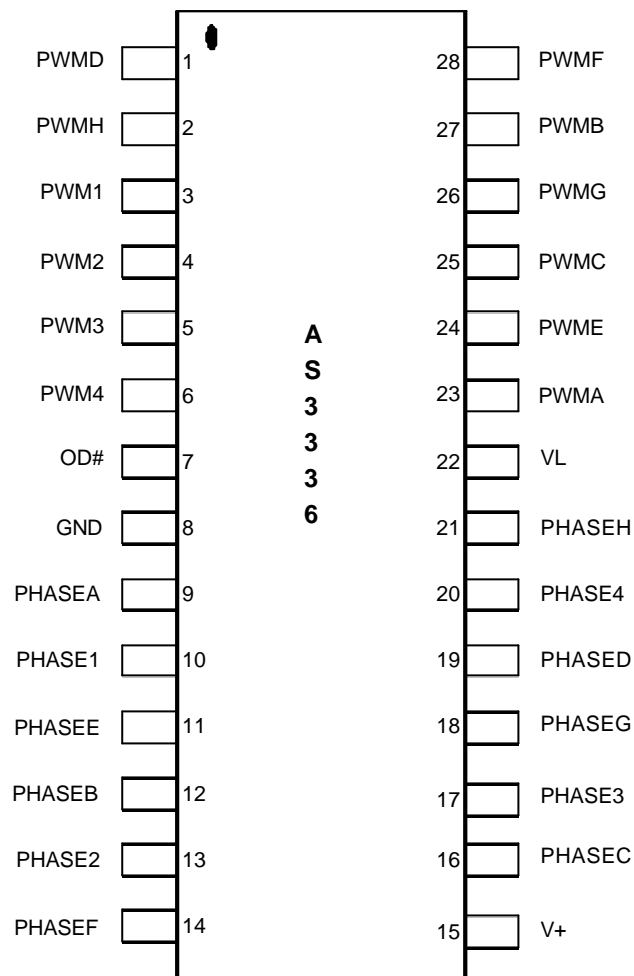
- 12V Supply Maximum Ratings
- Low On-Resistance ( $45\Omega$  max)
- Flat On-Resistance Over Analog Signal Range ( $\Delta 10\Omega$  max)
- Low On-Resistance Match Between Channel ( $4\Omega$  max)
- Low Power Dissipation
- Fast Switching Times  
 $t_{ON} < 175$  ns  
 $t_{OFF} < 145$  ns
- Low Leakage Currents ( $3.5$  nA max) on analog switches
- Low Charge Injection ( $10$  pC max)
- Low Charge Injection ( $10$  pC max)
- All AME's Lead Free Products Meet RoHS Standards

### ■ Applications

- Audio Switching
- Test Equipment
- Portable Instrumentation
- Communication Systems

## ■ Functional Block Diagram



**■ Pin Configuration**

**Figure 1. Pin Diagram (Top View)**
**■ Pin Description**

I/O TYPE DESCRIPTION

I/O Type	Function
I	Input Pin
O	Output Pin
PWR	Power Pin

**■ Pin Description (Contd.)**

Pin No.	Pin Name	I/O Type	Function Description
1	PWMD	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
2	PWMH	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
3	PWM1	I	Logic-level PWM Inputs. Each input is connected to the output of PWM. Connecting the PWM1 outputs to GND causes that phase to turn off.
4	PWM2	I	Logic-level PWM Inputs. Each input is connected to the output of PWM. Connecting the PWM2 outputs to GND causes that phase to turn off.
5	PWM3	I	Logic-level PWM Inputs. Each input is connected to the output of PWM. Connecting the PWM3 outputs to GND causes that phase to turn off.
6	PWM4	I	Logic-level PWM Inputs. Each input is connected to the output of PWM. Connecting the PWM4 outputs to GND causes that phase to turn off.
7	OD#	I	If the status is "0", the register's initial condition is pre-set, and the PWM A to H output is "Zero"; If the status is "1", the PWM A to H output is "Enable"..
8	GND	PWR	Ground. All internal biasing and the logic output signals of the device are referenced to this ground
9	PHASEA	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
10	PHASE1	I/O	Current Balance Outputs. It is generated by PHASE A and E signal.
11	PHASEE	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
12	PHASEB	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.

**■ Pin Description(Contd.)**

Pin No.	Pin Name	I/O Type	Function Description
13	PHASE2	I/O	Current Balance Outputs. It is generated by PHASE B and F signal.
14	PHASEF	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
15	V+	PWR	Most Positive Power Supply 12V
16	PHASEC	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
17	PHASE3	I/O	Current Balance Outputs. It is generated by PHASE C and G signal.
18	PHASEG	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
19	PHASED	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
20	PHASE4	I/O	Current Balance Outputs. It is generated by PHASE D and H signal.
21	PHASEH	I/O	Current Balance Inputs. Inputs for measuring the current level in each phase. The Phase pins of unused phases should be left open.
22	VL	PWR	5V for Logic Voltage Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
23	PWMA	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
24	PWME	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
25	PWMC	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
26	PWMG	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
27	PWMB	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.
28	PWMF	O	Logic-level PWM Outputs. Each output is connected to the input of an external MOSFET driver.



**AME, Inc.**

## **AS3336G**

## **Precision Multiple Analog Switches**

### **■ Ordering Information**

<b>Part Number</b>	<b>Marking</b>	<b>Package</b>	<b>Operating Ambient Temperature Range</b>
AS3336G	AS3336G yyww AA xxxxxxx ##	SSOP-28	0°C to 70°C

Note: yy:year (last two digits)

ww:week

xxxxxxx:wafer lot number

##:wafer number (It is a representative if a string of wafer are used.)

**■ Absolute Maximum Ratings**

Parameter	Max	Unit
V+ to GND	15	V
VL to GND	7	V
Analog inputs/ Outputs Voltage	GND –0.3 to 15	V
Digital inputs/ Outputs Voltage	GND –0.3 to 7	V
Continuous Current	20	mA
Peak Current (Pulsed at 1 ms, 10% duty cycle max)	40	mA
$\theta_{JA}$ , Thermal Impedance	130	°C/W

**CAUTION:**

**Note 1.** Stresses beyond those listed under “ Absolute Maximum Ratings ” may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2.** The device is not guaranteed to function outside its operating conditions.

**■ Recommended Operation Conditions**

Parameter	Symbol	Rating	Unit
Ambient Temperature Range	$T_A$	0 to 70	°C
Junction Temperature	$T_J$	- 40 to 125	°C
Storage Temperature Range	$T_{STG}$	- 65 to 125	°C

**■ Specifications**

SINGLE SUPPLY

 $V = +12V$ ,  $GND = 0V$ , unless otherwise noted

Parameter	+25°C	-40°C to +85°C	Unit	Test Conditions / Comments
ANALOG SWITCH				
Analog Signal Range		-0.3 V to $V_{DD} + 0.3$	V	$V_D = 1V, 10V, I_S = -1mA$
$R_{ON}$	35	75	$\Omega$ typ $\Omega$ max	
LEAKAGE CURRENTS <sup>1</sup>				
Source OFF leakage $I_S$ (OFF)	3.5		nA typ	
	3.5	5	nA max	
Channel ON Leakage $I_D, I_S$ (ON)	3.5		nA typ	
	3.5	5	nA max	
Logic Leakage $I_{Logic}$		1	$\mu A$ max	
DIGITAL INPUTS				
Input High Voltage, $V_{INH}$		2.6	V min	$V_{IN} = 0 V$ or $V_{DD}$
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				
$I_{INL}$ or $I_{INH}$		$\pm 0.005$	$\mu A$ typ	
		$\pm 0.5$	$\mu A$ max	
DYNAMIC CHARACTERISTICS <sup>1</sup>				
$t_{ON}$	110	200	ns typ ns max	$R_L = 300 \Omega, C_L = 35 pF$ $V_S = 8 V$ ;
$t_{OFF}$	100	180	ns typ ns max	
Break-Before-Make Delay, $t_{OPEN}$	10		ns min ns min	$R_L = 300 \Omega, C_L = 35 pF$ $V_S = 5 V$ ;
Charge Injection <sup>1</sup>	5		pC typ	
OFF Isolation <sup>1</sup>	72		dB typ	
Channel-to-Channel Crosstalk <sup>1</sup>	85		dB typ	
$C_S$ (OFF) <sup>1</sup>	12		pF typ	
$C_D, C_S$ (ON) <sup>1</sup>	25		pF typ	

1. Guaranteed by design: not subject to production test.

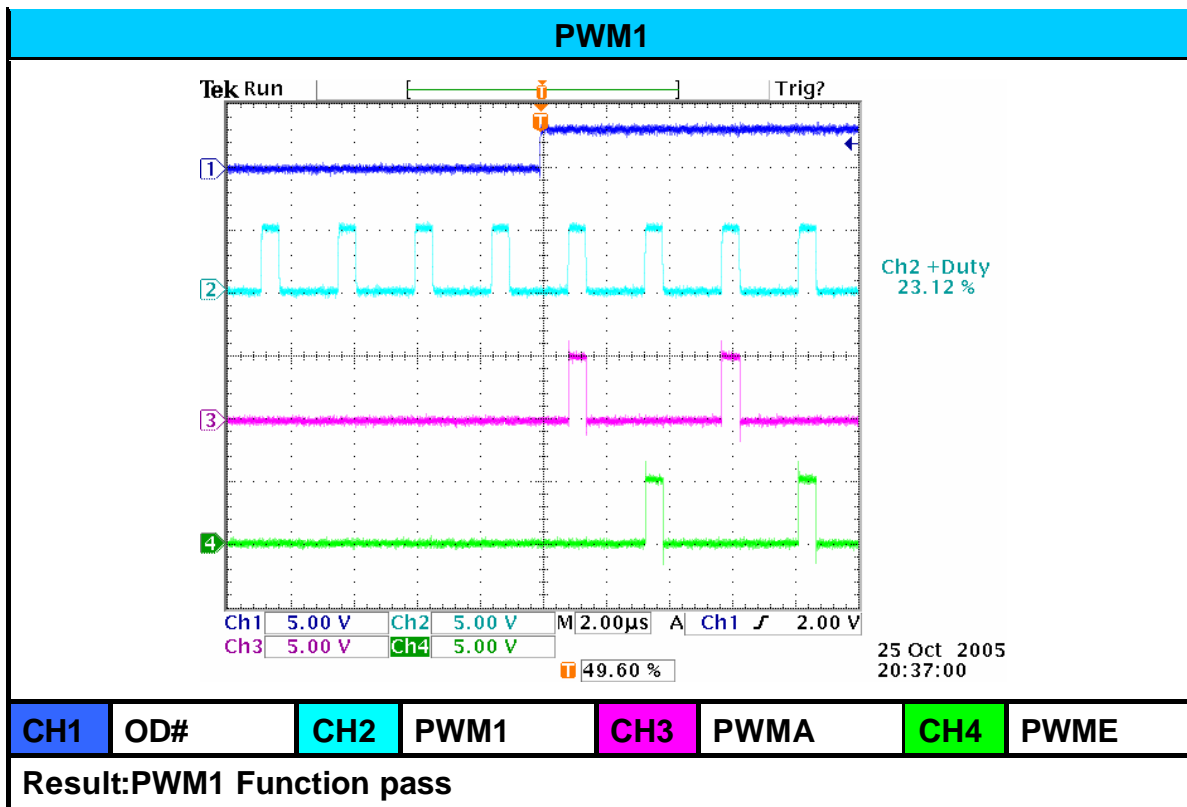


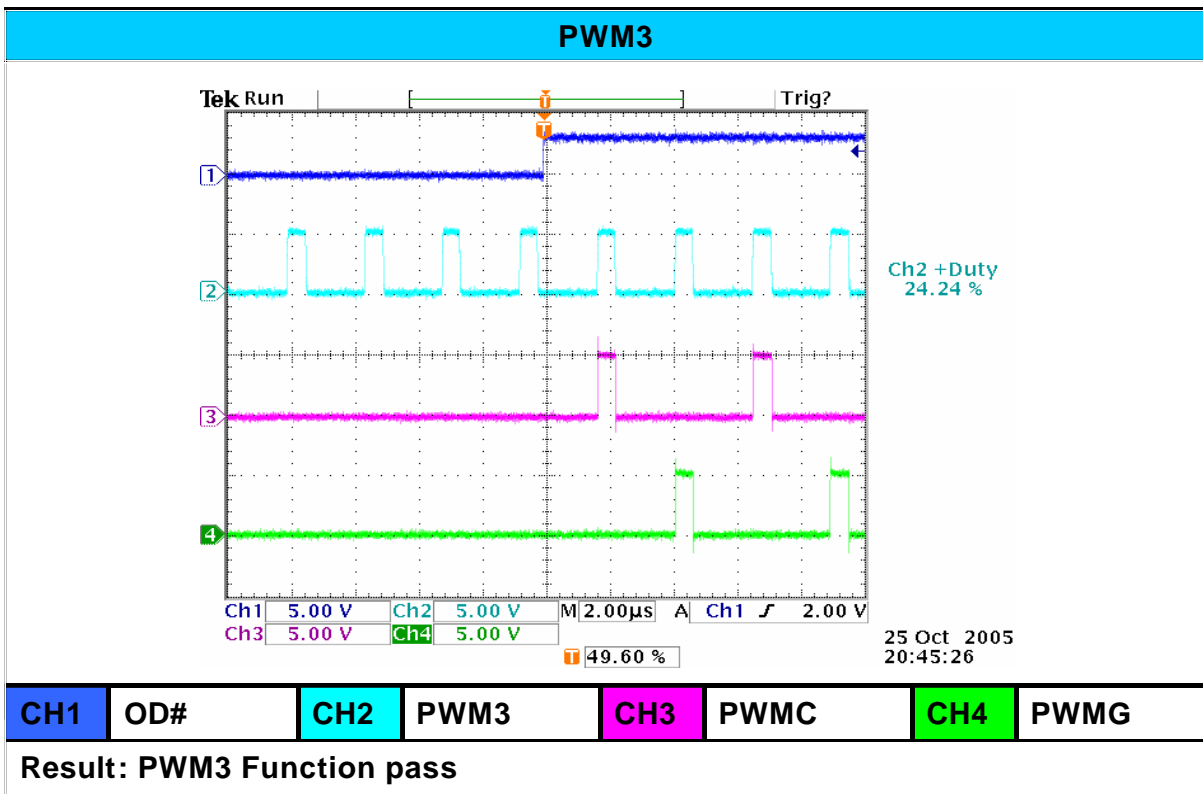
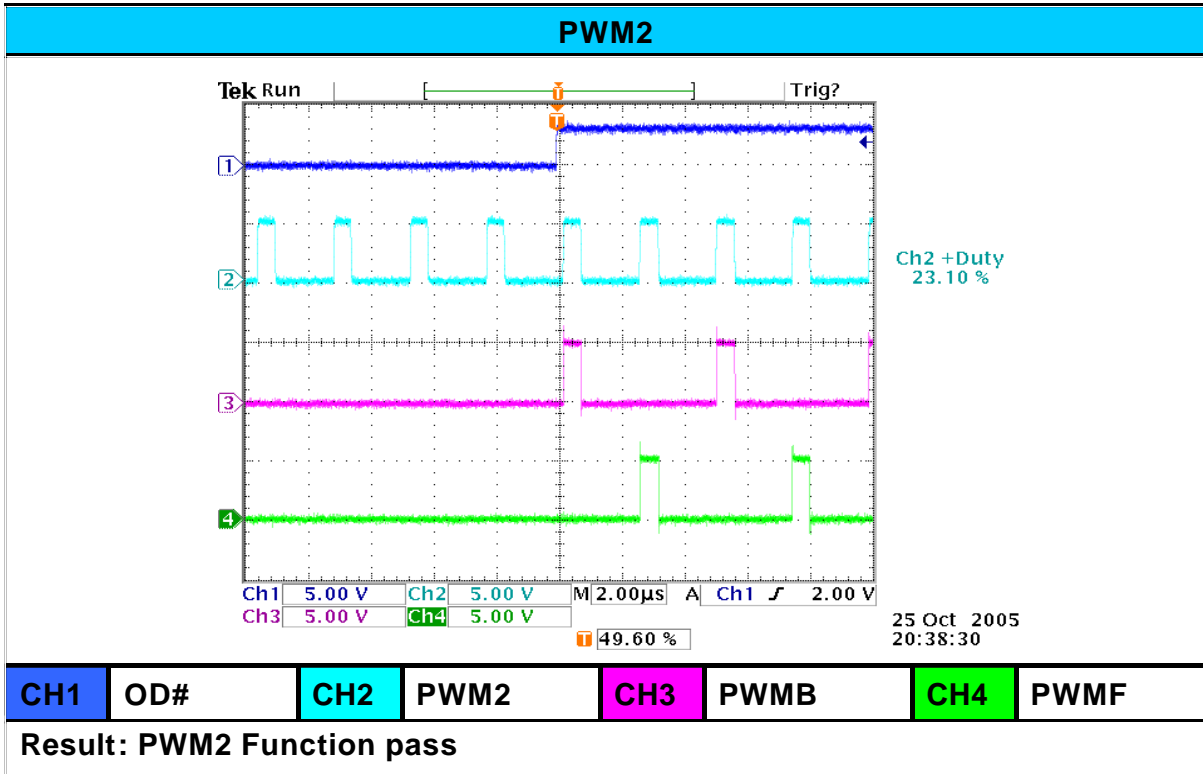
**■ Typical Performance Characteristic**
**1. Operating Current Test**

VDD pin	Spec.	IDD	Remark
Pin15 (12V)	350 $\mu$ A	120 $\mu$ A	@400KHZ
Pin22 (5V)	20mA	3mA	@400KHZ

**2. Function Test**

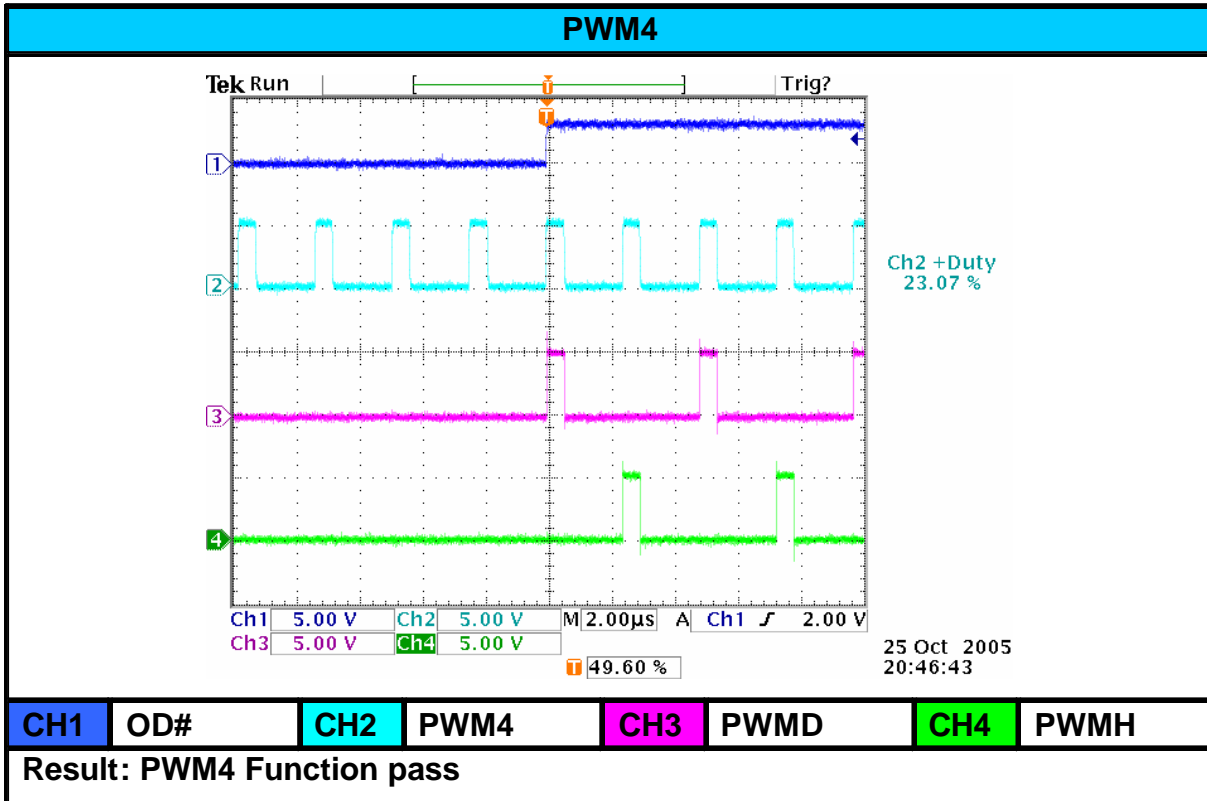
2-1 Function test of PWM pins



**Typical Performance Characteristic**


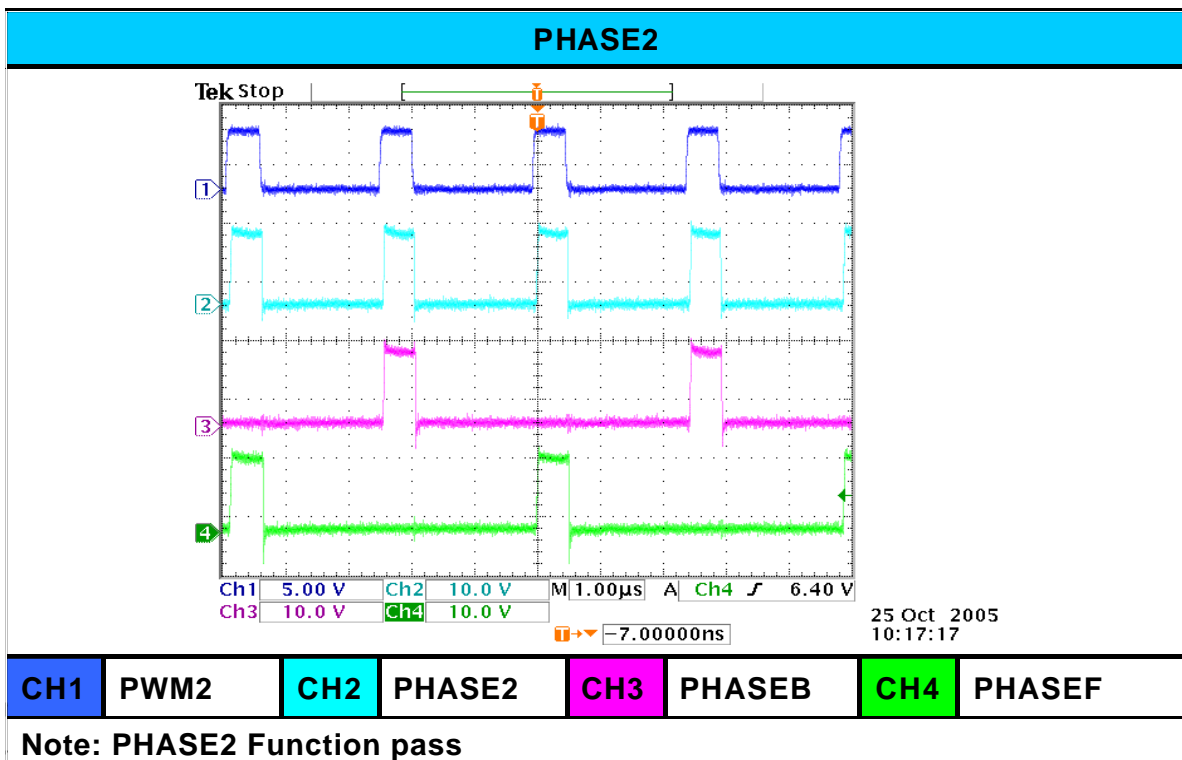
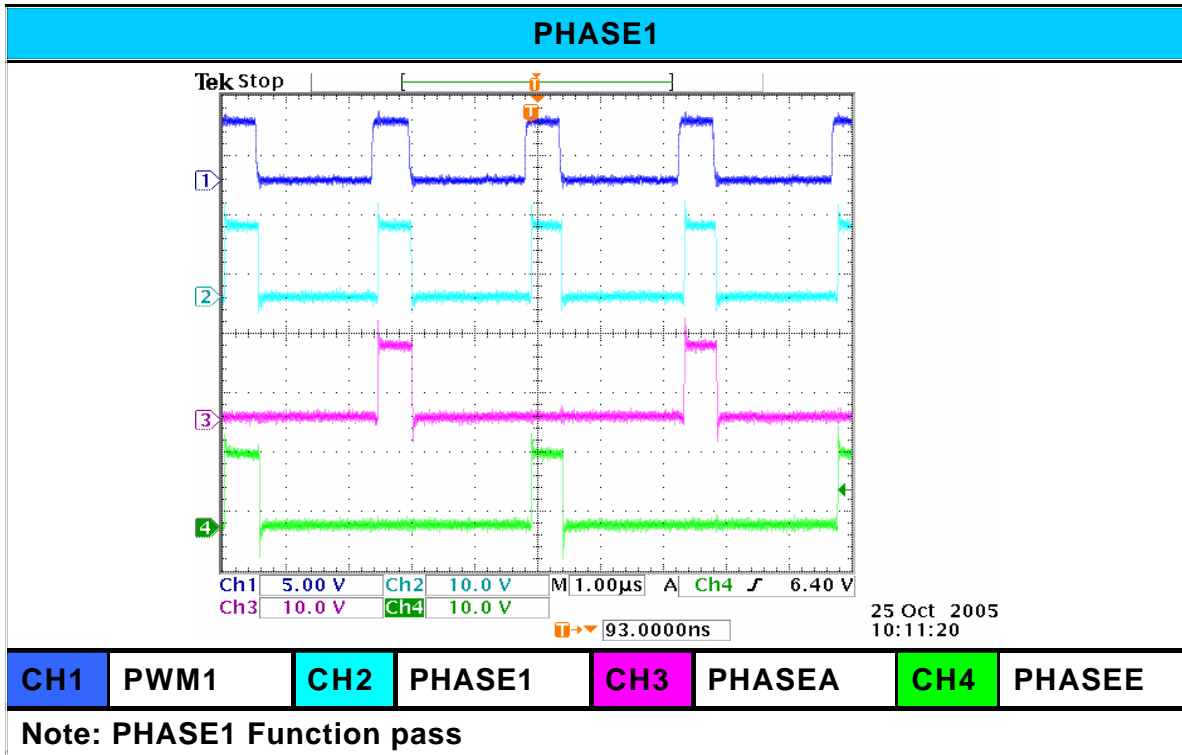


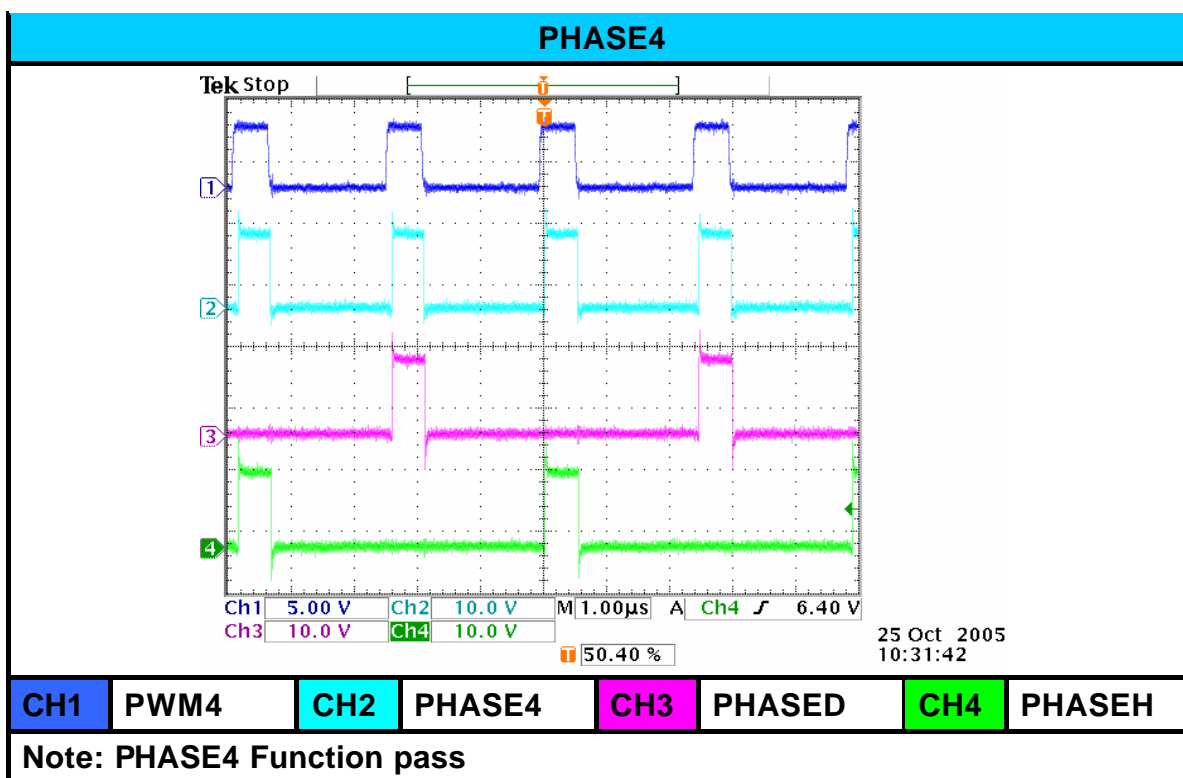
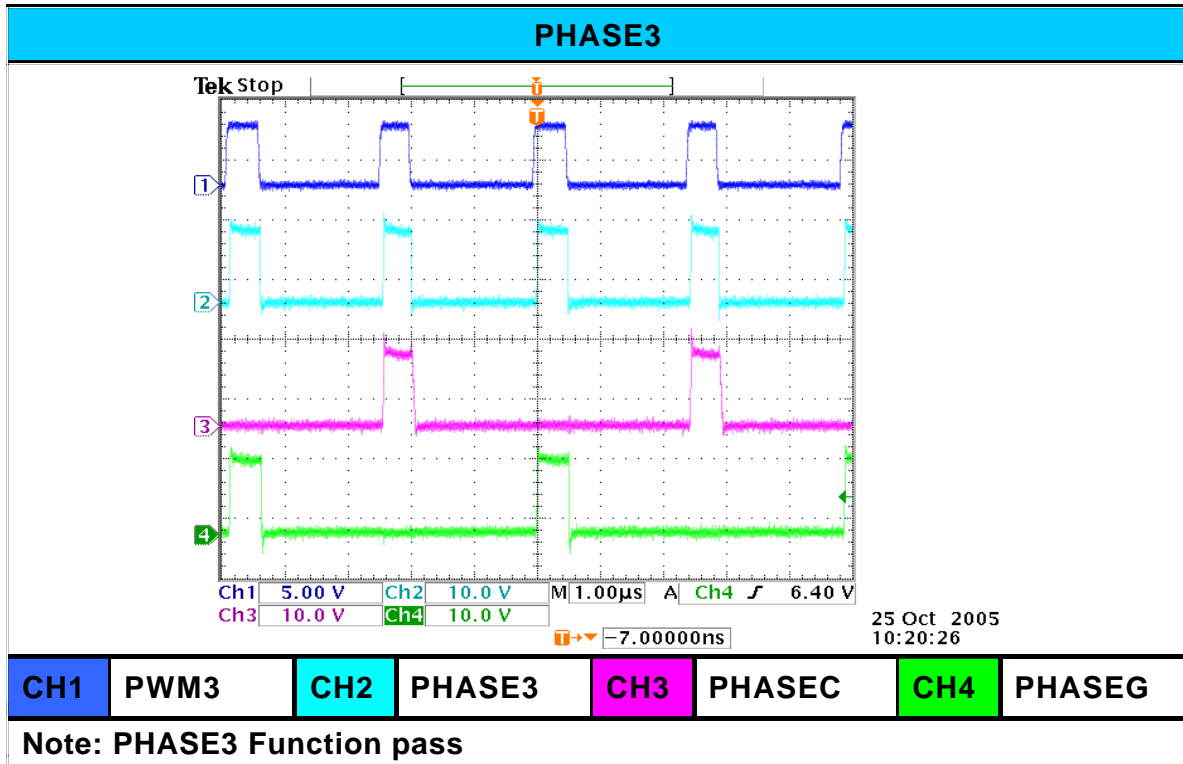
■ Typical Performance Characteristic

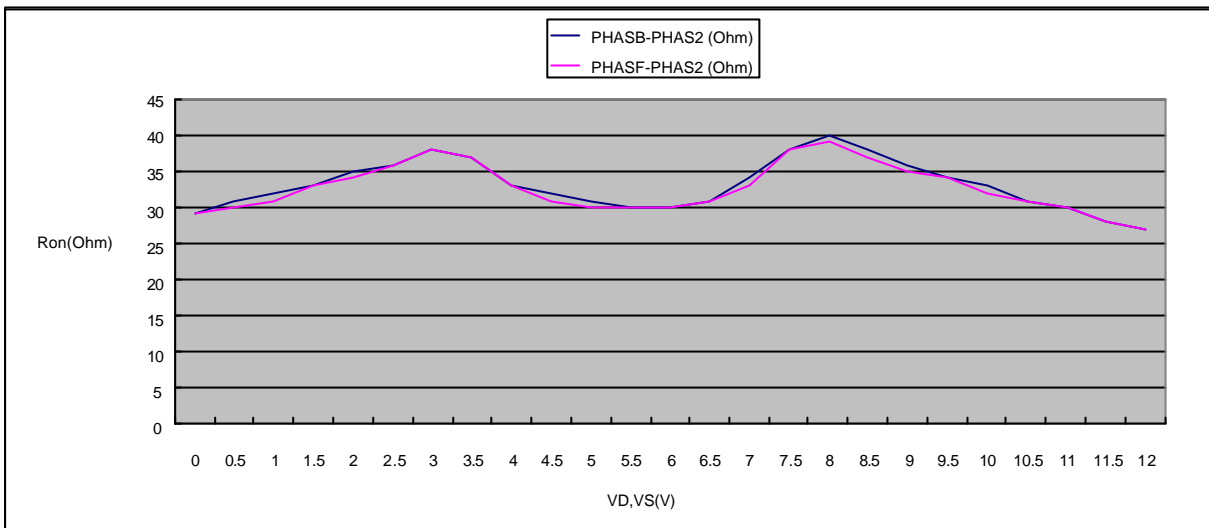
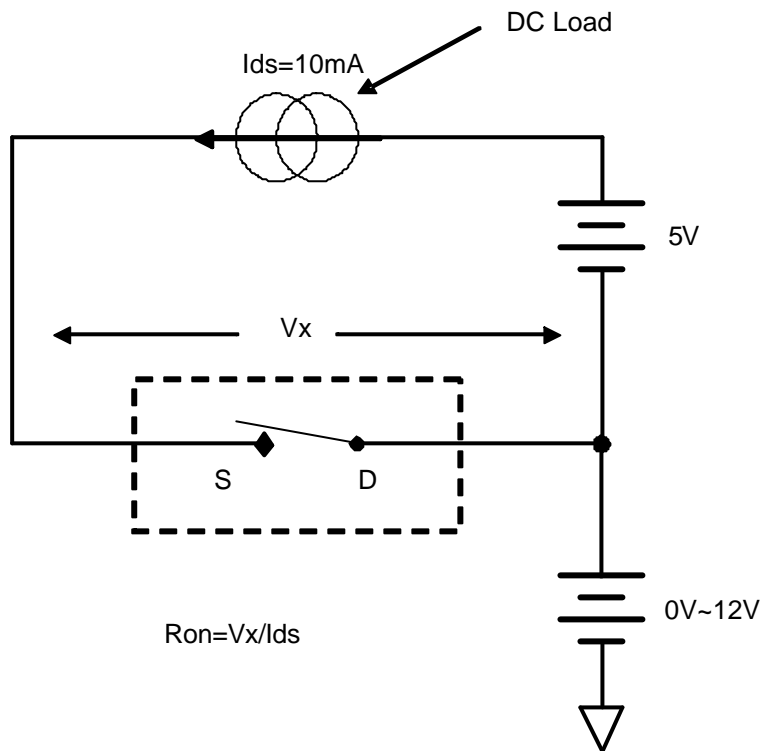


**Typical Performance Characteristic**

2-2 Function test of PHASE pins

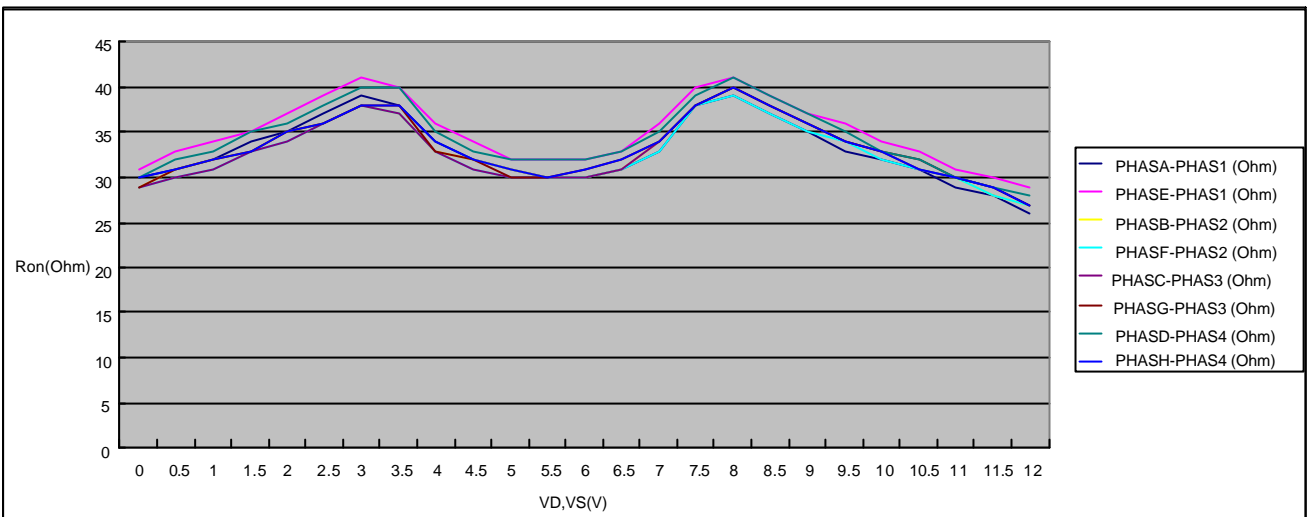
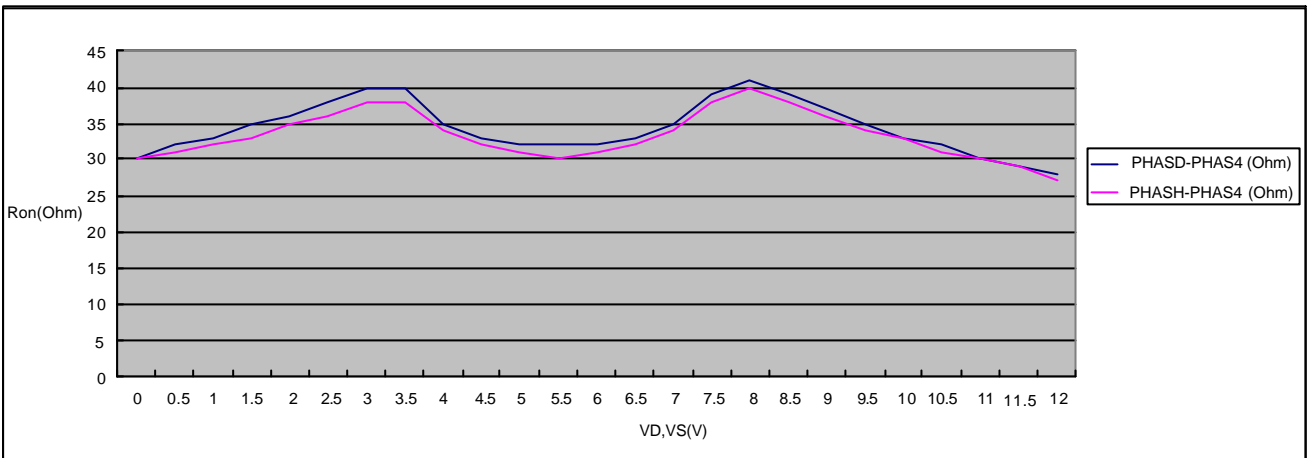
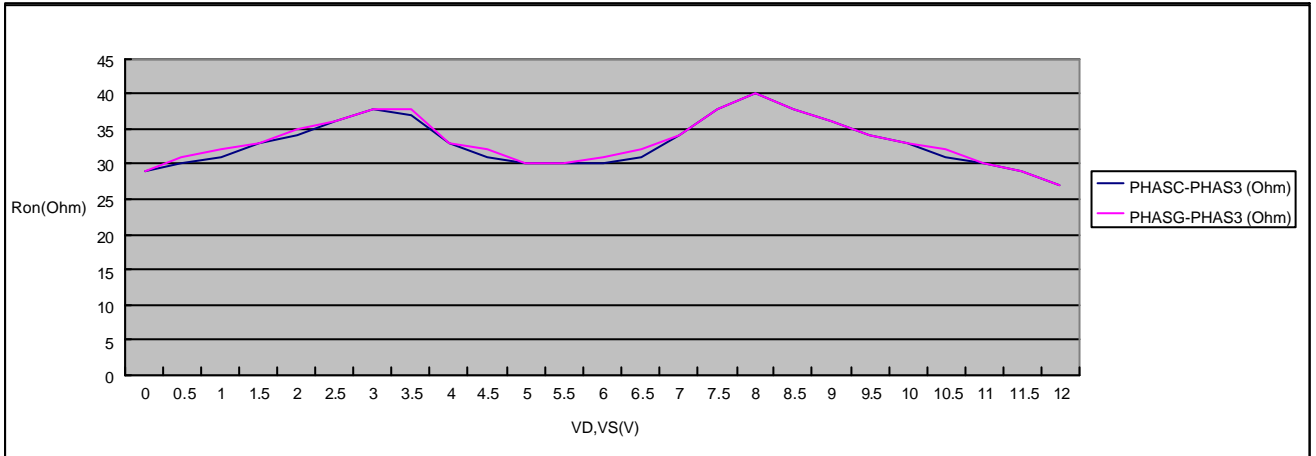


**■ Typical Performance Characteristic**


**Typical Performance Characteristic**
**3.  $R_{ON}$  Test**
 $R_{ON}$  Test Circuit


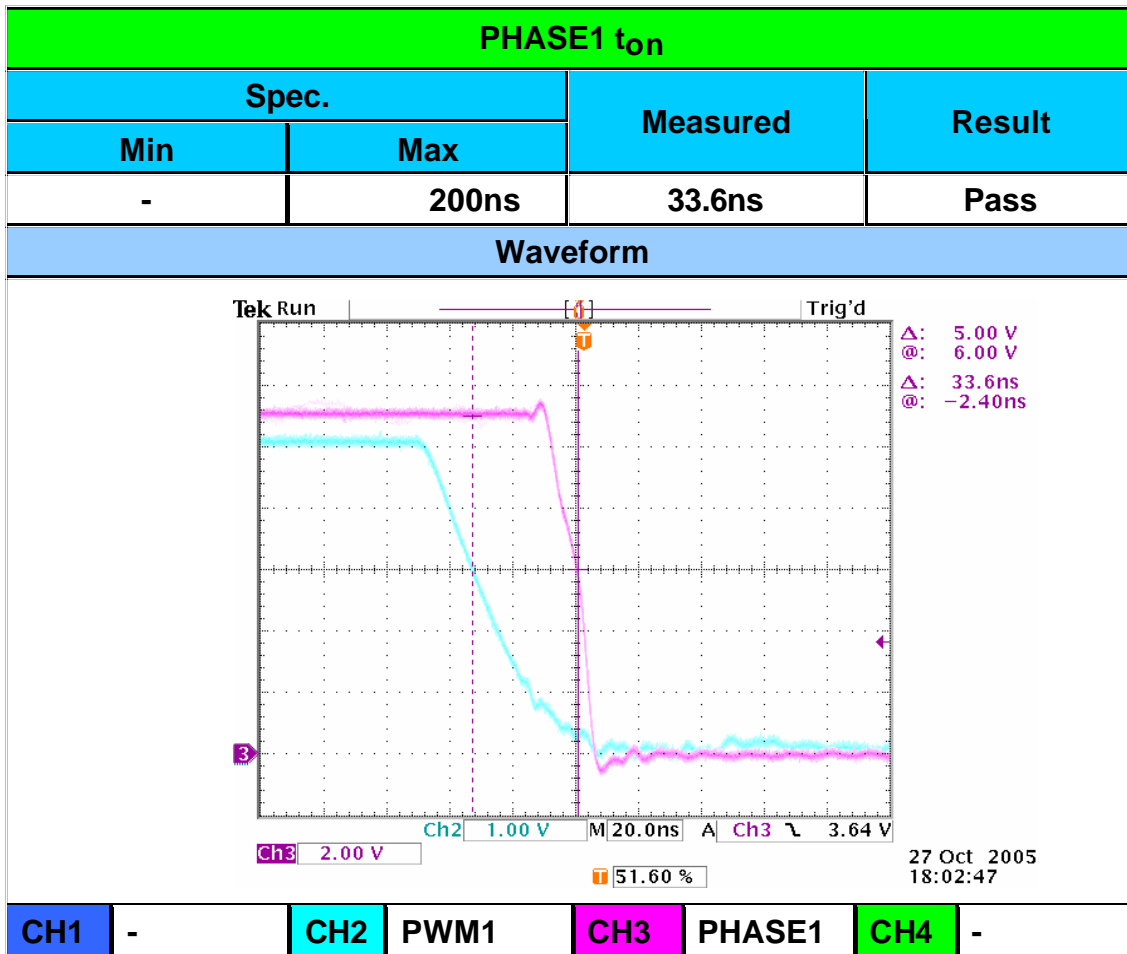


■ Typical Performance Characteristic

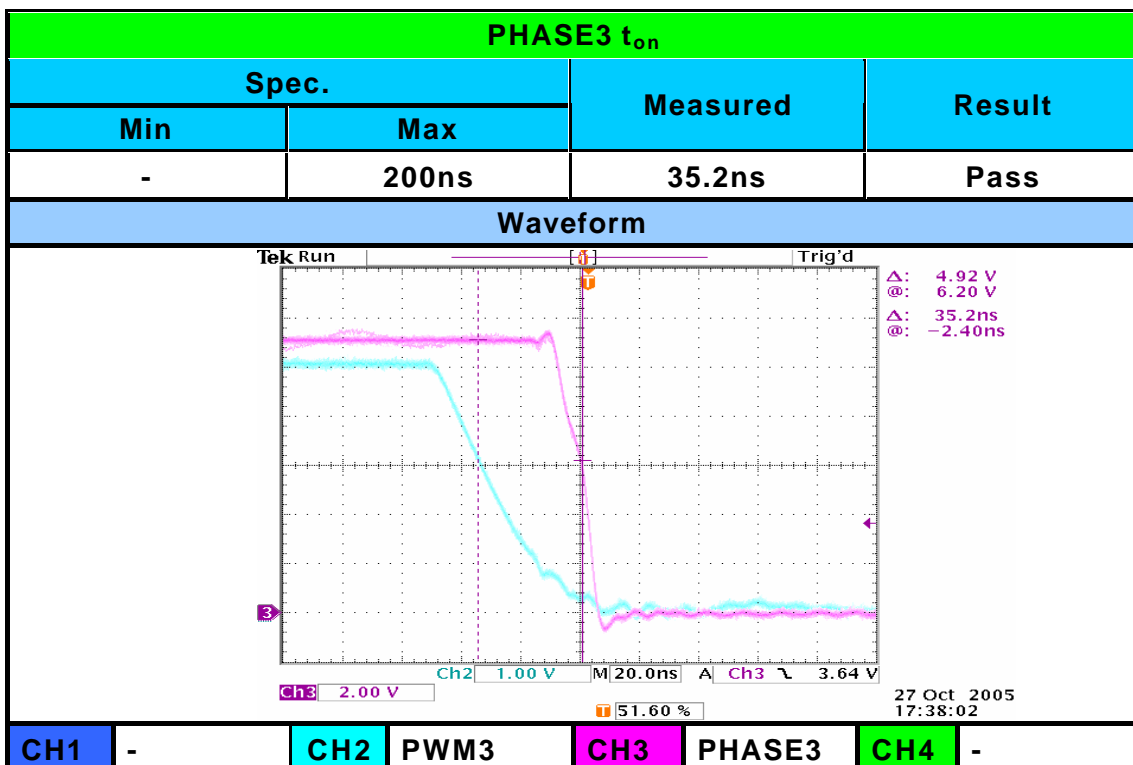
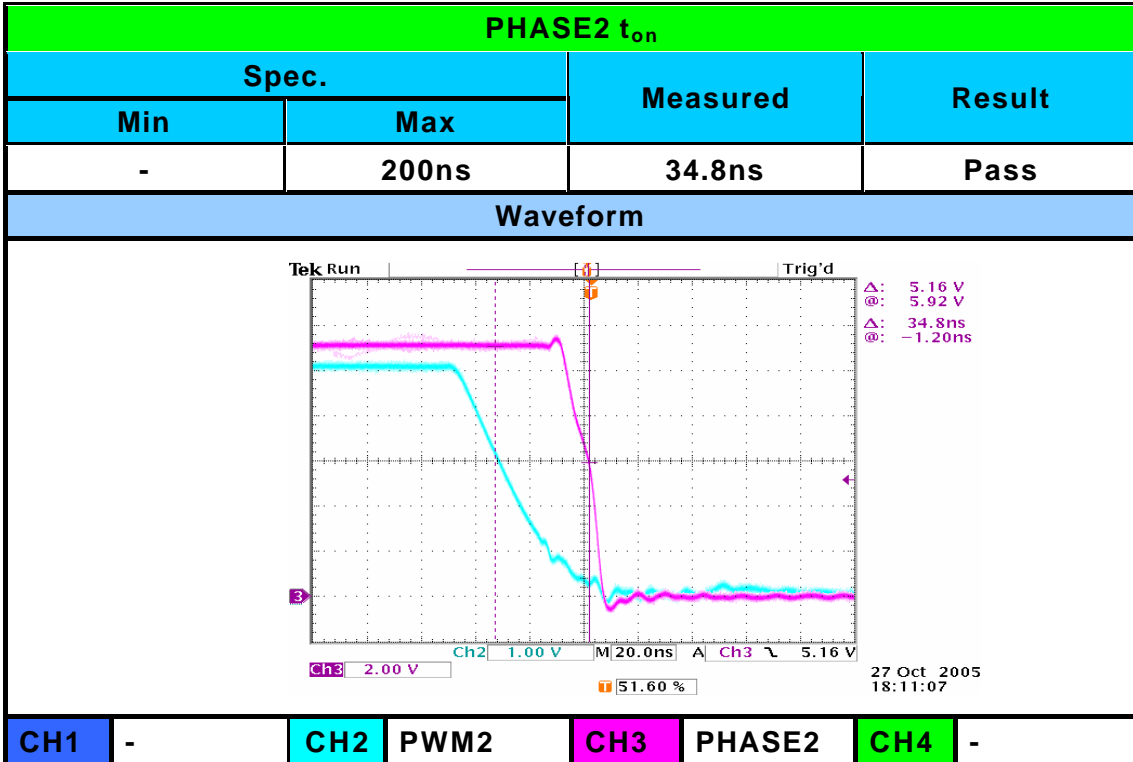


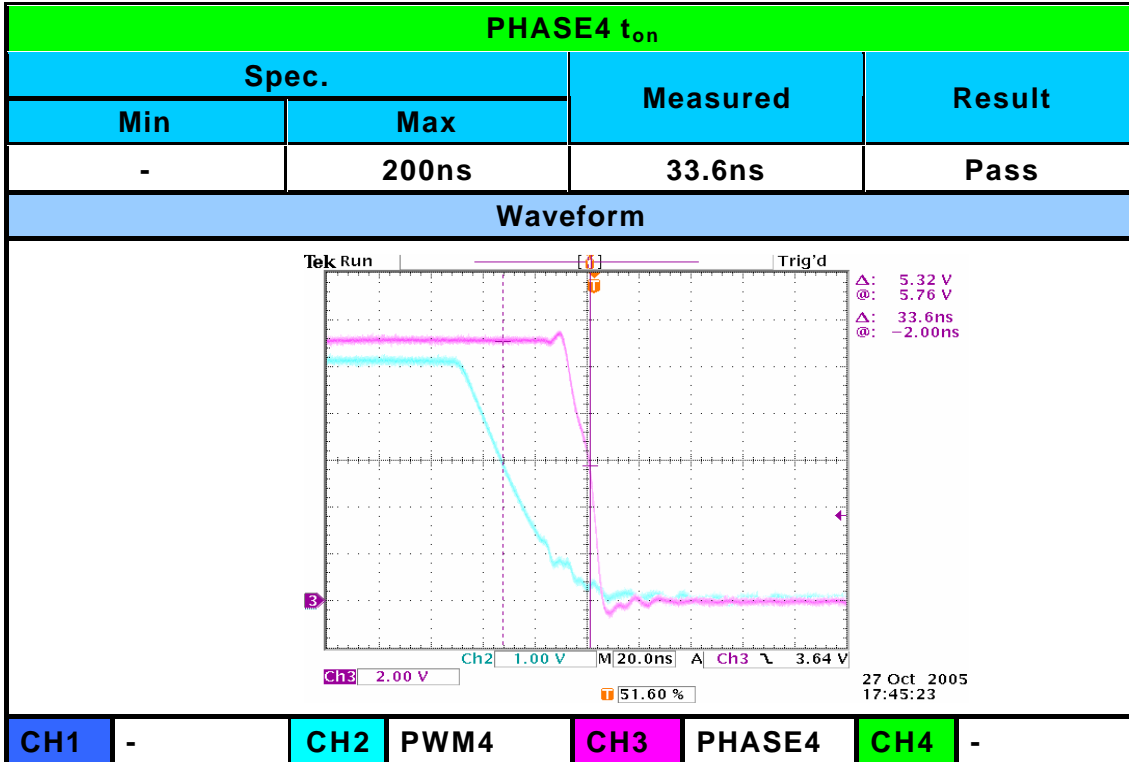
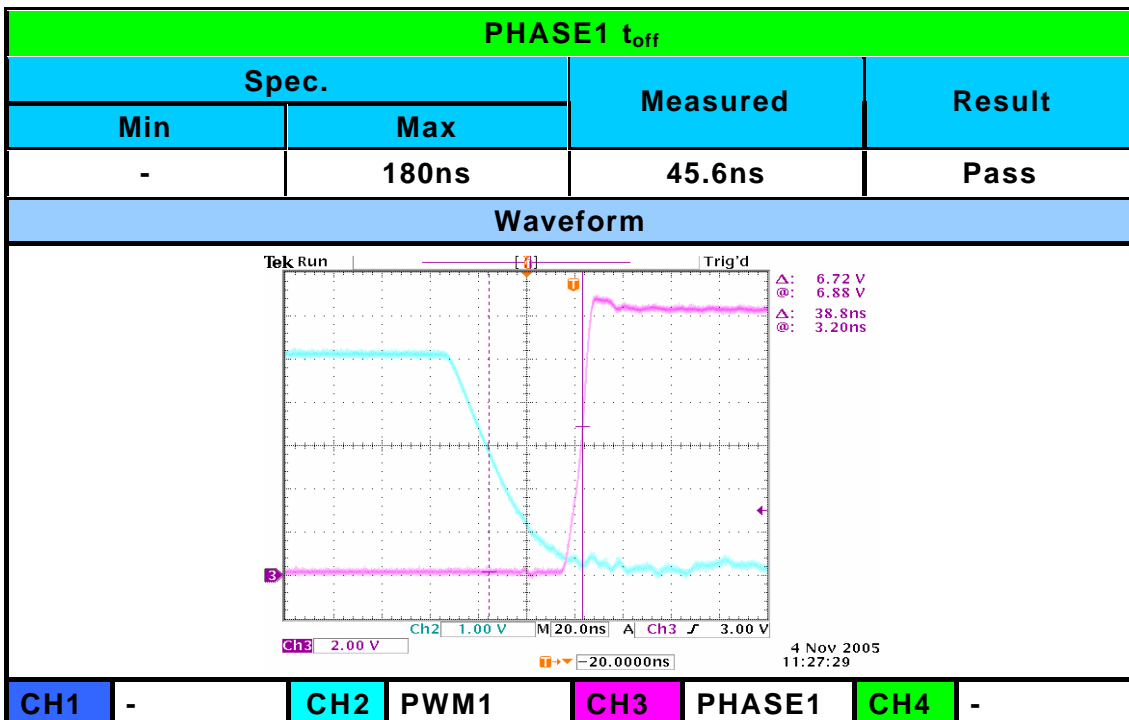
**Typical Performance Characteristic**

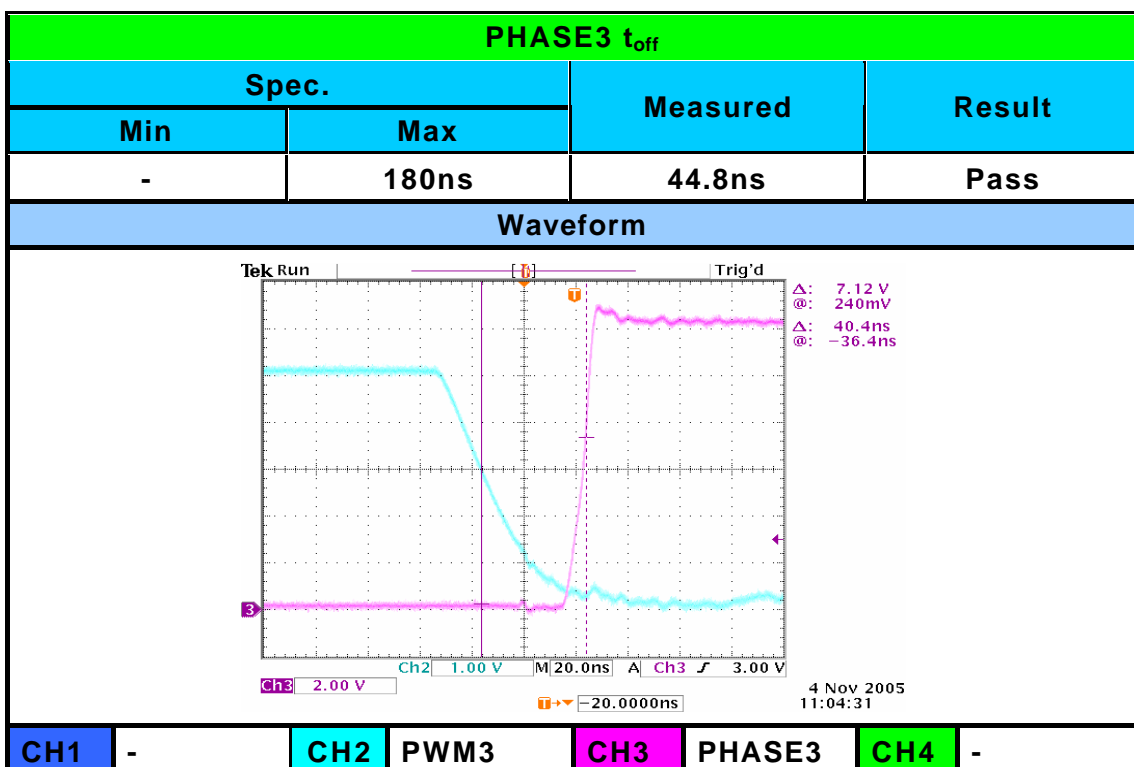
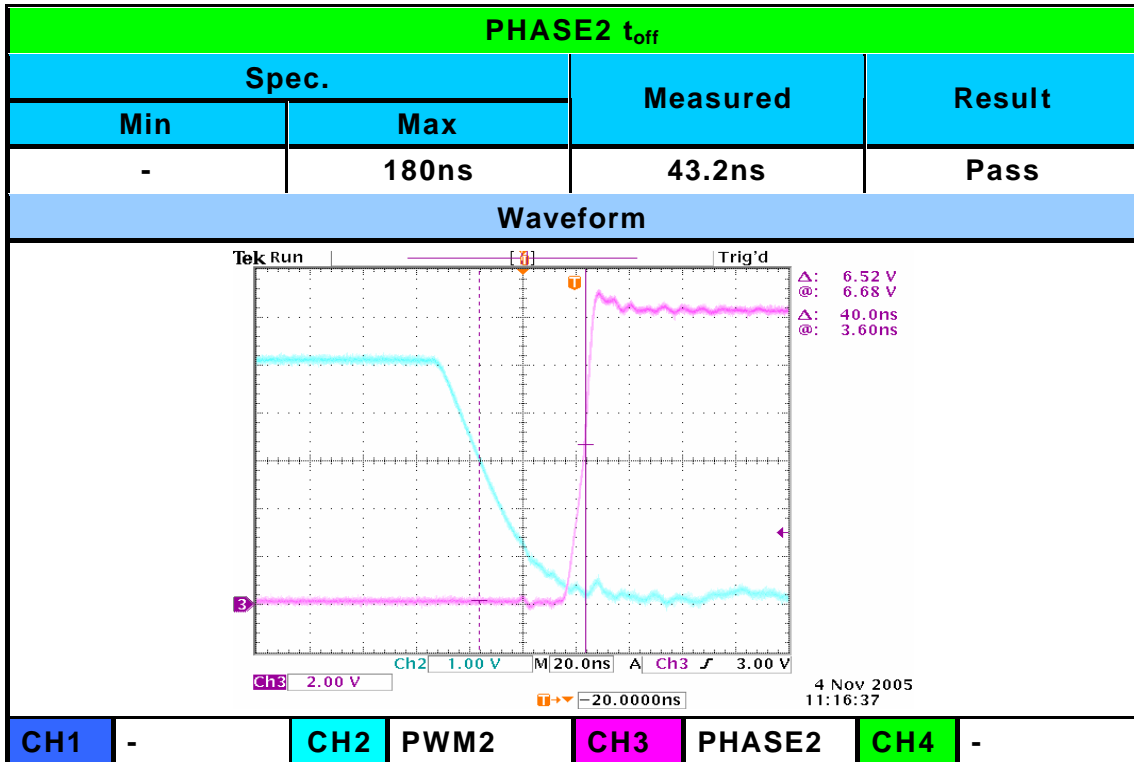
 4.  $t_{on} / t_{off}$  Test

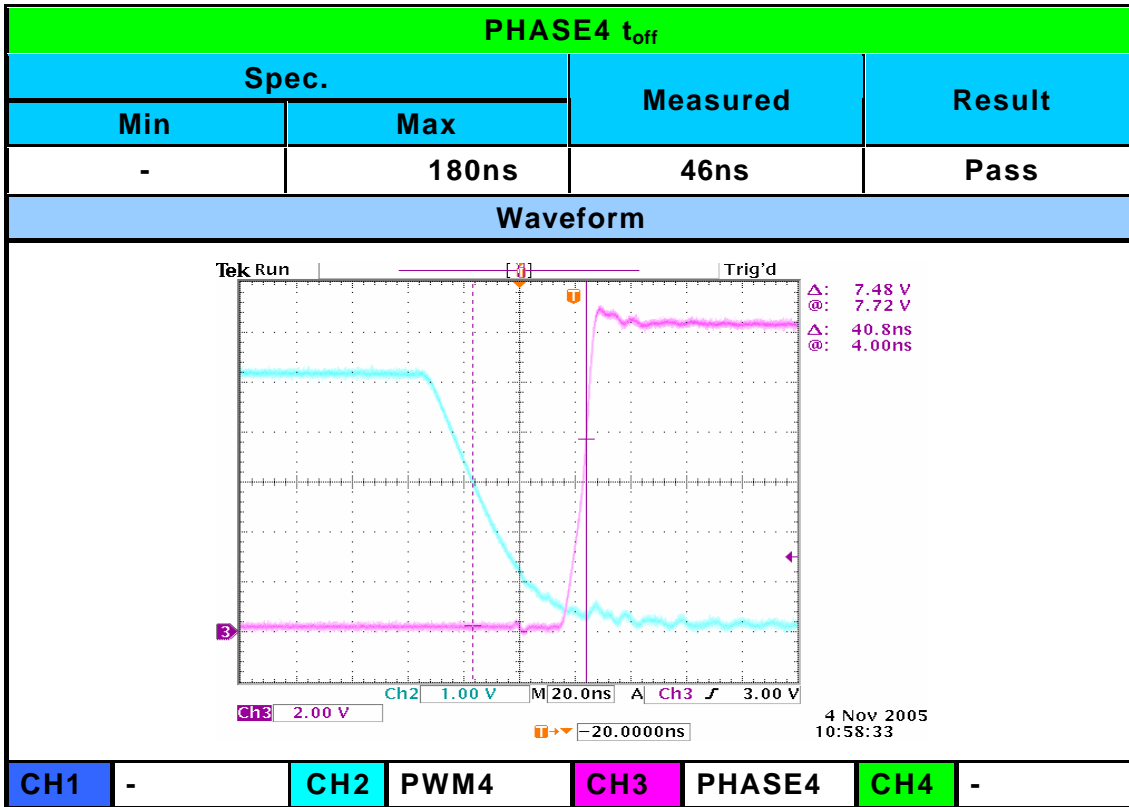
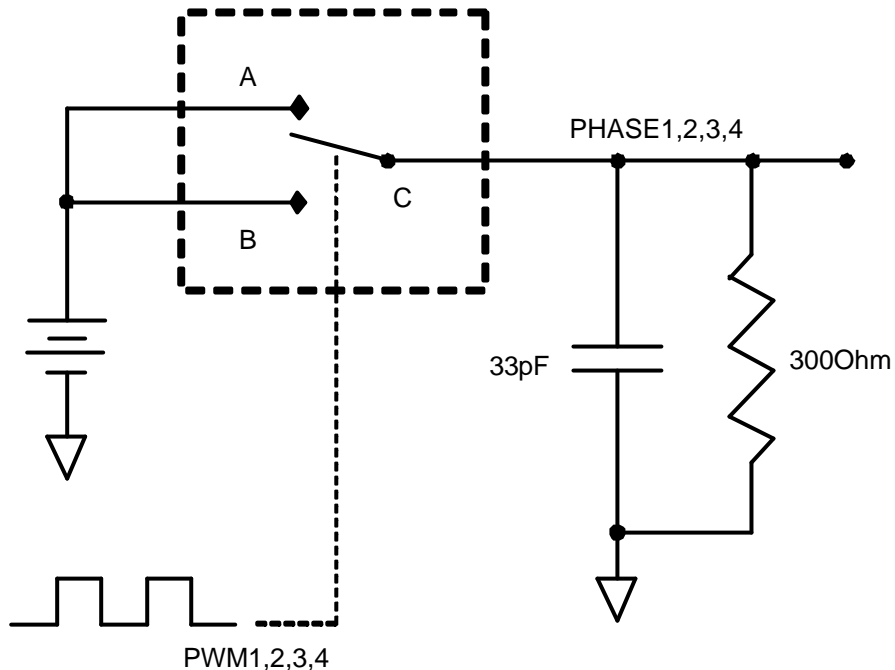
 4-1  $t_{on}$  Test


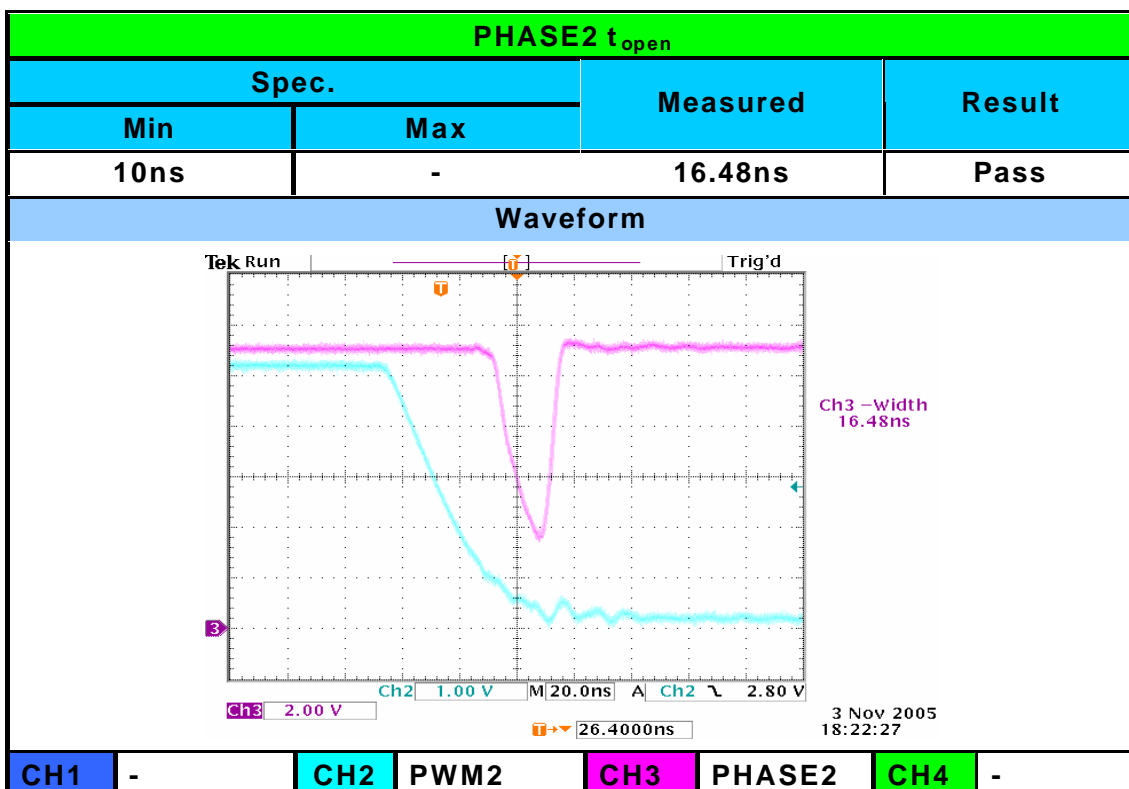
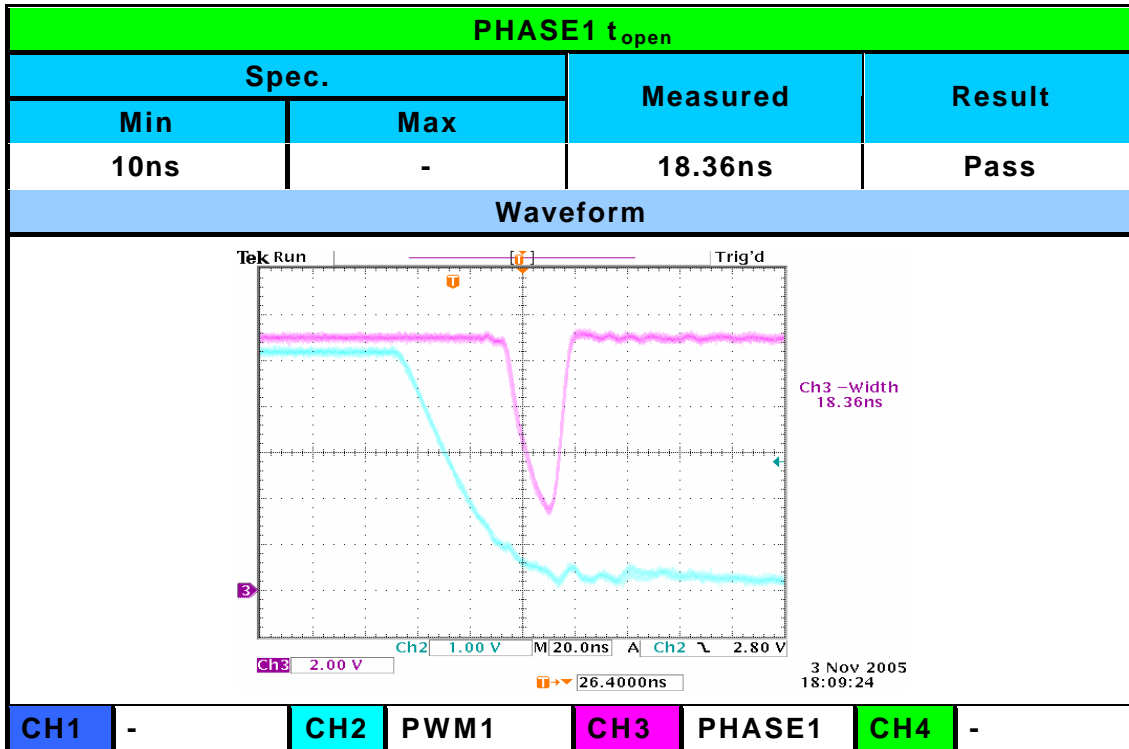


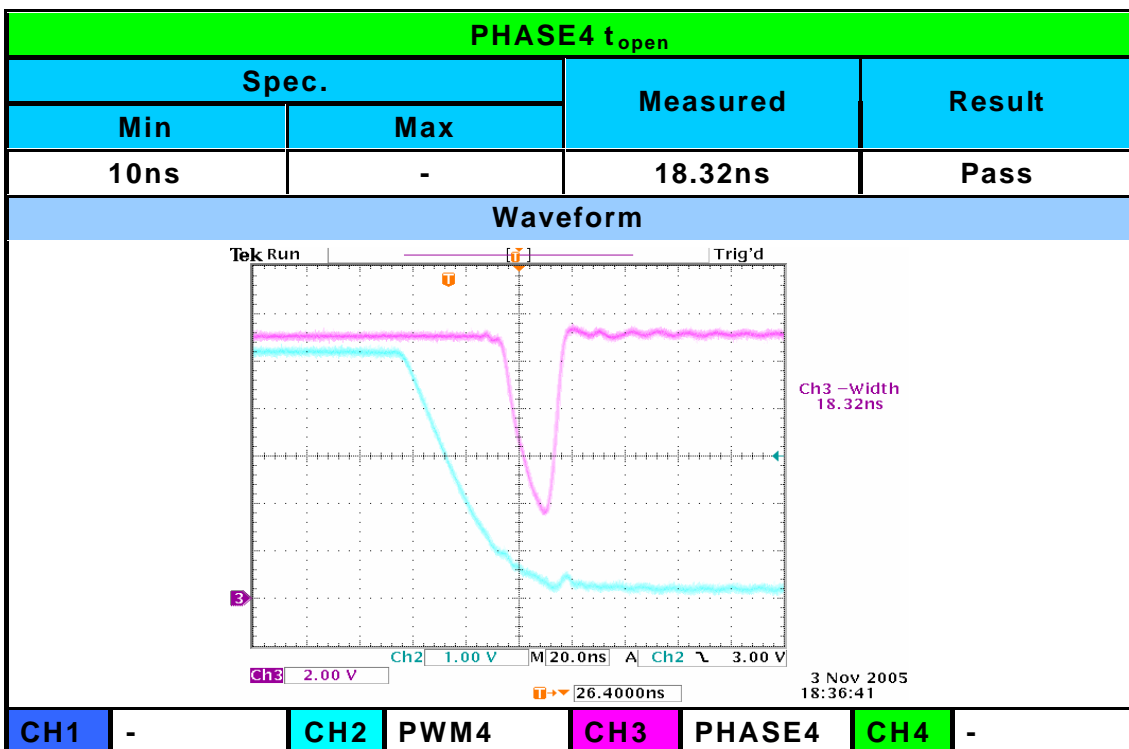
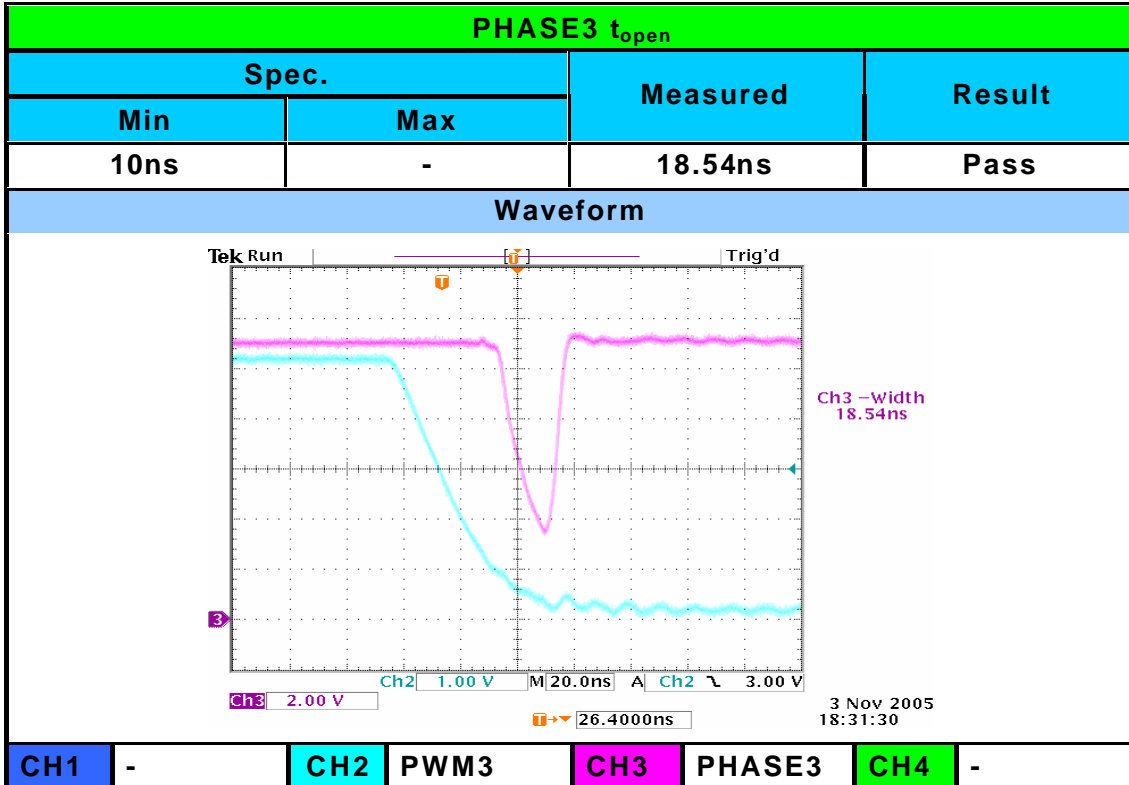
**Typical Performance Characteristic**


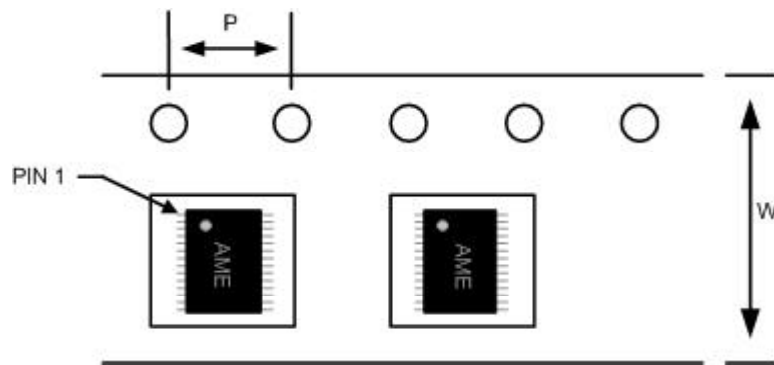
**Typical Performance Characteristic**

 4-2  $t_{off}$  Test


**Typical Performance Characteristic**


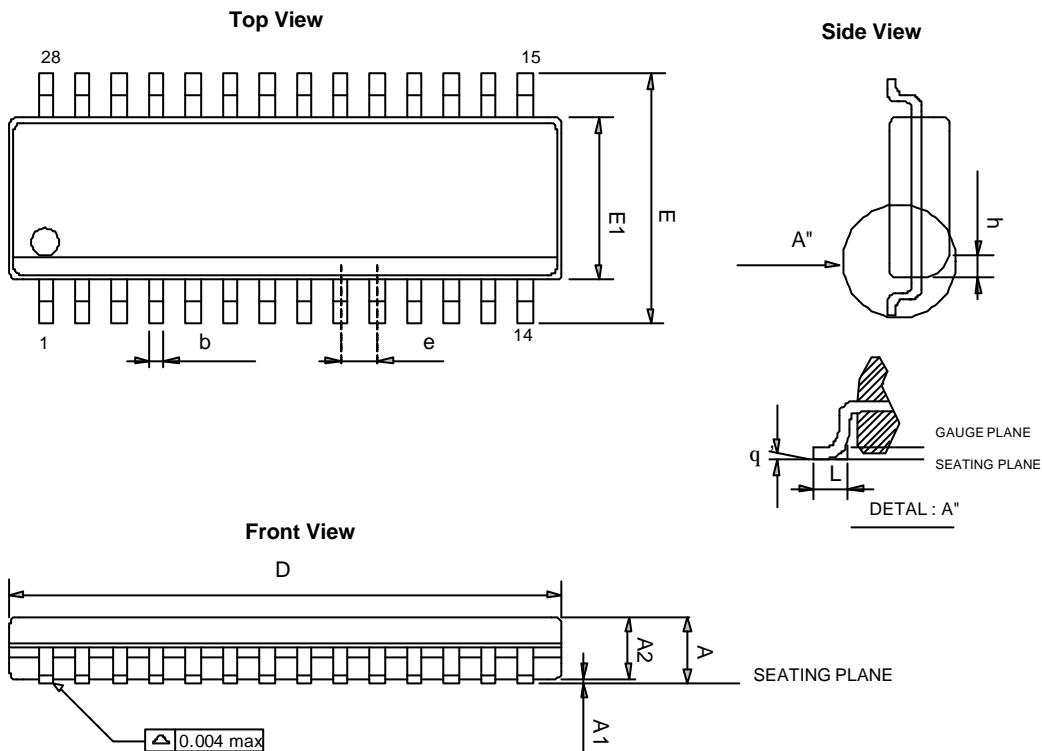
**Typical Performance Characteristic**

**5. Break-Before-Make Delay,  $t_{open}$  Test**
 $t_{open}$  Test Circuit


**Typical Performance Characteristic**


**Typical Performance Characteristic**


**■ Tape and Reel Dimension**
**SSOP-28**

**Carrier Tape, Number of Components Per Reel and Reel Size**

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SSOP-28	16.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm

**■ Package Dimension**
**SSOP-28**


SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	-	1.50	-	0.059
b	0.20	0.30	0.008	0.012
D	9.80	10.00	0.386	0.394
E1	3.81	4.00	0.150	0.157
e	0.635BASIC		0.025BASIC	
E	5.80	6.20	0.228	0.244
h	0.380BASIC		0.015BASIC	
L	0.41	1.27	0.016	0.500
q	0°	8°	0°	8°





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