

AS6C62256

32K X 8 BIT LOW POWER CMOS SRAM

FEATURES

■ Access time: 55ns

■ Low power consumption:

Operation current:

15mA (TYP.), Vcc = 3.0V

Standby current:

 $1\mu A$ (TYP.), Vcc = 3.0V

■ Wide range power supply : 2.7 ~ 5.5V

■ Fully Compatible with all Competitors 5V product

■ Fully Compatible with all Competitors 3.3V product

■ Fully static operation

■ Tri-state output

■ Data retention voltage : 2.0V (MIN.)

■ All products ROHS Compliant

■ Package : 28-pin 600 mil PDIP

28-pin 330 mil SOP

28-pin 8mm x 13.4mm sTSOP

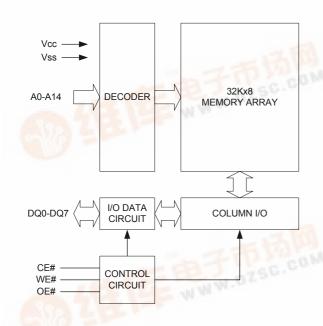
GENERAL DESCRIPTION

The AS6C62256 is a 262,144-bit low power CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C62256 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C62256 operates with wide range power supply 2.7 ~ 5.5V

FUNCTIONAL BLOCK DIAGRAM



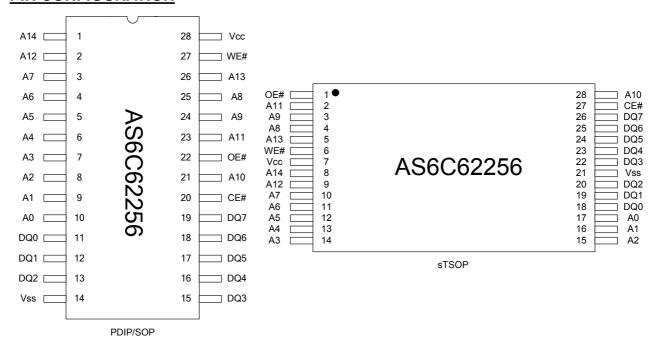
PIN DESCRIPTION

ddress Inputs ata Inputs/Outputs hip Enable Input
nip Enable Input
'
rite Enable Input
utput Enable Input
ower Supply
round





PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to Vss	VTERM	-0.5 to 7.0	V
		0 to 70(C grade)	°C
Operating Temperature	TA		
		-40 to 85(I grade)	°C
Storage Temperature	Тѕтс	-65 to 150	
Power Dissipation	Po	1	W
DC Output Current	Іоит	50	mA
Soldering Temperature (under 10 sec)	Tsolder	260	°C

^{*}Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	Н	X	Х	High-Z	ISB,ISB1
Output Disable	L	Н	Н	High-Z	Icc,Icc1
Read	L	L	Н	Dout	Icc,Icc1
Write	L	Х	L	Din	Icc,Icc1

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDI	TION		MIN.	TYP. *5	MAX.	UNIT
Supply Voltage	Vcc				2.7	3.3	5.5	V
Input High Voltage	V _{IH} *1				0.7*Vcc	-	Vcc+0.5	V
Input Low Voltage	VIL*2				- 0.5	-	0.6	V
Input Leakage Current	ILI	$V_{CC} \ge V_{IN} \ge V_{SS}$			- 1	-	1	μA
Output Leakage Current	ILO	$V_{CC} \ge V_{OUT} \ge V_{SS}$, Output Disabled	Vcc \geq Vouт \geq Vss, Output Disabled			-	1	μA
Output High Voltage	Vон	Iон = -1mA			2.4	3.0	-	V
Output Low Voltage	Vol	I _{OL} = 2mA			-	-	0.4	V
Average Operating	Icc	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0m	ıΑ	-55	-	15	45	mA
Power supply Current	Icc1	Cycle time = 1µs CE#≦0.2V and I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V		-	3	10	mA	
Standby Dower	IsB	CE# = V _{IH}			-	1	3	mA
Standby Power Supply Current	ISB1	CE# ≧Vcc - 0.2V	-C		-	1	50 ^{*4}	μA
Supply Culterit	1281	OL# ≤ V00 - 0.2V	-1		-	1	80 ^{°4}	μA

Notes: C = Commercial Temperature I = Industrial Temperature

- 1. Vih(max) = Vcc + 3.0V for pulse width less than 10ns.
- 2. V_{IL}(min) = V_{SS} 3.0V for pulse width less than 10ns.
- 3. Over/Undershoot specifications are characterized, not 100% tested.
- 4. 10µA for special request
- 5. Typical values are included for reference only and are not guaranteed or tested.

 Typical valued are measured at Vcc = Vcc(TYP.) and Ta = 25°C

CAPACITANCE (TA = 25° C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	Cin	-	6	pF
Input/Output Capacitance	CI/O	-	8	pF

Note: These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to Vcc - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 50pF + 1TTL$, $I_{OH}/I_{OL} = -1mA/2mA$



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM	AS6C62256-55		UNIT	
		MIN	MAX.		
Read Cycle Time	trc	55	-		ns
Address Access Time	taa	-	55		ns
Chip Enable Access Time	tace	-	55		ns
Output Enable Access Time	toe	-	30		ns
Chip Enable to Output in Low-Z	tcLz*	10	-		ns
Output Enable to Output in Low-Z	tolz*	5	-		ns
Chip Disable to Output in High-Z	tcHz*	-	20		ns
Output Disable to Output in High-Z	tonz*	-	20		ns
Output Hold from Address Change	tон	10	-		ns

(2) WRITE CYCLE

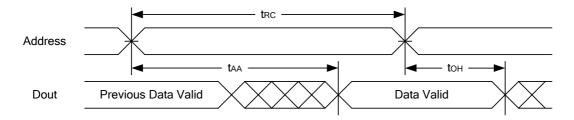
PARAMETER	SYM	SYM		AS6C62256-55			UNIT
				MIN.	MAX.		
Write Cycle Time	twc			55	-		ns
Address Valid to End of Write	taw			50	-		ns
Chip Enable to End of Write	tcw			50	-		ns
Address Set-up Time	tas			0	-		ns
Write Pulse Width	twp			45	-		ns
Write Recovery Time	twR			0	-		ns
Data to Write Time Overlap	tow			25	-		ns
Data Hold from End of Write Time	tон			0	-		ns
Output Active from End of Write	tow*			5	-		ns
Write to Output in High-Z	twnz*			-	20		ns

^{*}These parameters are guaranteed by device characterization, but not production tested.

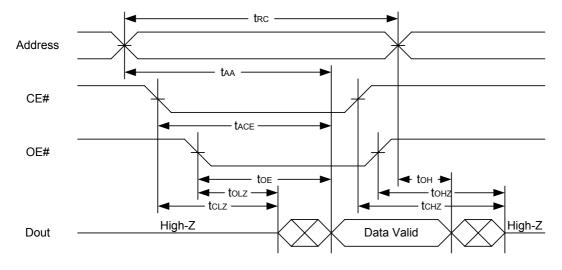


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)

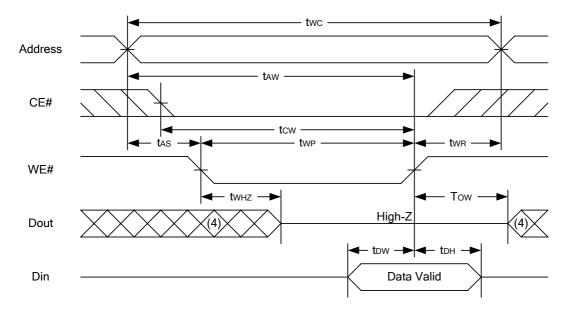


Notes:

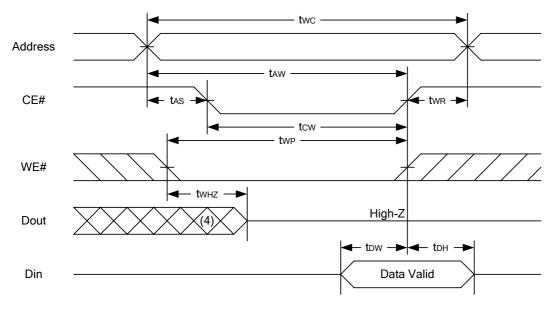
- 1.WE# is high for read cycle.
- 2.Device is continuously selected OE# = low, CE# = low.
- 3.Address must be valid prior to or coincident with CE# = low,; otherwise tAA is the limiting parameter.
- 4.tclz, tolz, tchz and tohz are specified with $C_L = 5pF$. Transition is measured ± 500 mV from steady state.
- 5.At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

- 1.WE#, CE# must be high during all address transitions.
- 2.A write occurs during the overlap of a low CE#, low WE#.
- 3.During a WE# controlled write cycle with OE# low, twp must be greater than twnz + tow to allow the drivers to turn off and data to be placed on the bus.
- $\ \, \text{4.During this period, I/O pins are in the output state, and input signals must not be applied.}$
- 5.If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
- 6.tow and tw_{HZ} are specified with C_{L} = 5pF. Transition is measured $\pm 500 \text{mV}$ from steady state.

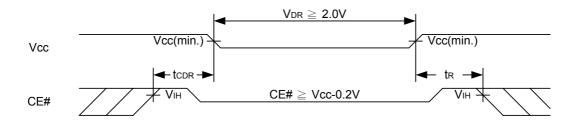


DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V _{DR}	CE# ≧ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current		V _{CC} = 2.0V CE# ≧ V _{CC} - 0.2V	-	0.5	20	μA
Chip Disable to Data Retention Time	tcdr	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

tRC∗ = Read Cycle Time

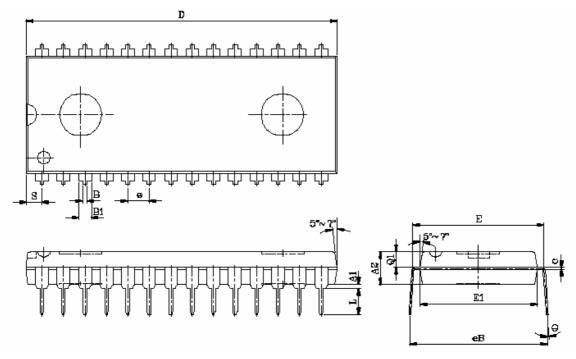
DATA RETENTION WAVEFORM





PACKAGE OUTLINE DIMENSION

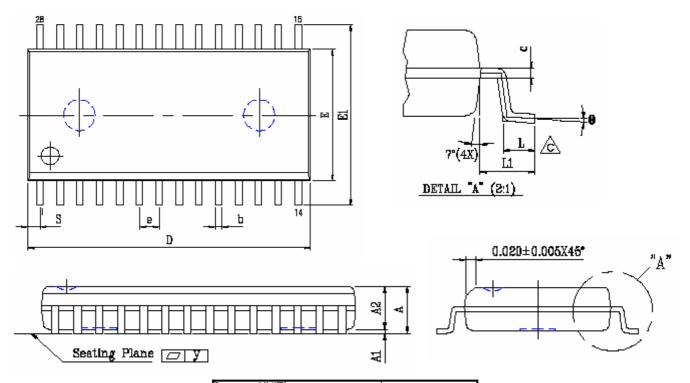
28 pin 600 mil PDIP Package Outline Dimension



SYM. UNIT	INCH.(BASE)	MM(REF)
A1	0.010 (MIN)	0.254 (MIN)
A2	0.150±0.005	3.810±0.127
В	0.020 (MAX)	0.508(MAX)
B1	0.055 (MAX)	1.397(MAX)
С	0.012 (MAX)	0.304 (MAX)
D	1.430 (MAX)	36.322 (MAX)
E	0.6 (TYP)	15.24 (TYP)
E1	0.52 (MAX)	13.208 (MAX)
е	0.100 (TYP)	2.540(TYP)
eB	0.625 (MAX)	15.87 (MAX)
L	0.180(MAX)	4.572(MAX)
S	0.06 (MAX)	1.524 (MAX)
Q1	0.08(MAX)	2.032(MAX)
Θ	15°(MAX)	15°(MAX)



28 pin 330 mil SOP Package Outline Dimension

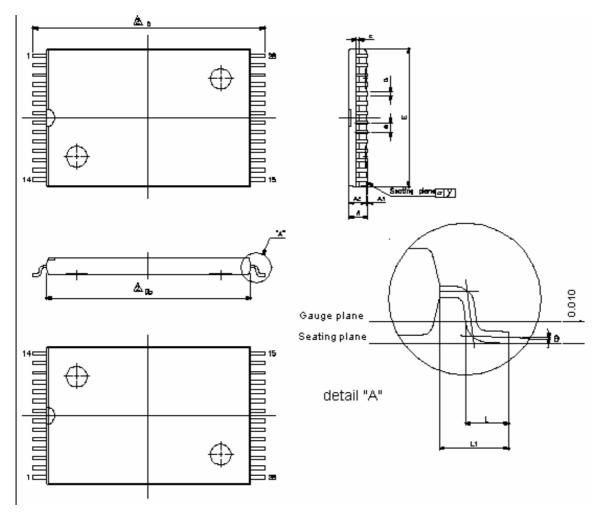


SYM. UNIT	INCH(BASE)	MM(REF)
Α	0.120 (MAX)	3.048 (MAX)
A1	0.002(MIN)	0.05(MIN)
A2	0.098±0.005	2.489±0.127
b	0.016 (TYP)	0.406(TYP)
С	0.010 (TYP)	0.254(TYP)
D	0.728 (MAX)	18.491 (MAX)
Е	0.340 (MAX)	8.636 (MAX)
E1	0.465±0.012	11.811±0.305
е	0.050 (TYP)	1.270(TYP)
L	0.05 (MAX)	1.270 (MAX)
L1	0.067±0.008	1.702 ±0.203
S	0.047 (MAX)	1.194 (MAX)
У	0.003(MAX)	0.076(MAX)
Θ	0°~10°	0°~10°



28 pin 8mm x 13.4mm sTSOP Package Outline Dimension

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SYM. UNIT	INCH(BASE)	MM(REF)
Α	0.047 (MAX)	1.20 (MAX)
A1	0.004±0.002	0.10±0.05
A2	0.039±0.002	1.00±0.05
b	0.006 (TYP)	0.15(TYP)
С	0.010 (TYP)	0.254(TYP)
Db	0.465±0.004	11.80±0.10
Е	0.315±0.004	8.00±0.10
е	0.022 (TYP)	0.55(TYP)
D	0.528±0.008	13.40±0.20
L	0.020±0.004	0.50±0.10
L1	0.0315±0.004	0.80±0.10
у	0.08(MAX)	0.003(MAX)
Θ	0°~5°	0°∼5°

Note: E dimension is not including end flash. The total of both sides' end flash is not above 0.3mm.



ORDERING INFORMATION

Ordering Codes

				Operating	Speed
Alliance	Organization	VCC range	Package	Temp	ns
				Commercial ~	
AS6C62256-55PCN	32k x 8	2.7-5.5V	28pin 600mil PDIP	0° C to 70° C	55
				Commercial ~	
AS6C62256-55SCN	32k x 8	2.7-5.5V	28pin 330mil SOP	0° C to 70° C	55
				Industrial ~	
AS6C62256-55SIN	32k x 8	2.7-5.5V	28pin 330mil SOP	-40°C to 85° C	55
				Commercial ~	
AS6C62256-55STCN	32k x 8	2.7-5.5V	28pin sTSOP (8 x 13.4 mm)	0° C to 70° C	55
				Industrial ~	
AS6C62256-55STIN	32k x 8	2.7-5.5V	28pin sTSOP (8 x 13.4 mm)	-40°C to 85° C	55

Part numbering system

AS6C	62256	- 55	X	X	N
				Temperature Range:	
low	Device		Package Options:	C = Commercial	N = Lead
power	Number		P = 28 pin 600 mil P-DIP	(0°C to +70° C)	Free ROHS
SRAM	62256	Access	S = 28 pin 330 mil SOP	I = Industrial	Compliant
prefix		Time	ST = 28 pin sTSOP (8mm x 13.4 mm)	(-40° to +85° C)	Part

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Rev 1





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