

February 2007



AS6C6264

8K X 8 BIT LOW POWER CMOS SRAM

FEATURES

- Access time :55ns
- Low power consumption:
Operation current :
15mA (TYP.), V_{CC} = 3.0V
Standby current :
1μA (TYP.), V_{CC} = 3.0V
- Wide range power supply : 2.7 ~ 5.5V
- Fully Compatible with all Competitors 5V product
- Fully Compatible with all Competitors 3.3V product
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **All products ROHS Compliant**
- Package : 28-pin 600 mil PDIP
28-pin 330 mil SOP
28-pin 8mm x 13.4mm sTSOP

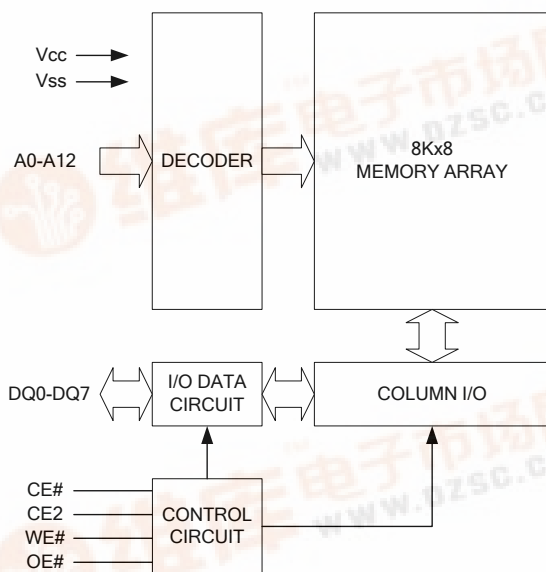
GENERAL DESCRIPTION

The AS6C6264 is a 65,536-bit low power CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS6C6264 is well designed for low power application, and particularly well suited for battery back-up nonvolatile memory application.

The AS6C6264 operates with wide range power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

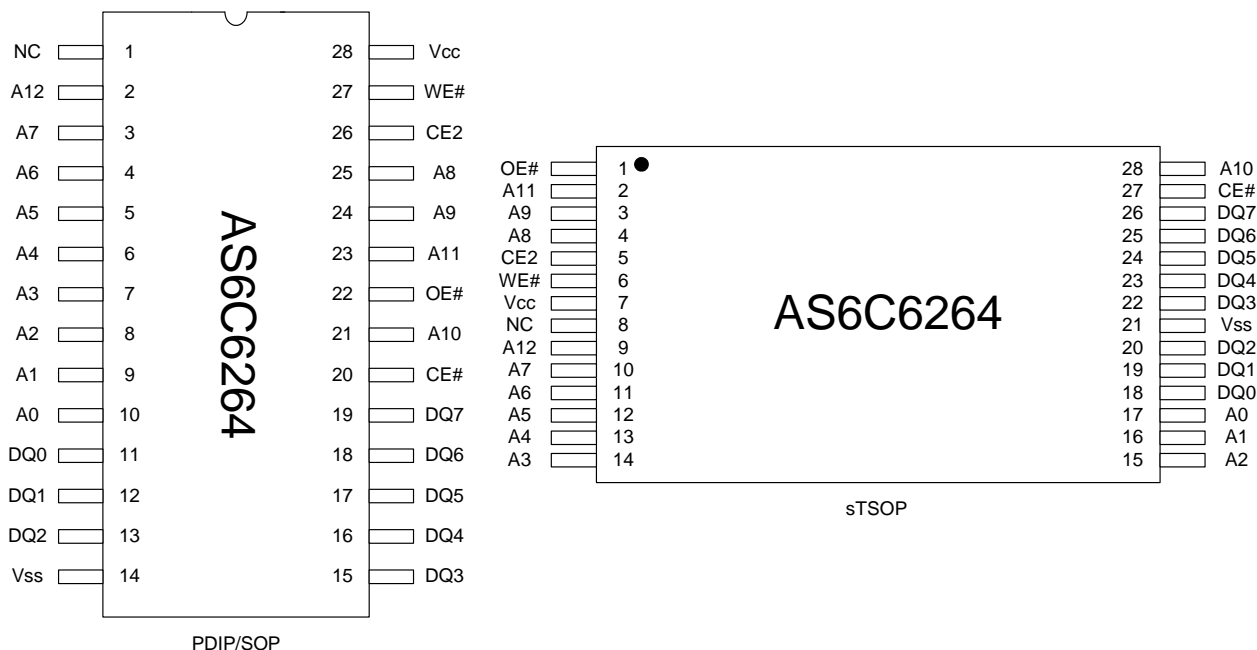
| SYMBOL | DESCRIPTION |
|-----------|---------------------|
| A0 - A12 | Address Inputs |
| DQ0 - DQ7 | Data Inputs/Outputs |
| CE#, CE2 | Chip Enable Inputs |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| Vcc | Power Supply |
| Vss | Ground |
| NC | No Connection |





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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--------------------------------------|---------------------|--------------------|------|
| Terminal Voltage with Respect to Vss | V _{TERM} | -0.5 to 7.0 | V |
| Operating Temperature | T _A | 0 to 70(C grade) | °C |
| | | -40 to 85(I grade) | |
| Storage Temperature | T _{STG} | -65 to 150 | °C |
| Power Dissipation | P _D | 1 | W |
| DC Output Current | I _{OUT} | 50 | mA |
| Soldering Temperature (under 10 sec) | T _{SOLDER} | 260 | °C |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | CE2 | OE# | WE# | I/O OPERATION | SUPPLY CURRENT |
|----------------|-----|-----|-----|-----|------------------|------------------------------------|
| Standby | H | X | X | X | High-Z | I _{SB} , I _{SB1} |
| | X | L | X | X | High-Z | I _{SB} , I _{SB1} |
| Output Disable | L | H | H | H | High-Z | I _{CC} , I _{CC1} |
| Read | L | H | L | H | D _{OUT} | I _{CC} , I _{CC1} |
| Write | L | H | X | L | D _{IN} | I _{CC} , I _{CC1} |

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



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DC ELECTRICAL CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. ⁵ | MAX. | UNIT |
|--|------------------------------|--|---------------------|-------------------|----------------------|-----------------|
| Supply Voltage | V _{CC} | | 2.7 | 3.0 | 5.5 | V |
| Input High Voltage | V _{IH} ¹ | | 0.7*V _{CC} | - | V _{CC} +0.3 | V |
| Input Low Voltage | V _{IL} ² | | - 0.5 | - | 0.6 | V |
| Input Leakage Current | I _{LI} | V _{CC} ≥ V _{IN} ≥ V _{SS} | - 1 | - | 1 | μA |
| Output Leakage Current | I _{LO} | V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled | - 1 | - | 1 | μA |
| Output High Voltage | V _{OH} | I _{OH} = -1mA | 2.4 | 3.0 | - | V |
| Output Low Voltage | V _{OL} | I _{OL} = 2mA | - | - | 0.4 | V |
| Average Operating Power supply Current | I _{CC} | Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA | - 55 | 15 | 45 | mA |
| | I _{CC1} | Cycle time = 1μs CE# ≤ 0.2V and CE2 ≥ V _{CC} -0.2V, I _{I/O} = 0mA other pins at 0.2V or V _{CC} -0.2V | - | 3 | 10 | mA |
| Standby Power Supply Current | I _{SB1} | CE# ≥ V _{CC} -0.2V | -C | 1 | 50 ⁴ | μA |
| | | or CE2 ≤ 0.2V | -I | - | 1 | 80 ⁴ |

Notes: C = Commercial Temperature I = Industrial temperature

1. V_{IH}(max) = V_{CC} + 30V for pulse width less than 10ns

2. V_{IL}(min) = V_{CC} - 3.0V for pulse width less than 10ns.

3. Over/Undershoot specifications are characterized, not 10% tested.

4. 10μA for special request

5. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|------------------|------|-----|------|
| Input Capacitance | C _{IN} | - | 6 | pF |
| Input/Output Capacitance | C _{I/O} | - | 8 | pF |

Note :These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|---|
| Input Pulse Levels | 0.2V to V _{CC} - 0.2V |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | 1.5V |
| Output Load | C _L = 50pF + 1TTL, I _{OH} /I _{OL} = -1mA/2mA |



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

| PARAMETER | SYM. | AS6C6264-55 | | UNIT |
|------------------------------------|--------------------|-------------|------|------|
| | | MIN. | MAX. | |
| Read Cycle Time | t _{RC} | 55 | - | ns |
| Address Access Time | t _{AA} | - | 55 | ns |
| Chip Enable Access Time | t _{ACE} | - | 55 | ns |
| Output Enable Access Time | t _{OE} | | 30 | ns |
| Chip Enable to Output in Low-Z | t _{CLZ} * | 10 | - | ns |
| Output Enable to Output in Low-Z | t _{OLZ} * | 5 | - | ns |
| Chip Disable to Output in High-Z | t _{CHZ} * | - | 20 | ns |
| Output Disable to Output in High-Z | t _{OHZ} * | | 20 | ns |
| Output Hold from Address Change | t _{OH} | 10 | - | ns |

(2) WRITE CYCLE

| PARAMETER | SYM. | AS6C6264-55 | | UNIT |
|----------------------------------|--------------------|-------------|------|------|
| | | MIN. | MAX. | |
| Write Cycle Time | t _{WC} | 55 | - | ns |
| Address Valid to End of Write | t _{AW} | 50 | - | ns |
| Chip Enable to End of Write | t _{CW} | 50 | - | ns |
| Address Set-up Time | t _{AS} | 0 | - | ns |
| Write Pulse Width | t _{WP} | 45 | - | ns |
| Write Recovery Time | t _{WR} | 0 | - | ns |
| Data to Write Time Overlap | t _{DW} | 25 | - | ns |
| Data Hold from End of Write Time | t _{DH} | 0 | - | ns |
| Output Active from End of Write | t _{OW} * | 5 | - | ns |
| Write to Output in High-Z | t _{WHZ} * | - | 20 | ns |

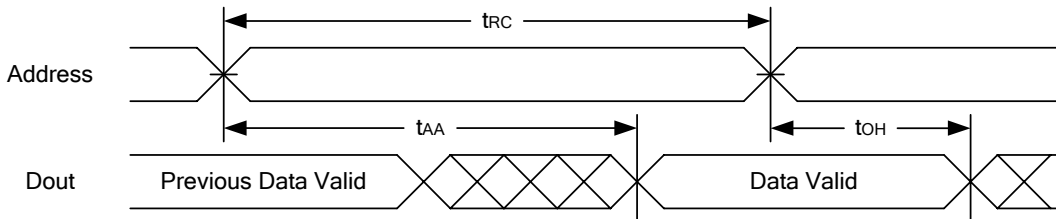
*These parameters are guaranteed by device characterization, but not production tested.



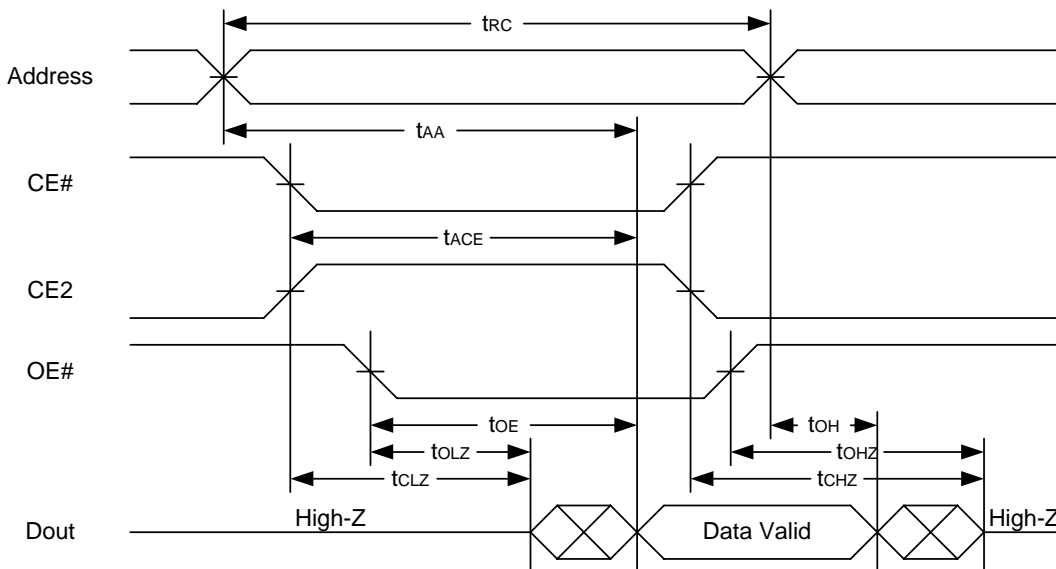
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TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



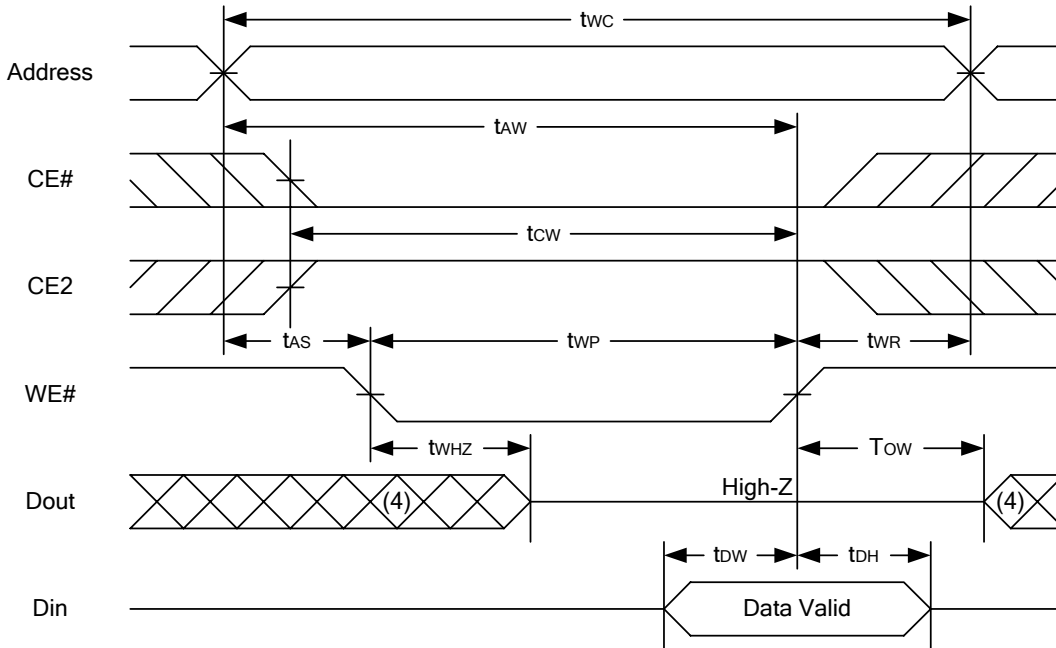
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

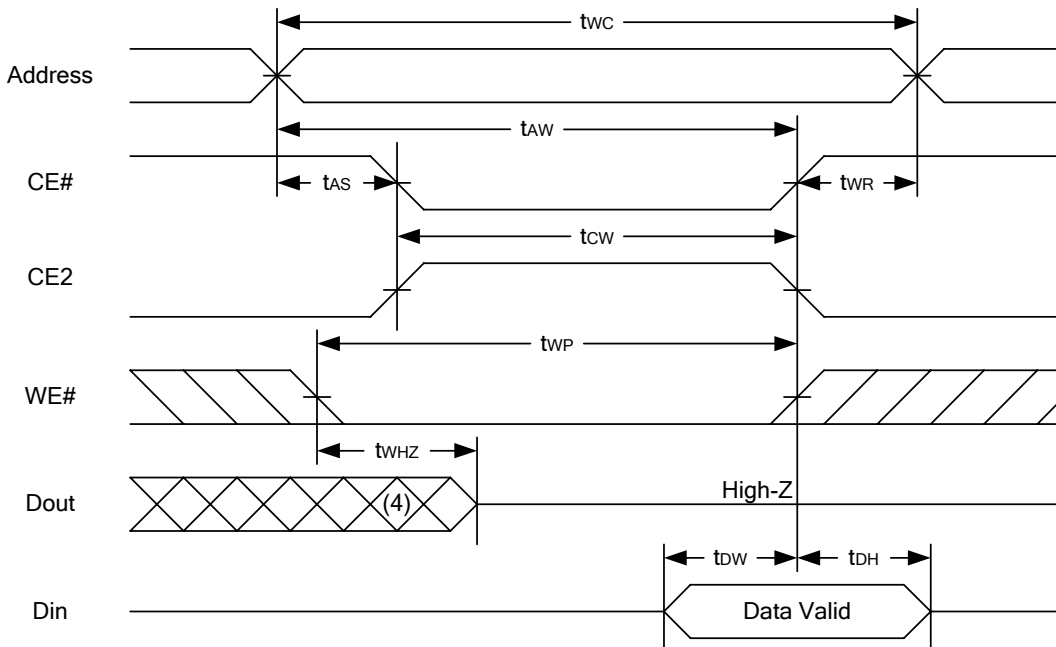


8K X 8 BIT LOW POWER CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, twp must be greater than twhZ + tOW to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. tOW and twhZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.



8K X 8 BIT LOW POWER CMOS SRAM

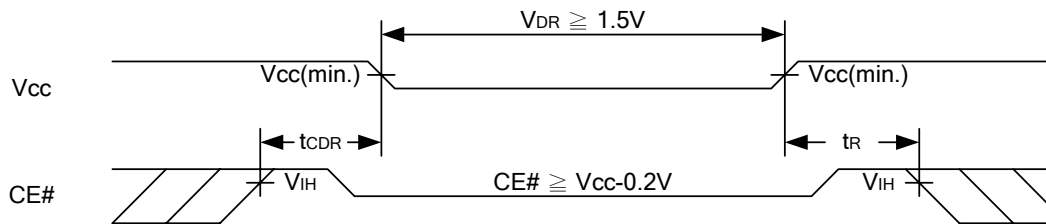
DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|------------------|---|-------------------|------|------|---------|
| V _{CC} for Data Retention | V _{DR} | CE# \geq V _{CC} - 0.2V or CE2 \leq 0.2V | 1.5 | - | 5.5 | V |
| Data Retention Current | I _{DR} | V _{CC} = 1.5V CE# \geq V _{CC} - 0.2V or CE2 \leq 0.2V | - | 0.5 | 10 | μ A |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns |
| Recovery Time | t _R | | t _{RC} * | - | - | ns |

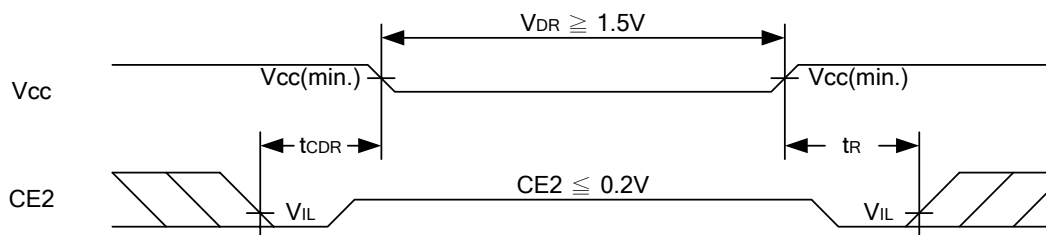
t_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)



Low V_{CC} Data Retention Waveform (2) (CE2 controlled)

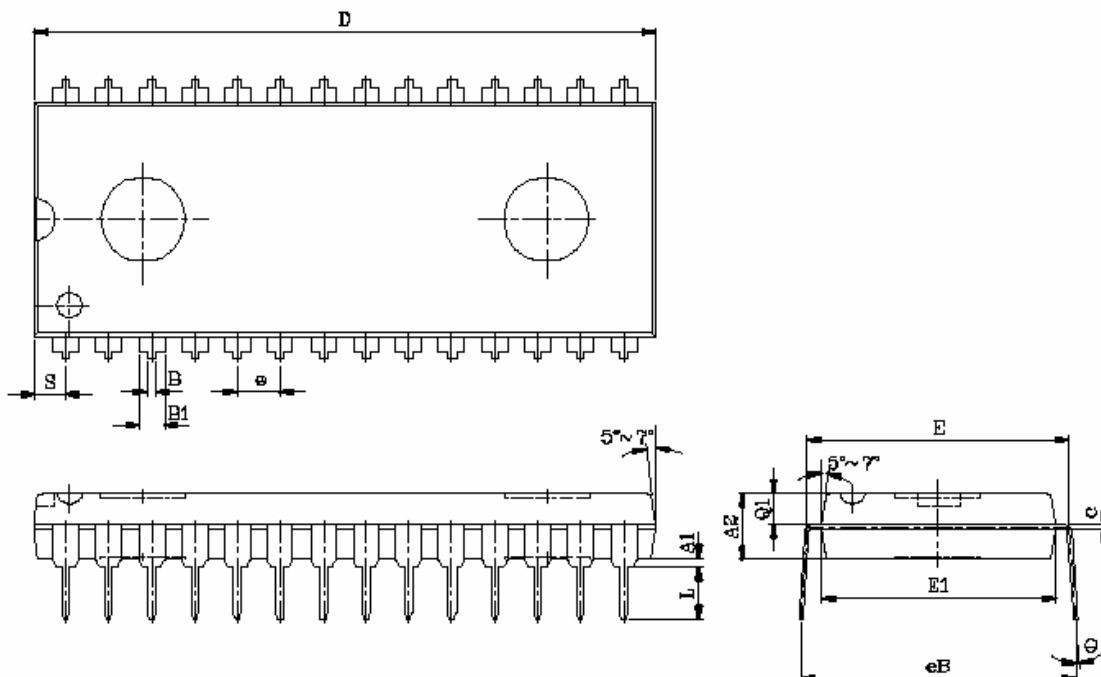




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PACKAGE OUTLINE DIMENSION

28 pin 600 mil PDIP Package Outline Dimension

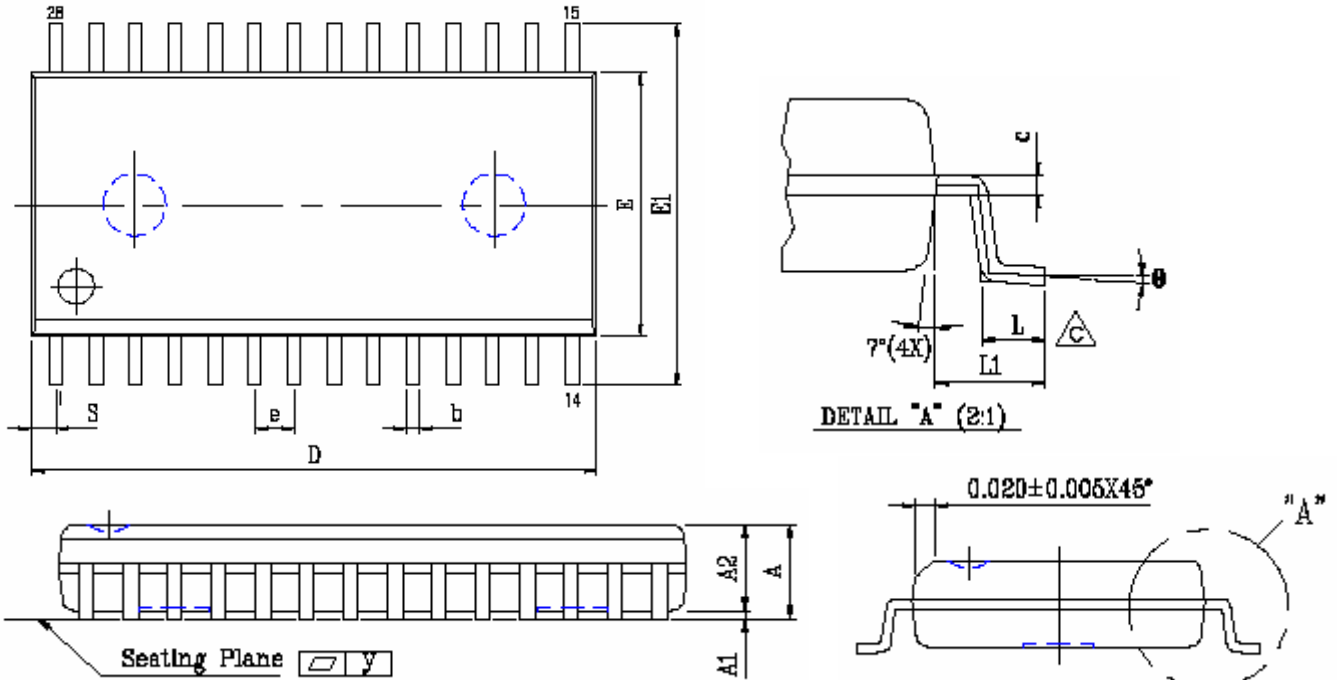


| SYM. | UNIT | INCH.(BASE) | MM(REF) |
|------|------|-------------|--------------|
| A1 | | 0.010 (MIN) | 0.254 (MIN) |
| A2 | | 0.150±0.005 | 3.810±0.127 |
| B | | 0.020 (MAX) | 0.508(MAX) |
| B1 | | 0.055 (MAX) | 1.397(MAX) |
| c | | 0.012 (MAX) | 0.304 (MAX) |
| D | | 1.430 (MAX) | 36.322 (MAX) |
| E | | 0.6 (TYP) | 15.24 (TYP) |
| E1 | | 0.52 (MAX) | 13.208 (MAX) |
| e | | 0.100 (TYP) | 2.540(TYP) |
| eB | | 0.625 (MAX) | 15.87 (MAX) |
| L | | 0.180(MAX) | 4.572(MAX) |
| S | | 0.06 (MAX) | 1.524 (MAX) |
| Q1 | | 0.08(MAX) | 2.032(MAX) |
| Θ | | 15°(MAX) | 15°(MAX) |



8K X 8 BIT LOW POWER CMOS SRAM

28 pin 330 mil SOP Package Outline Dimension

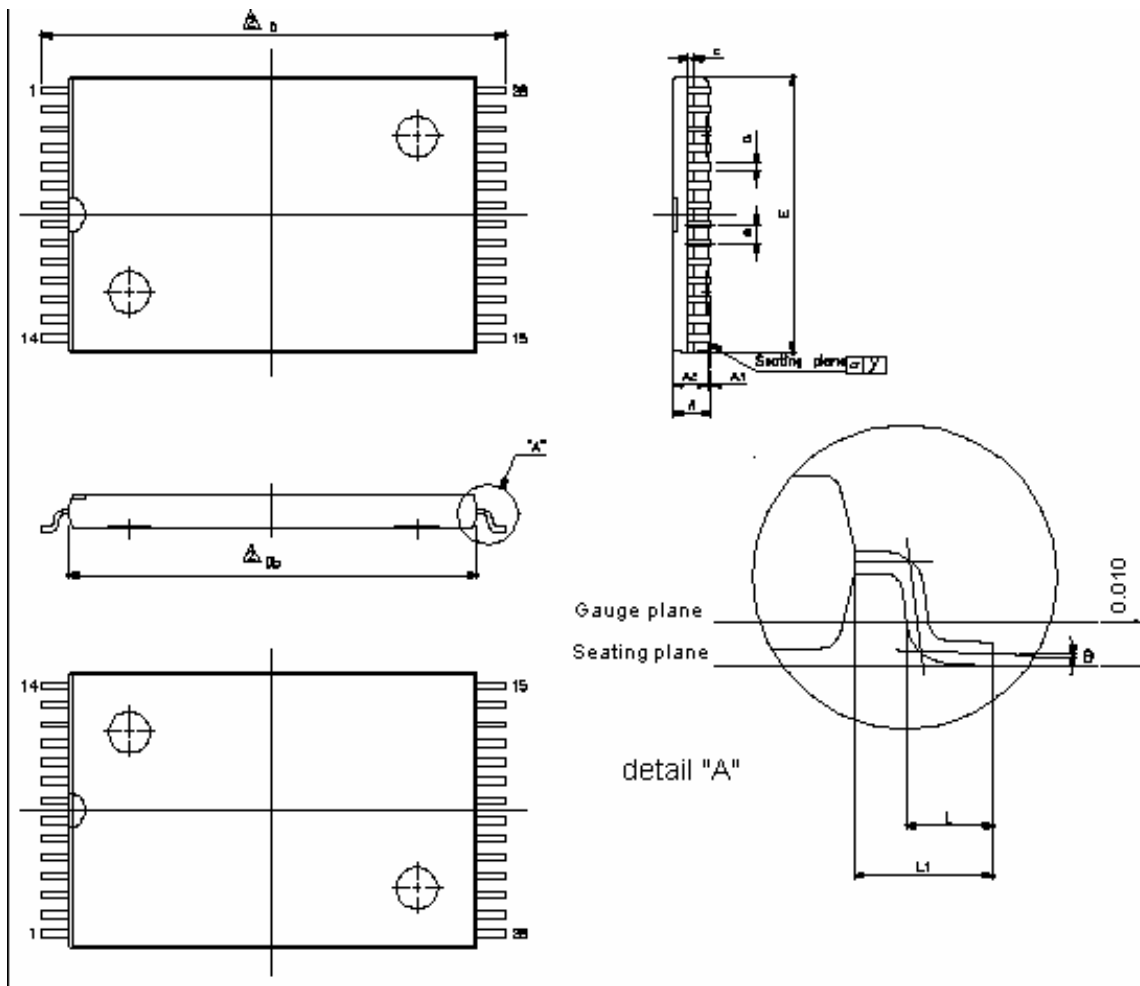


| SYM. | UNIT | |
|------|-------------|--------------|
| | INCH(BASE) | MM(REF) |
| A | 0.120 (MAX) | 3.048 (MAX) |
| A1 | 0.002(MIN) | 0.05(MIN) |
| A2 | 0.098±0.005 | 2.489±0.127 |
| b | 0.016 (TYP) | 0.406(TYP) |
| c | 0.010 (TYP) | 0.254(TYP) |
| D | 0.728 (MAX) | 18.491 (MAX) |
| E | 0.340 (MAX) | 8.636 (MAX) |
| E1 | 0.465±0.012 | 11.811±0.305 |
| e | 0.050 (TYP) | 1.270(TYP) |
| L | 0.05 (MAX) | 1.270 (MAX) |
| L1 | 0.067±0.008 | 1.702 ±0.203 |
| S | 0.047 (MAX) | 1.194 (MAX) |
| y | 0.003(MAX) | 0.076(MAX) |
| θ | 0°~10° | 0°~10° |



8K X 8 BIT LOW POWER CMOS SRAM

28 pin 8mm x 13.4mm sTSSOP Package Outline Dimension



| SYM. | UNIT | INCH(BASE) | MM(REF) |
|----------|------|--------------|------------|
| A | | 0.047 (MAX) | 1.20 (MAX) |
| A1 | | 0.004±0.002 | 0.10±0.05 |
| A2 | | 0.039±0.002 | 1.00±0.05 |
| b | | 0.006 (TYP) | 0.15(TYP) |
| c | | 0.010 (TYP) | 0.254(TYP) |
| Db | | 0.465±0.004 | 11.80±0.10 |
| E | | 0.315±0.004 | 8.00±0.10 |
| e | | 0.022 (TYP) | 0.55(TYP) |
| D | | 0.528±0.008 | 13.40±0.20 |
| L | | 0.020±0.004 | 0.50±0.10 |
| L1 | | 0.0315±0.004 | 0.80±0.10 |
| y | | 0.08(MAX) | 0.003(MAX) |
| θ | | 0°~5° | 0°~5° |

Note : E dimension is not including end flash. The total of both sides' end flash is not above 0.3mm.



8K X 8 BIT LOW POWER CMOS SRAM

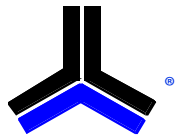
ORDERING INFORMATION

Ordering Codes

| Alliance | Organization | VCC range | Package | Operating Temp | Speed ns |
|------------------------|--------------|-----------|---------------------------|---------------------------------|----------|
| AS6C6264-55PCN | 8k x 8 | 2.7-5.5V | 28pin 600mil PDIP | Commercial ~ 0° C to 70° C | 55 |
| AS6C6264-55SCN | 8k x 8 | 2.7-5.5V | 28pin 330mil SOP | Commercial ~ 0° C to 70° C | 55 |
| AS6C6264-55SIN | 8k x 8 | 2.7-5.5V | 28pin 330mil SOP | Industrial ~ -40° C to 85° C | 55 |
| AS6C6264-55STCN | 8k x 8 | 2.7-5.5V | 28pin sTSOP (8 x 13.4 mm) | Commercial ~ 0° C to 70° C | 55 |
| AS6C6264-55STIN | 8k x 8 | 2.7-5.5V | 28pin sTSOP (8 x 13.4 mm) | Industrial ~ -40° C to 85° C | 55 |

Part numbering system

| AS6C | 6264 | - 55 | X | X | N |
|-----------------------|------------------------------|-------------|---|--|-----------------------------------|
| low power SRAM prefix | Device Number 6264 | Access Time | Package Options: P = 28 pin 600 mil P-DIP S = 28 pin 330 mil SOP ST = 28 pin sTSOP (8mm x 13.4 mm) | Temperature Range: C = Commercial (0° C to +70° C) I = Industrial (-40° to +85° C) | N = Lead Free ROHS Compliant Part |



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