MACOM an AMP company

5-Bit Digital Attenuator 20 - 1000 MHz

AT-103

V2.00

Features

- Attenuation 0.5 dB Steps to 15.5 dB
- CMOS Control Interface
- Internal Latch on Control Input
- Hermetic Case

Guaranteed Specifications* (From-55°C to +85°C)

Frequency Range		20-1000 MHz
Nominal Attenuation**		0.5 dB Steps to 15.5 dB
Attenuation Accuracy	20-500 MHz	±0.25 dB ±2% Max
	20-1000 MHz	±0.35 dB ±2% Max
VSWR	20-500 MHz	1.6:1 Max
	20-1000 MHz	2.0:1 Max
Reference Insertion Loss		5.0 dB Max

Operating Characteristics

Impedance		50 Ohms Nominal
Switching Characteristics		
Switching Time (50% CTL to 90%/10% RF)		8 μS Typ
Transients (In-Band)		20 mV Typ
Input Power for 1 dB Compression	20-1000 MHz	+ 18 dBm Typ
Intermodulation Intercept Point (for two-tone input power up to + 5 dBm)		
Second Order		+ 40 dBm Typ
Third Order		+ 30 dBm Typ
Bias Power		+10 to + 15 VDC @ 30 mA Max (330 mW Typ)
Control		5 line, CMOS Data Bus with Internal Latch controlled by Clock (Data Strobe) and reset inputs.

Environmental
MIL-STD-883 screening available.

* All specifications apply when operated with bias voltage of +15 VDC and a 50 ohm impedance at both RF ports.
** Above reference insertion loss.

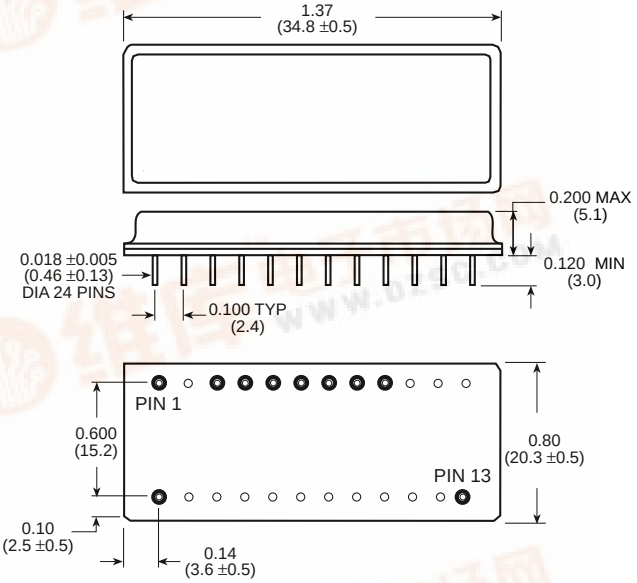
Ordering Information

Model No.	Package
AT-103 PIN	Dual Inline

Pin Configuration

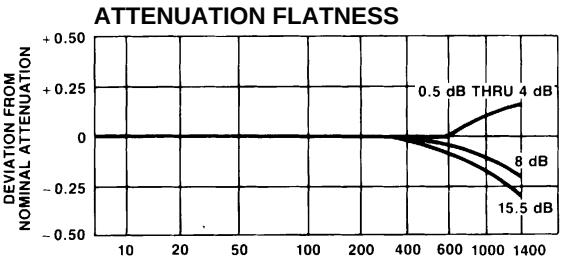
1	2	3	4	5	6	7	8	9	10 - 12	13	14 - 23	24
+ 5V	GND	C	R	0.5	1	2	4	8	GND	RF2	GND	RF1

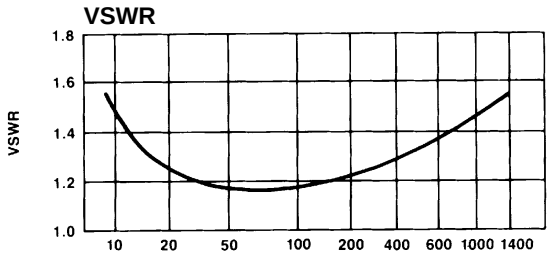
DI-3

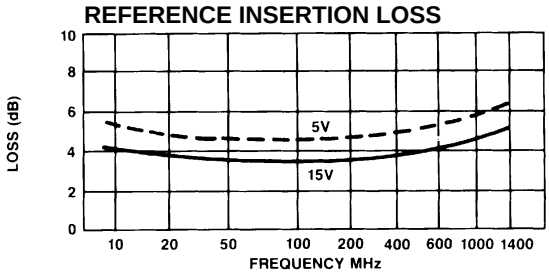


Dimensions in ( ) are in mm.
Unless Otherwise Noted: .xxx = ±0.010 (.xx = ±0.25)
.xx = ±0.02 (.x = ±0.5)
WEIGHT (APPROX.): 0.39 OUNCES 11 GRAMS

Typical Performance







Truth Table

CONTROL INPUT							ATTENUATOR SETTING
0.5	1	2	4	8	C*	R	
0	0	0	0	0	1	1	REFERENCE
1	0	0	0	0	1	1	0.5 dB
0	1	0	0	0	1	1	1 dB
0	0	1	0	0	1	1	2 dB
0	0	0	1	0	1	1	4 dB
0	0	0	0	1	1	1	8 dB
ANY COMBINATION					1	1	SUM OF BITS SELECTED
X	X	X	X	X	0	1	NO CHANGE IN ATTENUATION
X	X	X	X	X	X	0	RESET TO REFERENCE

"1" = LOGIC HIGH
"0" = LOGIC LOW
"X" = DON'T CARE
*CLOCK INPUT STROBES DATA ON RISING EDGE

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