AME, Inc.

# AT7601F Printer Port Controller

## 1. General Description

The AT7601F is a Printer Port Controller. It supports the existing Centronics printer and IEEE 1284 compatible parallel ports

## 2. Features

- 5V parallel port I/O
- IBM PC compatible printer port
- PS/2 compatible bi-directional parallel port
- IEEE 1284 compatible Enhanced Parallel Port (EPP)
- IEEE 1284 compatible Extended Capabilities Port (ECP)
- Legacy parallel ports

## ※Order Information

AT7601F- Commercial Standard

AT7601FG- Green Device with Commercial Standard

| Part Number | Marking | Package |
|---|---|---|
| AT7601FG | AT7601FG<br>yyww AA | LQFP-48 |

Note: yyww represent the date code.

## 3. Pin Configuration

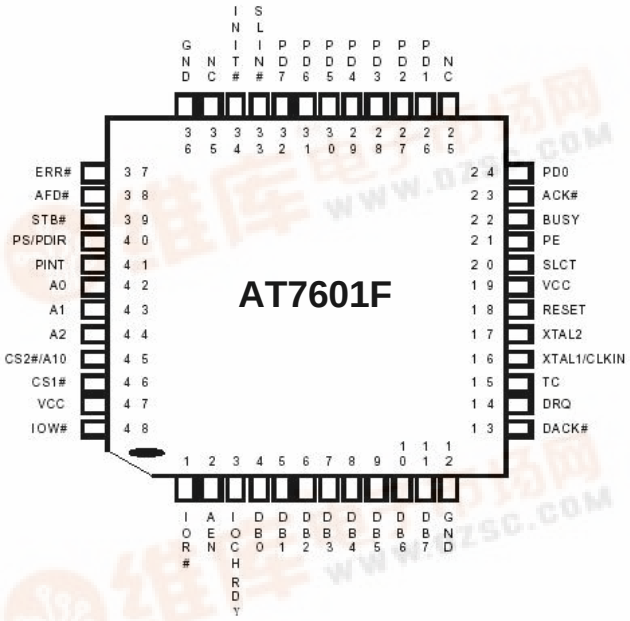



Figure 1. AT7601F Pin Diagram (Top View)

# 4. Pin Description

I - TTL level input
O12 - Out buffer with 12mA drive/sink current
OD12 - Open-drain with 12mA sink current
ICLK - Clock Input
OCLK - Clock Output

| Pin No. | Pin name | I/O Type | Function |
|---|---|---|---|
| 2 | AEN | I | DMA Address Enable: active high, DMA controller has control of the address bus. |
| 3 | IOCHRDY | OD12 | I/O channel Ready: active High |
| 4 - 11 | DB [0: 7] | I/O12 | Data Bus: bi-direction data port |
| 13 | DACK# | I | DMA Acknowledge: Active low |
| 14 | DRQ | O12 | DMA Request: Active high |
| 15 | TC | I | Terminal count: |
| 16 | XTAL1/CLKIN | ICLK | Crystal oscillator input, |
| 17 | XTAL2 | OCLK | Crystal oscillator output, |
| 18 | RESET | I | System Reset: active high |
| 25, 35 | NC | | |
| 40 | PS/PDIR | I<br>O12 | Power on strapping<br>Printer Port Direction Indicator |
| 41 | PINT | OD12/O12 | Print Interrupt |
| 42-44 | A [0: 2] | I | Address select line 0 - 2 |
| 45 | CS2# /A10 | I | A10: Address select line 10<br>Chip Select 2: active low, enables the parallel port / CPU data transfer operation |
| 46 | CS1# | I | Chip Select 1: active low, enables the parallel port / CPU data transfer operation |
| 48 | IOW# | I | I/O write: active low |
| 1 | IOR# | I | I/O read: active low |

**Table 1. Host Interface**

| Pin No. | Pin name | I/O Type | Function |
|---|---|---|---|
| 20 | SLCT | I | Printer Selected input. |
| 21 | PE | I | Printer Paper End input. |
| 22 | BUSY | I | Printer Busy input. |
| 23 | ACK# | I | Printer Acknowledge input: active low |
| 24, 26-32 | PD [0:7] | I/O12 | Printer port data bus. |
| 33 | SLIN# | OD12/O12 | Printer Select output: active low |
| 34 | INIT# | OD12/O12 | Printer Initialization output: active low |
| 37 | ERR# | I | Printer Error input: active low |
| 38 | AFD# | OD12/O12 | Auto Line Feed output: active low |
| 39 | STB# | OD12/O12 | Strobe output: active low |

**Table 2. Print Port Interface**

| Pin No. | Pin name | I/O Type | Function |
|---|---|---|---|
| 19, 47 | VCC | PWR | 5V Supply. |
| 12, 36 | GND | PWR | Ground |

**Table 3. Power Signals**

# 5. Function Description

### 5-1 Printer Interface

The AT7601F fully supports an IBM XT/AT compatible parallel port, bi-directional parallel port (SPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP).

| Pin NO. | Host Connector | Pin Attribute | SPP | EPP | ECP |
|---|---|---|---|---|---|
| 39 | 1 | O | STB# | Write# | STB#*, HostClk** |
| 24, 26 - 32 | 2-9 | I/O | PD [0:7] | PD [0:7] | PD [0:7] |
| 23 | 10 | I | ACK# | Intr | ACK#*, PeriphClk** |
| 22 | 11 | I | BUSY | Wait# | BUSY*, PeriphAck** |
| 21 | 12 | I | PE | PE | Perror*, AckReverse#** |
| 20 | 13 | I | SLCT | Select | SLCT*, Xflag** |
| 38 | 14 | O | AFD# | DataSTB# | AFD#*, HostAck** |
| 37 | 15 | I | ERR# | Error# | Fault#*, PeriphReq** |
| 34 | 16 | O | INIT# | Init# | INIT#*, ReverseReq#** |
| 33 | 17 | O | SLIN# | AddrSTB# | SLIN#*, EcpMode** |

**Table 4. Parallel Port Connector and Different Modes Pin Definitions**

# means active low

* Compatible Mode

** High Speed Mode

**5-2 Enhanced Parallel Port(EPP)**

| SPP Name | EPP Name | I/O Type | EPP Description |
|---|---|---|---|
| STB# | Write# | O | Active low; It indicates a write operation. |
| PD[0:7] | PD [0: 7] | I/O | Bi-directional EPP byte wide address and data bus. |
| ACK# | INTR | I | Interrupt, Active high; Peripheral generates an interrupt to the host. |
| BUSY | Wait# | I | Active low; it is handshake signal. When low, it indicates that the device is ready for next transfer, when high, it indicates that the data transfer is complete. |
| PE | PE | I | Paper End; Same as SPP mode. |
| SLCT | Select | I | Printer selected status; Same as SPP mode. |
| AFD | DataSTB# | O | Data Strobe ; Active low; it indicates a data read or write operation. |
| ERR# | Error# | I | Error; Same as SPP mode. |
| INIT# | INIT# | O | Active low; The EPP device is reset to its initial operating mode. |
| SLIN# | AddrSTB# | O | Address Strobe ; Active low; It indicates an address read or write operation. |

**Table 5. EPP Pin Descriptions**

| A2 | A1 | A0 | Register | Note |
|---|---|---|---|---|
| 0 | 0 | 0 | Data Port | 1 |
| 0 | 0 | 1 | Printer Status Port | 1 |
| 0 | 1 | 0 | Printer Control Port | 1 |
| 0 | 1 | 1 | EPP Address Port | 2,3 |
| 1 | 0 | 0 | EPP Data Port 0 | 2,3 |
| 1 | 0 | 1 | EPP Data Port 1 | 2,3 |
| 1 | 1 | 0 | EPP Data Port 2 | 2,3 |
| 1 | 1 | 1 | EPP Data Port 3 | 2,3 |

**Table 6. EPP Pin Descriptions**

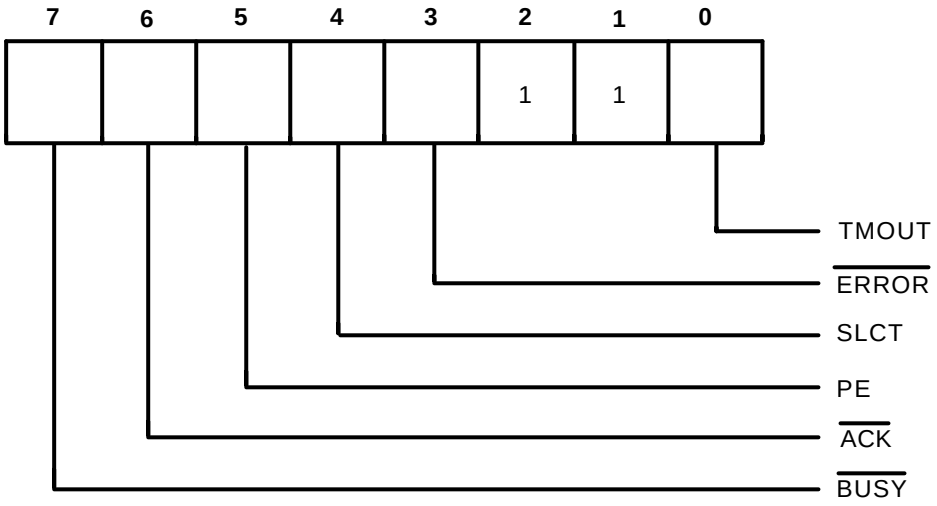
Note 1: These registers are in all mode

Note 2: These registers are in EPP mode

Note 3: For EPP mode, IOCHRDY must be connect to the ISA BUS

**5- 2- 1 Printer Status Port Address Offset = 01H**

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of an IOR# read cycle. The bits of the Status Port are defined as follows:




**Bit 7 BUSY# (BUSY)**

This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data. This bit is the inversion value of the Busy input pin.

**Bit 6 ACK# (ACKNOWLEDGE)**

The level on the ACK# input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

**Bit 5 PE (PAPER END)**

The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

**Bit 4 SLCT (PRINTER SELECTED STATUS)**

The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

**Bit 3 ERR# (ERROR)**

The level on the Error# input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

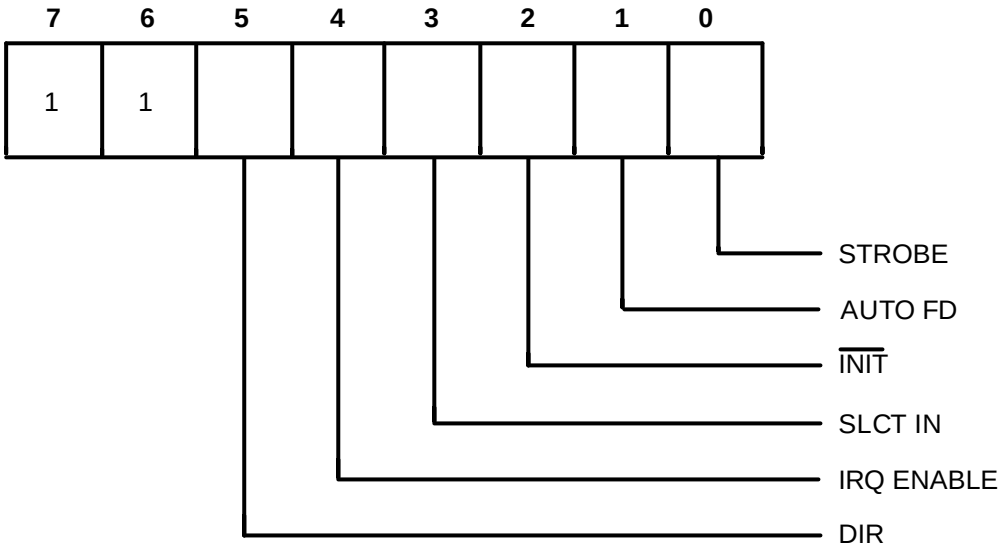
**Bits 1, 2:** are not implemented as register bits, during a read of the Printer Status Register these bits are Logic High.

**Bit 0 TMout: TIME OUT**

The bit is valid in EPP mode only and indicates that a 10 uSec time out has occurred on the EPP bus. A logic 0 means that no time out error has occurred; a logic 1 means that a time out error has been detected. This bit is cleared by a RESET. Writing a one to this bit clears the time out status bit. On a write, this bit is self clearing and does not require a write of a zero. Writing a zero to this bit has no effect.

### 5-2-2 Printer Control Port ADDRESS PORT = 02H

The Control Port is located at an offset of '02H" from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are Logic High.




**Bit 6 and 7** These tow bits are Logic High during a read, and cannot be written.

**Bit 5 PDIR (PARALLEL DIRECTION CONTROL)**

Parallel Direction Control is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, A logic 0 means that the printer port is in output mode (write); A logic 1 means that the printer port is in input mode (read).

**Bit 4 IRQEn (INTERRUPT REQUEST ENABLE)**

The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going ACK# input. When the IRQEn bit is programmed low the IRQ is disabled.

**Bit 3 SLIN (PRINTER SELECT INPUT)**

This bit is inverted and output onto the SLIN# output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

**Bit 2 INIT# (INITIATE OUTPUT)**

A 0 starts the printer (50 microsecond pulse, minimum).

**Bit 1 AFD (AUTOFEED)**

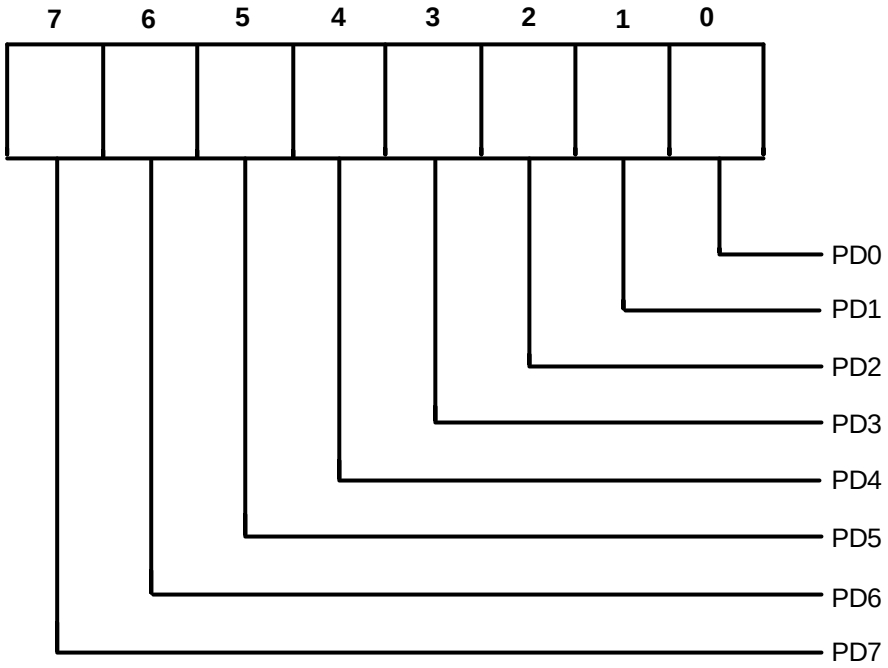
This bit is inverted and output onto the AFD# output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

**Bit 0 STB (STROBE)**

A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse. This bit is inverted and output onto the STB# output.

### 5-2-3 EPP Address Port ADDRESS OFFSET = 03H

The address port is available only in EPP mode. Bit definitions are as follows:

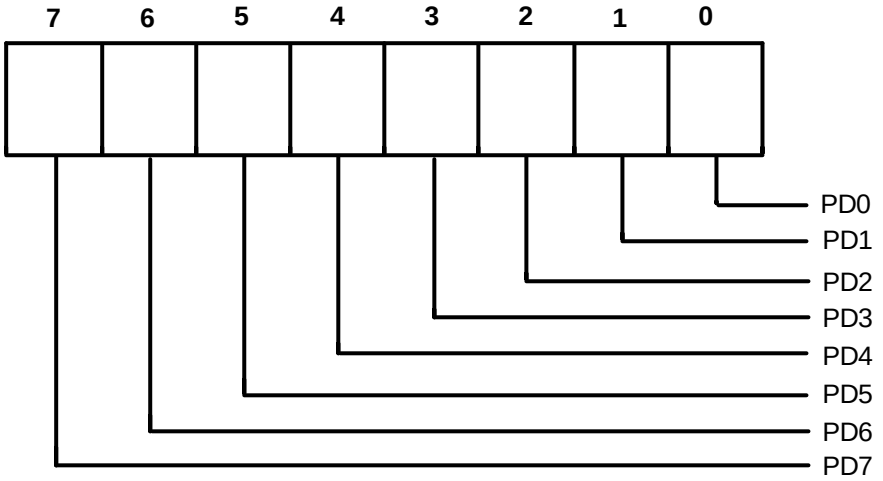



The contents of DB0-DB7 are b uffered (non- inverting) and output to ports PD0-PD7 during a write operation. The leading edge of LOW causes an EPP address write cycle to be performed, and the trailing edge of LOW latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR causes and EPP address read cycle to be performed and the data to be output to the host CPU.

**5-2-4 EPP Data Port 0 ~ 3**

These four registers are available only in EPP mode. Bit definitions of each port are as follows:




When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of LOW latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of LOR causes an EPP read cycle to be performed and the data to be output to the host CPU.

| REGISTER | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data Port | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Status Port | BUSY# | ACK# | PE | SLCT | ERR# | 1 | 1 | TMout |
| Control Port | 1 | 1 | PDIR | IRQEn | SLIN | INIT# | AFD | STB |
| EPP Address Port | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 0 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 1 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 2 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| EPP Data Port 3 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |

**Table 7. Parallel Port and EPP Registers**

### 5-2-5 EPP 1.9 Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STB, AFDD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle (IOR# or IOW# asserted ) to WAIT# being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the WRITE# signal to always be asserted.

### 5-2-6 EPP Version 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STB, AFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.
In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle (IOR# or IOW# asserted) to the end of the cycle IOR# or IOW# deasserted). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

## 5-3 Extended Capabilities Parallel (ECP) Port

ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

- High performance half-duplex forward and reverse channel
- Interlocked handshake, for fast reliable transfer
- Optional single byte RLE compression for improved throughput(64:1)
- Channel addressing for low-cost peripherals
- Maintains link and data layer separation
- Permits the use of active output drivers
- Permits the use of adaptive signal timing
- Peer-to-peer capability

| Pin Name | ECP Mode Name | I/O Type | Description |
|---|---|---|---|
| STB# | HostClk | O | During write operations STB# registers data or address into the slave on the asserting edge. These signal handshakes with Busy. |
| PD [7:0] | D0-D7 | I/O | These signals contain address or data or RLE data. |
| ACK# | PeriphClk | I | This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with AFD# in reverse. |
| Busy | PeriphAck | I | This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low. |
| PError | AckReverse# | I | This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge ReverseReq#. The host relies upon AckReverse# to determine when it is permitted to drive the data bus. |
| SLCT | Xflag | I | Indicates printer on line. |
| AFD# | HostAck | O | Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when AFD# (HostAck) is high and an 8-bit command is transferred when it is low. |
| Fault# | PeriphReq# | I | Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode. |
| INIT# | ReverseReq# | O | This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. |
| SLIN# | ECPMode | O | This signal is always deasserted in ECP mode. |

**Table 8. ECP Pin Descriptions**

| Name | Address | I/O Type | Mode | Function |
|---|---|---|---|---|
| Data | Base+000h | R/W | 000-001 | Data Register |
| ECP-AFIFO | Base+000h | R/W | 011 | ECP FIFO (Address) |
| DSR | Base+001h | R/W | All | Status Register |
| DCR | Base+002h | R/W | All | Control Register |
| C-FIFO | Base+400h | R/W | 010 | Parallel Port Data FIFO |
| ECP-DFIFO | Base+400h | R/W | 011 | ECP FIFO (DATA) |
| T-FIFO | Base+400h | R/W | 110 | Test FIFO |
| Cnfg-A | Base+400h | R | 111 | Configuration Register A |
| Cnfg-B | Base+401h | R/W | 111 | Configuration Register B |
| ECR | Base+402h | R/W | All | Extended Control Register |

**Table 9. ECP Register Definitions**

Note 1: These address are added to the parallel port base address as selected by configuration register or jumpers.

Note 2: All address are qualified with AEN. Refer to the AEN pin definition.

Note 3: The register definitions are based on the standard IBM address

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | NOTE |
|---|---|---|---|---|---|---|---|---|---|
| Data | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 | |
| ECP-AFIFO | Addr/RLE | Address or RLE field | | | | | | | ** |
| DSR | BUSY# | ACK# | PError | SLCT | Fault# | 1 | 1 | 1 | * |
| DCR | 1 | 1 | PDIR | AckIntEn | SLIN | INIT# | AFD | STB | * |
| C-FIFO | Parallel Port Data FIFO | | | | | | | | ** |
| ECP-DFIFO | ECP Data FIFO | | | | | | | | ** |
| T-FIFO | Test FIFO | | | | | | | | ** |
| Cnfg-A | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| Cnfg-B | Compress | IntrValue | IRQ | IRQ | IRQ | DMA | DMA | DMA | |
| ECR | MODE | | | ErrIntrEn# | DMA En/Dis | Service Intr | FIFO Full | FIFO EMPTY | |

**Table 10. Parallel Port and ECP Registers**

* Registers are in all modes.

** All FIFOs use one common 16-byte FIFO.

**5-3-1.1 Data and ECP- AFIFO Port ADDRESS OFFSET = 400H**

**Modes 000 and 001 (Data Port)**

The Data Port is located at an offset of '00H'from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus on the rising edge of the IOW# input. The contents of this register are buffered (non inverting) and output onto the PD0-PD7 ports. During a READ operation, PD0-PD7 ports are read and output to the host CPU.

**Mode 011 (ECP FIFO-Address/RLE)**

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is only defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet.

**5-3-1.2 Device Status Register (DSR)**

The Status Port is located at an offset of '01H'from the base address. Bits 0-2 are not implemented as register bits; during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

**Bit 0-2**: the Status Port is located at an offset of '01H'from the base address. Bits 0-2 are not implemented as register bits; during a read of the Printer Status Register these bits are a low level.

**Bit 3 Fault# :** The level on the Fault# input is read by the CPU as bit 3 of the Device Status Register.

**Bit 4 SLCT:** The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

**Bit 5 PError:** The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

**Bit 6 ACK#:** The level on the ACK# input is read by the CPU as bit 6 of the Device Status Register.

**Bit 7 BUSY#:** This complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

**5-3-1.3 Device Control Register (DCR)**

The Control Register is located at an offset of '02H'from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

**Bit 6 and 7** during a read are a low level, and cannot be written.

**Bit 5 PDIR:**

If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

**Bit 4 AckIntEn-INTERRUPT REQUEST ENABLE:** The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the ACK# input. Refer to the description of the interrupt under Operation, Interrupts.

**Bit 3 SLIN**: This bit is inverted and output onto the SLIN# output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

**Bit 2 INIT#** (INITIATE OUTPUT):

This bit is output onto the INIT# output without inversion.

**Bit 1 AFD** (AUTOFEED):

This bit is inverted and output onto the AFD# output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

**Bit 0 STB** (STROBE):

This bit is inverted and output onto the STROBE# output.

**5-3-1.4 C-FIFO (Parallel Port Data FIFO) Mode = 010 ADDRESS OFFSET = 400H**

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

**5-3-1.5 ECP- DFIFO (ECP Data FIFO) Mode = 011 ADDRESS OFFSET = 400H**

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned. Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

**5-3-1.6 T- FIFO (Test FIFO Mode) Mode = 110 ADDRESS OFFSET = 400H**

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction.

Data in the T-FIFO will not be transmitted to the parallel port lines using a hardware protocol handshake. However, data in the T-FIFO may be displayed on the parallel port data lines.

The T-FIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full T-FIFO, the new data is not accepted into the T-FIFO. If an attempt is made to read data from an empty T-FIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The T-FIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and ServiceIntr bits.

The writeIntrThreshold can be determined by starting with a full T-FIFO, setting the direction bit to 0 and emptying it a byte at a time until ServiceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty T-FIFO a byte at a time until ServiceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of T-FIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the T-FIFO will return 44h, 33h, 22h in the same order as was written.

**5-3-1.7 Cnfg-A (Configuration Register A) Mode = 111 ADDRESS OFFSET = 400H**

This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord =1 byte)

**5-3-1.8 Cnfg-B (Configuration Register B) Mode = 111 ADDRESS OFFSET = 400H**

The bit definitions are as follows:

**Bit 7 Compress:** This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

**Bit 6 IntrValue:** Returns the value on the ISA IRQ line to determine possible conflicts.

**Bits** [3:0] **Parallel Port IRQ**

Refer to Table A.

**Bits [2:0] Parallel Port DMA**

Refer to Table B.

**Table A**

| IRQ SELECTED | CONFIG REG B BITS 5:3 |
|---|---|
| 15 | 110 |
| 14 | 101 |
| 11 | 100 |
| 10 | 011 |
| 9 | 010 |
| 7 | 001 |
| 5 | 111 |
| All Others | 000 |

**Table B**

| DMA SELECTED | CONFIG REG B BITS 2:0 |
|---|---|
| 3 | 011 |
| 2 | 010 |
| 1 | 001 |
| All Others | 000 |

**5-3-1.9 ECR (Extended Control Register) Mode = all ADDRESS OFFSET = 402H**

This register controls the extended ECP parallel port functions.

**Bit 7,6,5:** These bits are Read/Write and select the Mode.

| Mode [7:5] | Description |
|---|---|
| 000 | Standard Parallel Port Mode. In this mode the FIFO is reset and common collector drivers are used on the control lines (STB#, AFD#, lNIT# and SLIN#). Setting the direction bit will not tri-state the output drivers in this mode. |
| 001 | PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull). |
| 010 | Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull). |
| 011 | ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ECP-DFIFO and bytes written to the ECP-AFIFO are placed in a single FIFO and transmitted automatically to the peripheral using ECP parallel port and packed into bytes in the ECP-DFIFO. All drivers have active pull-ups (push-pull). |
| 100 | Selects EPP Mode: In this mode, EPP is selected if the EPP supported option in selected in configuration register L3-CRFO. All drivers have active pull-ups (push-pull). |
| 101 | Reserved |
| 110 | Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull). |
| 111 | Configuration Mode. In this mode the Cnfg-A, Cnfg-B registers are accessible at Ox400 and Ox401. All drivers have active pull-ups (push-pull). |

**Table 11. Mode Table**

**Bit 4** ErrIntrEn# : Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of Fault#.

0 Enables an interrupt pulse on the high to low edge of Fault#. Note that an interrupt will be generated if Fault# is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ECR and the write of the ECR.

**Bit 3 DMAEn**

Read/Write

1 Enables DMA (DMA starts when ServiceIntr is 0).

0 Disables DMA unconditionally.

**Bit 2 ServiceIntr**

Read/Write

Disables DMA and all of the service interrupts.

Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred ServiceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.

Case DMAEn=1

During DMA (this bit is set to a 1 when terminal count is reached).

Case DMAEn=0 direction=0

This bit shall be set to 1 whenever there are WriteIntrThreshold or more bytes free in the FIFO.

Case DMAEn=0 direction=1

This bit shall be set to 1 whenever there are ReadIntrThreshold or more valid bytes to be read from the FIFO.

**Bit 1 full**

Read only

1 The FIFO cannot accept another byte or the FIFO is completely full.

0 The FIFO has at least 1 free byte.

**Bit 0 empty**

Read only

1 The FIFO is completely empty.

0 The FIFO contains at least 1 byte of data.

### 5-3-2 Operation

Mode Switching / Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer.

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

Once in an extended forward mode the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In this case all control signals will be deasserted before the mode switch. In an ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001. Since the automatic hardware ECP reverse handshake only cares about the state of the FIFO it may have acquired extra data which will be discarded. It may in fact be in the middle of a transfer when the mode is changed back to 000 or 001. In this case the port will deassert AFD# independent of the state of the transfer. The design shall not cause glitches on the handshake signals if the software meets the constraints above.

#### 5-3-2.1 ECP Operation

Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

- Set Direction=0, enabling the drivers.
- Set Strobe=0, causing the STB# signal to default to the deasserted state.
- Set AutoFeed=0, causing the AFD# signal to default to the deasserted state.
- Set mode=011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ECP-AFIFO or ECP-DFIFO respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode=001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode= 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ECP-DFIFO as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

#### 5-3-2.2 Termination form ECP mode

Termination form ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only is specific well-defined states. The termination can only be executed while the bus is in the forward direction. While the channel is in the reverse direction, it must first be transitioned into the forward direction.

**5-3-2.3 Command/Data**

ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8-bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8-bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

**5-3-2.4 Data Compression**

The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ECP-AFIFO and the data byte is written to the ECP-DFIFO.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

**TABLE C**

Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeriphAck Low)

| D7 | D(6:0) |
|---|---|
| 0 | Run-Length Count (0-127)<br>(mode 0011 0X00 only) |
| 1 | Channel Address (0-127) |

**5-3-2.5 Pin Definition**

The drivers for STB#, AFD#, lNIT# and SLIN# are open-collector in mode 000 and are push-pull in all other modes.

**5-3-2.6 ISA Connections**

The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide; byte aligned and end on a byte boundary. (The PWord value can be obtained Configuration Register A, Cnfg-A, described in the next section.) single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

**5-3-2.7 Interrupts**

The interrupts are enabled by ServiceIntr in the ECR register.

ServiceIntr = 1 Disables the DMA and all of the service interrupts.

ServiceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold. The interrupt generated is ISA friendly in that it must pulse the interrupt line low, allowing for interrupt sharing. After a brief pulse low following the interrupt event, the interrupt line is tri-stated so that other interrupts may assert.

An interrupt is generated when:

1. For DMA transfers: When ServiceIntr is 0, DMAEn is 1and the DMA TC is received.
2. For Programmed I/O:
   a. When ServiceIntr is 0, DMAEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when ServiceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.
   b. When ServiceIntr is 0, DMAEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when ServiceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO
3. When ErrIntrEn# is 0 and Fault# transitions from high to low or when ErrIntrEn# is set from 1 to 0 and ErrIntrEn# is set from 1 to 0 and Fault# is asserted.
4. When AckIntEn is 1 and the ACK# signal transitions from a low to a high.

**5-3-2.8 FIFO Operation**

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or PDRQ depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e.2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e.2) is used with a "sluggish" system by affording a ling latency period after a service request, but results in more frequent service requests.

**5-3-2.9 DMA Transfers**

DMA transfers are always to or from the ECP-DFIFO, T-FIFO or C-FIFO. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets DMAEn to 1 and ServiceIntr to 0. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and ServiceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests dReq shall not be asserted for more than 32 DMA cycles in a row. The FIFO is enabled directly by asserting PDACK# and addresses need not be valid. PINTR is generated when a TC is received. RDRQ must not be asserted for more than 32 DMA cycles in a row. After the 32nd cycle, PDRQ must be kept unasserted until PDACK# is deasserted for a minimum of 350nsec. (Note: The only way to properly terminate DMA transfers is with a TC.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting ServiceIntr to 1, followed by setting DMAEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting DMAEn to 1, followed by setting ServiceIntr to 0.

**5-3-2.10 DMA Mode - Transfers from the FIFO to Host**

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP activates the PDRQ pin whenever there is data in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The ECP will deactivate the PDRQ pin when the FIFO becomes empty or when the TC becomes true (qualified by PDACK#), indicating that no more data is required. PDRQ goes inactive after PDACK# goes active for the last byte of a data transfer (or on the active edge of lOR#, on the last byte, if no edge is present on PDACK#). If PDRQ goes inactive due to the FIFO going empty, then PDRQ is active again as soon as there is one byte in the FIFO. If PDRQ goes inactive due to the TC, then PDRQ is active again when there is one byte in the FIFO, and ServiceIntr has been re-enabled. (Note: A data underrun may occur if PDRQ is not removed in time to prevent an unwanted cycle.)

**5-3-2.11 Programmed I/O (NON-DMA) Mode**

The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the WriteIntrThreshold, ReadIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ECP-DFIFO at 400H and ECP-AFIFO at 000H or from

The ECP-DFIFO located at 400H, or to/from the T-FIFO at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets DMAEn to 0 and ServiceIntr to 0. The ECP requests programmed I/O transfers from the host by activating the PINTR pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

**5-3-2-12 Programmed I/O - Transfer from the FIFO to Host**

In the reverse direction an interrupt occurs when ServiceIntr is 0 and ReadIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise ReadIntrThreshold bytes may be read from the FIFO in a single burst. ReadIntrThreshold=16-<threshold>) data bytes in FIFO

An interrupt is generated when ServiceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold=12, then the interrupt is set whenever there are 4-16 bytes in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

**5-3-2-13 Programmed I/O -- Transfer from the Host to FIFO**

In the forward direction an interrupt occurs when ServiceIntr is 0 and there are WriteIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with WriteIntrThreshold bytes. WriteIntrThreshold=(16-<threshold>) free bytes in FIFO.

An interrupt is generated when ServiceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold=12. then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The PINT pin can be used for interrupt-driven systems. The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty. It can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART2 and the parallel port. For each logical device, two types of power management are provided; direct powerdown and auto powerdown.

# 6. Configuration Register

The configuration registers of AT7601F are implemented to provide special function control, such as power-down mode, I/O port tri-state control, and select address-decoding modes. The current IRQ and DMA channel used for AT7601F can be setting in configuration registers.

The configuration registers can only be accessed through configuration I/O ports (INDEX and DATA) under configuration mode. These two ports'addresses are assigned to high base address+04H and high base address+05H.

To enter configuration mode, the configuration Key (78H) must be write twice into INDEX register successively. And write AAH into INDEX register to exit configuration mode.

An example program for entering configuration mode, accessing configuration register, and exiting configuration mode as shown following:

```
; ***************************************
; * ENTER CONFIG MODE             *
; * Low base address: 378H        *
; * And address mode 0 is selected *
; * A10 is connected to A10       *
;***************************************
MOV DX,77CH
MOV AL,78H
OUT     DX,AL
OUT     DX,AL
;***********************************
; * Accessing Config Register *
;***********************************
MOV DX,77CH
MOV AL ,F0H   ; Accessing CR-F0
OUT DX,AL
INC DX
MOV AL,3FH
OUT DX,AL ; Write 3FH to CR-F0
IN AL,DX ; Read CR-F0
;*******************************
;*   Exit  Config  Mode    *
;*******************************
DEC DX
MOV AL,AAH
OUT DX,AL
INT 21
```

**6-1 Configuration Register Description**

**CR20 CHIP ID REGISTER 1(Default 0x76)**

This register is read-only.

**CR21 CHIP ID REGISTER 2(Default 0x01)**

This register is read-only.

**CRF0 MODE CONTROL REGISTER (Default 0x3F)**

Bit 7: Parallel Port Interrupt Type

This bit is valid except Parallel Port Mode is set in Printer Mode(Bit[2:0]=100), os Standard& Bi-directional Mode(Bit[2:0]=000).

= 1 Pulsed low, released to high-Z.

= 0 Parallel Port Interrupt follows ACK# when Parallel Port is in EPP mode or Printer Mode, SPP Mode, or EPP mode under ECP mode.

Bit 6-3: ECP FIFO Threshold.

Bit 2-0: Parallel Port Mode (Default 111)

= 100 Printer Mode

= 000 Standard and Bi-direction (SPP) mode

= 001 EPP - 1.9 and SPP mode

= 101 EPP - 1.7 and SPP mode

= 010 ECP mode

= 011 ECP and EPP - 1.9 mode

= 111 ECP and EPP - 1.7 mode.

**CRF1 ECP IRQ/DRQ CHANNEL SELECT REGISTER (Default 0x31)**

Bit 7-6: Reserved.

Bit 5-4: ECP DRQ Channel Select. These two bits reflect to ECP Extended Control Register bit 1-0.

= 00 No DMA.

= 01 DRQ 1.

= 10 DRQ 2.

= 11 DRQ 3.

Bit 2-0: ECP IRQ Channel Select. These three bits reflect to ECP Extended Control Register bit 5-3.

= 000 All others.

= 001 IRQ 7.

= 010 IRQ 9.

= 011 IRQ 10.

= 100 IRQ 11

= 101 IRQ 14.

= 110 IRQ 15.

= 111 IRQ 5.

**CRF2 CHIP CONTROL REGISTER 1(Default 0x00)**

Bit 7: Power-Down.

= 0 Chip is operating.

= 1 Chip is power-down.

Bit 6: Tri-state Control.

= 0 Output ports are driving.

= 1 Output ports are tri-state if bit7 is set.

Bit 5: Legacy IRQ/DRQ Select.

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ.

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ.

Bit 4-2: Reserved.

Bit 1: Enable/Disable DRQ.

= 0 DRQ enable.

= 1 DRQ disable.

Bit 0: Enable/Disable IRQ.

= 0 IRQ enable.

= 1 IRQ disable.

**CRF3 CHIP CONTROL REGISTER 2(Default 0b0000000s)**

Bit 7: Lock Register.

= 0 Unlock

= 1 Configuration mode is locked and exit. The host can access configuration register any more unless system reset.

Bit 6-1: Reserved.

Bit 0: Chip Address Mode Select. This bit latches the power-on strapping value on PDIR(pin 40) during system reset.

= 0 Pin 45 is defined as A10. To access high bank registers of ECP port, A10 must set high and CS1# set low.

= 1 Pin 45 is defined as CS2#. Set CS2# to low and keep CS1# high fir accessing high bank registers of ECP port.

TA = 0-70°C, Vcc = 5.0V ± 10% unless otherwise specified.

| Symbol | Parameter | Limits | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| T1 | ANE setup to command active | 40 | | | ns | |
| T2 | Command width | 60 | | | ns | |
| T3 | ANE hold from command inactive | 5 | | | ns | |
| T4 | Data access from IOR# active | | | 100 | ns | |
| T5 | Data setup to IOW# inactive | 40 | | | ns | |
| T6 | Data hold from command inactive | 10 | | | ns | |
| T7 | PD [0:7], STB#, AFD#, INIT, SLIN# delay from IOW# inactive | | | 100 | ns | |
| T8 | Interrupt delay from ACK# | | | 60 | ns | |
| T9 | Interrupt pre-charge pulse at release | | | 10 | ns | |
| T10 | TC pulse width | 60 | | | ns | |
| T11 | TC active to DRQ inactive | | | 100 | ns | |
| T12 | DRQ active to DACK# active | 0 | | | ns | |
| T13 | DRQ inactive delay from DACK# active | | | 100 | ns | |
| T14 | PD [0:7] setup to STB# active | | 600 | | ns | |
| T15 | STB# width | | 600 | | ns | |
| T16 | PD [0:7], hold from STB# inactive | | 450 | | ns | |
| T17 | PD [0:7], hold from BUSY inactive | | 80 | | ns | |
| T18 | STB# active to BUSY active (handshake) | | | 500 | ns | |
| T19 | BUSY inactive to STROBE active (cycle delay) | | 680 | | ns | |
| T20 | PD [0:7], AFD# setup to STB# active | | 0 | 60 | ns | |
| T21 | PD [0:7], AFD#D hold from BUS active | | 80 | 180 | ns | |
| T22 | STB# inactive to BUSY inactive | | 0 | | ns | |
| T23 | BUSY inactive to STB# active | | 80 | 200 | ns | |
| T24 | STB# active to BUSY active | | 0 | | ns | |
| T25 | BUSY active to STB# inactive | | 80 | 180 | ns | |
| T26 | PD [0:7], BUSY setup to ACK# active | | 0 | | ns | |
| T27 | PD [0:7], data hold from AFD# active | | 0 | | ns | |
| T28 | ACK# inactive to AFD# active | | 80 | 200 | ns | |
| T29 | AFD# active to ACK# active | | 0 | | ns | |
| T30 | ACK# active to AFD# inactive | | 80 | 200 | ns | |
| T31 | AFD# inactive to ACK# inactive | | 0 | | ns | |
| T32 | Host address setup to IOW# active | | 40 | | ns | |
| T33 | Host address hold from IOW# active | | 10 | | ns | |

**Table 12. AC Electrical Characteristics**

TA=0 ~70°C, Vcc=5.0V ± l0% unless otherwise specified.

| Symbol | Parameter | Limits | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| T34 | Hose data setup to IOW# active | | 0 | 20 | us | |
| T35 | Hose data hold from IOW# active | | 0 | | us | |
| T36 | IOW# active to IOCHRDY low | | 0 | 20 | us | |
| T37 | IOCHRDY high to Host terminate (IOW# inactive) | | 10 | | us | |
| T38 | IOW# inactive to Host command active (IOW# or IOR#) | | 40 | | us | |
| T39 | IOCHRDY pre-charge width at release | | | 10 | us | |
| T40 | Hose address setup to IOR# active | | 40 | | us | |
| T41 | Hose address hold from IOR# active | | 10 | | us | |
| T42 | Hose data setup to IOR# inactive | | 0 | 20 | us | |
| T43 | Host data hold from IOR# inactive | | 0 | | us | |
| T44 | IOR# active to IOCHRDY low | | 0 | 20 | us | |
| T45 | IOCHRDY high to Host terminate (IOR# inactive) | | 10 | | us | |
| T46 | IOR# inactive to Host commandactive (IOW# or IOR#) | | 40 | | us | |

**Table 12. AC Electrical Characteristics**

| Parameter | Maximum | Unit |
|---|---|---|
| Supply range | 7 | V |
| Voltage at any pin | GND-0.3V to VCC +0.3 | |
| Operating temperature | 0 to +70 | °C |
| Storage temperature | -140 to +150 | |
| Package dissipation | 500 | mW |

**Table 13. Absolute Maximum Ratings**

TA=0 ~70$^{O}$C, Vcc=5.0V ± 10% unless otherwise specified.

| Symbol | Parameter | Limits | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| VILCK | Clock Input Low level | -0.5 | | 0.6 | V | |
| CIHCL | Clock Input High level | 3 | | VCC | V | |
| VIL | Input Low level | -0.5 | | 0.8 | V | |
| VIH | Input High level | 2 | | VCC | V | |
| VOL | Output Low level | | | 0.4 | V | Except PDIR, |
| VOL | Output Low level | | | 0.4 | V | DB[0:7] |
| PDIR | IDL=4mA | | | | | IOL=20mA |
| VOH | Output high level | 2.4 | | | V | DB[0:7], |
| | | | | | | IOL=12mA |
| VOH | Output High level | 2.4 | | | V | |
| PDIR | IOH=-1 mA | | | | | Except PDIR, |
| ICC | Avg. power supply current | | 5 | 7 | mA | DB[0:7] |
| IIL | Input leakage | | | 10 | µA | IOH=-20mA |
| ICL | Clock leakage | | | 10 | µA | DB[0:7], |
| RIN | Internal pull up/down resistances | 25 | | 50 | kΩ | IOL=-12mA |

**Table 14. DC Electrical Characteristics**

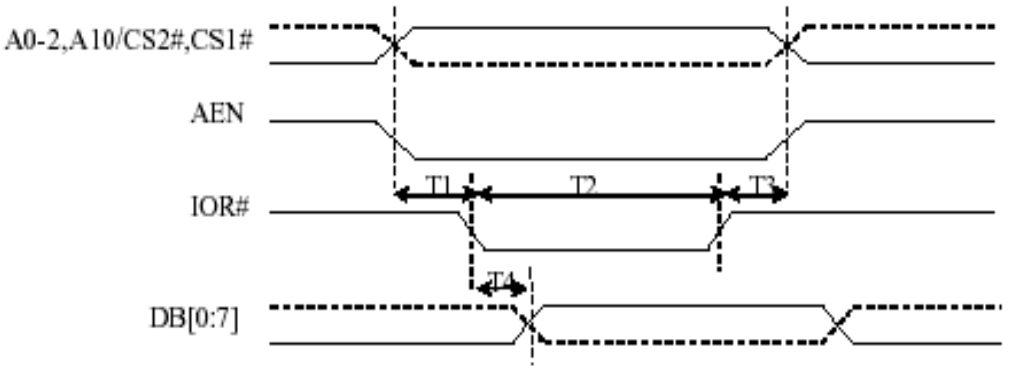



Figure 2.1 General Read/Write Timing

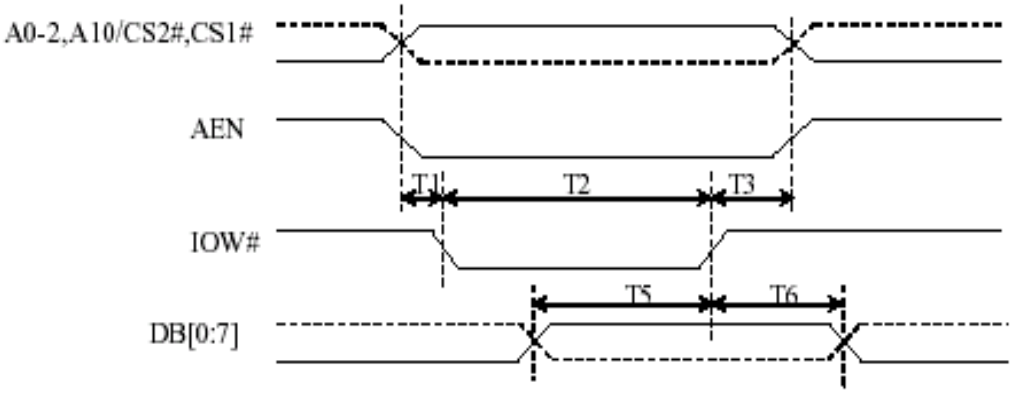



Figure 2.2 General Read/Write Timing

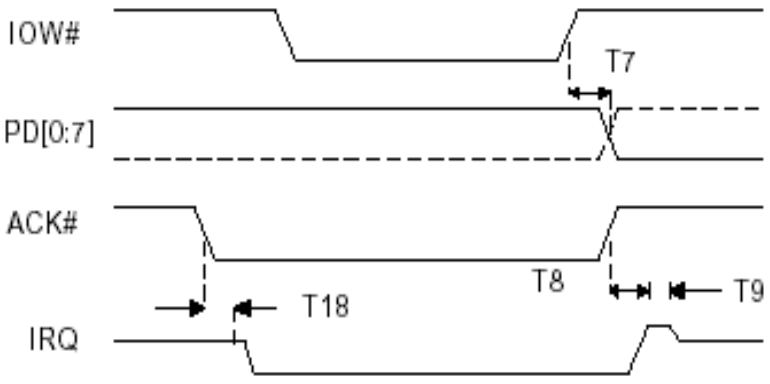



Figure 3. Parallel Port Timing in SPP, PS/2 Mode

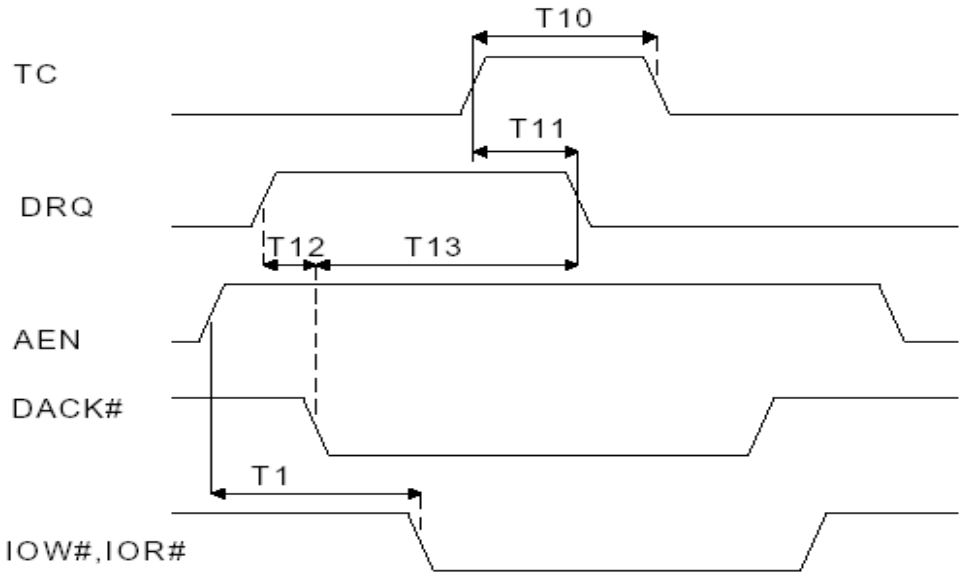



Figure 4. Host DMA Timing in ECP Mode

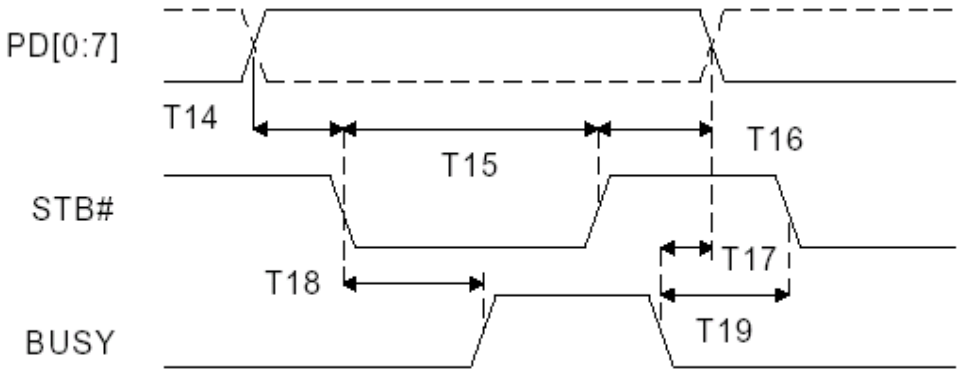



Figure 5. Parallel Port FIFO Timing

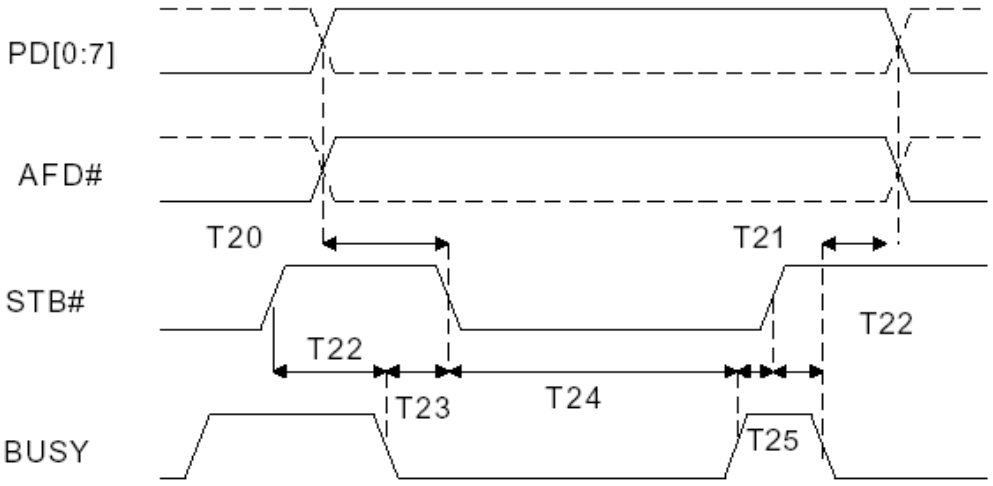



Figure 6. Parallel Port Forward Timing in ECP Mode

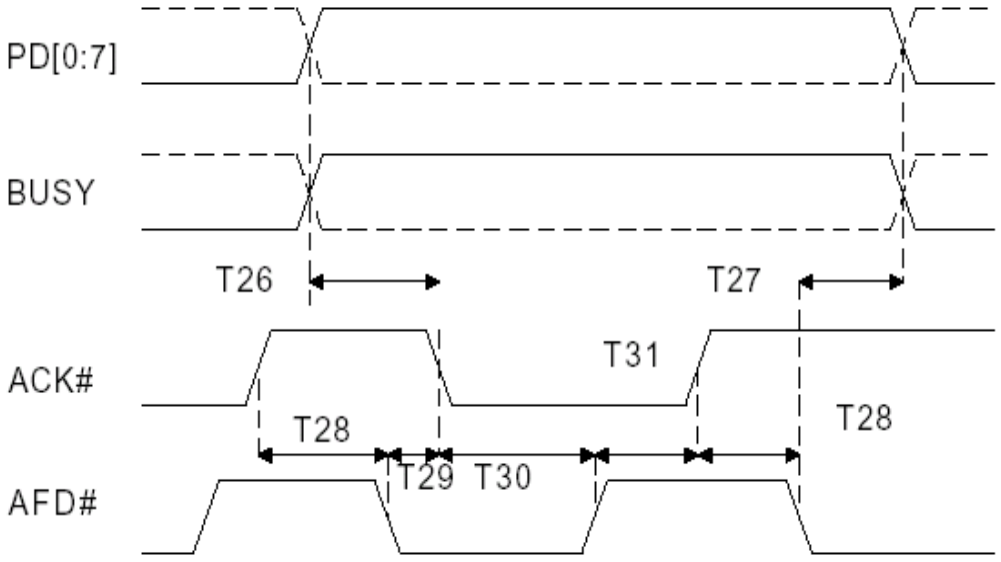



Figure 7. Parallel Port Reverse Timing in ECP Mode

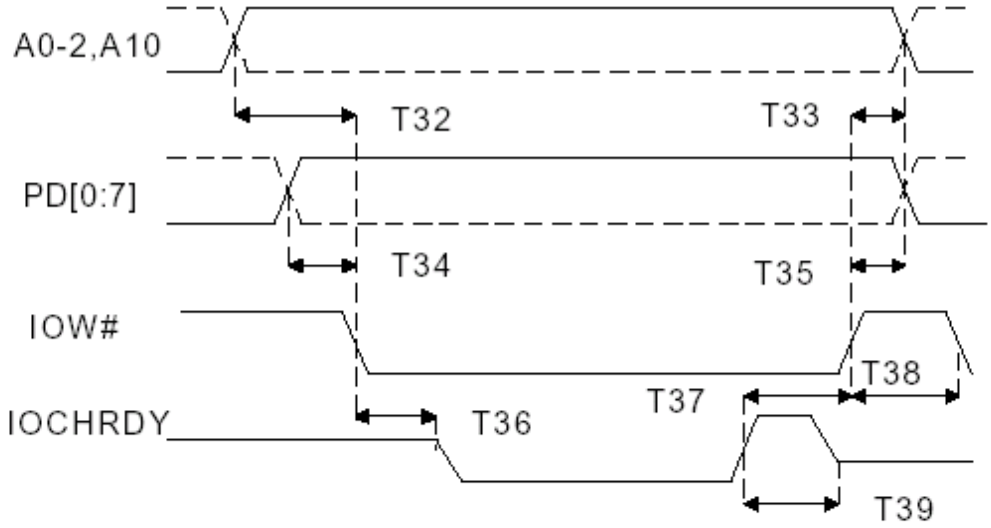



Figure 8. Address or Data Write Timing in EPP Mode

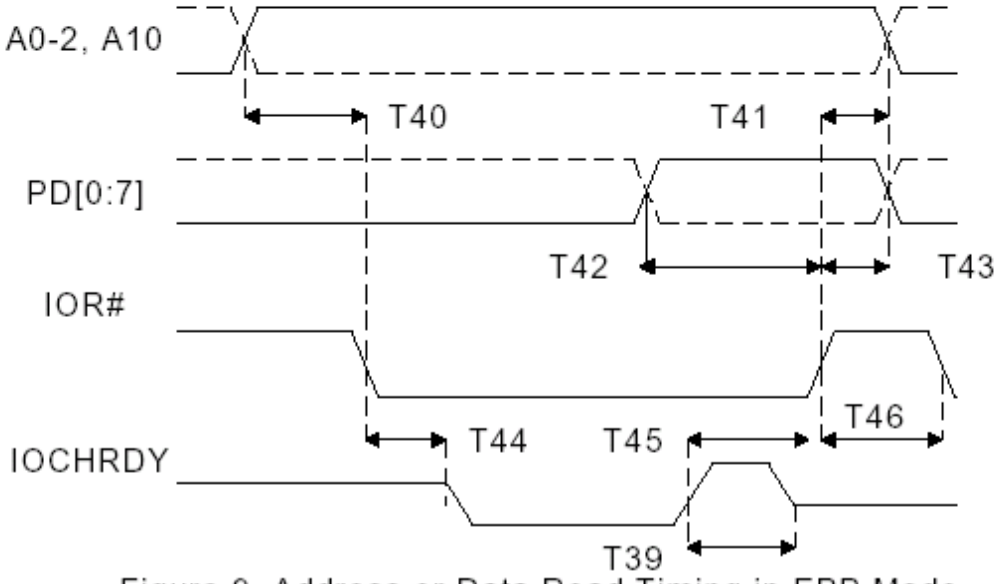
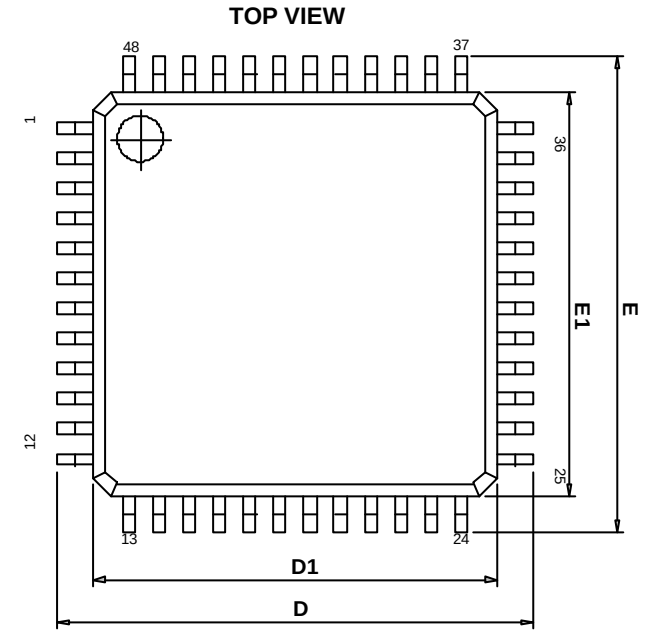


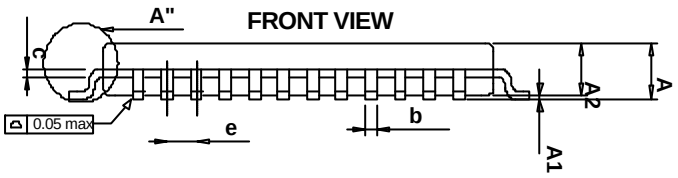

Figure 9. Address or Data Read Timing in EPP Mode

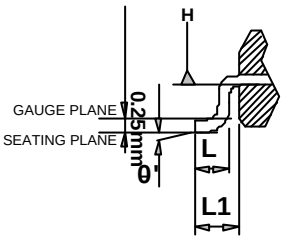
# 6. Package Information

**LQFP-48 Outline Dimension**




| SYMBOLS | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | - | - | 1.20 | - | - | 0.047 |
| A1 | 0.05 | - | 0.15 | 0.001 | | 0.005 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.17 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| c | 0.09 | - | 0.16 | 0.004 | - | 0.006 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 7.00 BSC | | | 0.276 BSC | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 7.00 BSC | | | 0.276 BSC | | |
| e | 0.50 BSC | | | 0.020 BSC | | |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| q | $0^o$ | $3.5^o$ | $7^o$ | $0^o$ | $3.5^o$ | $7^o$ |

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