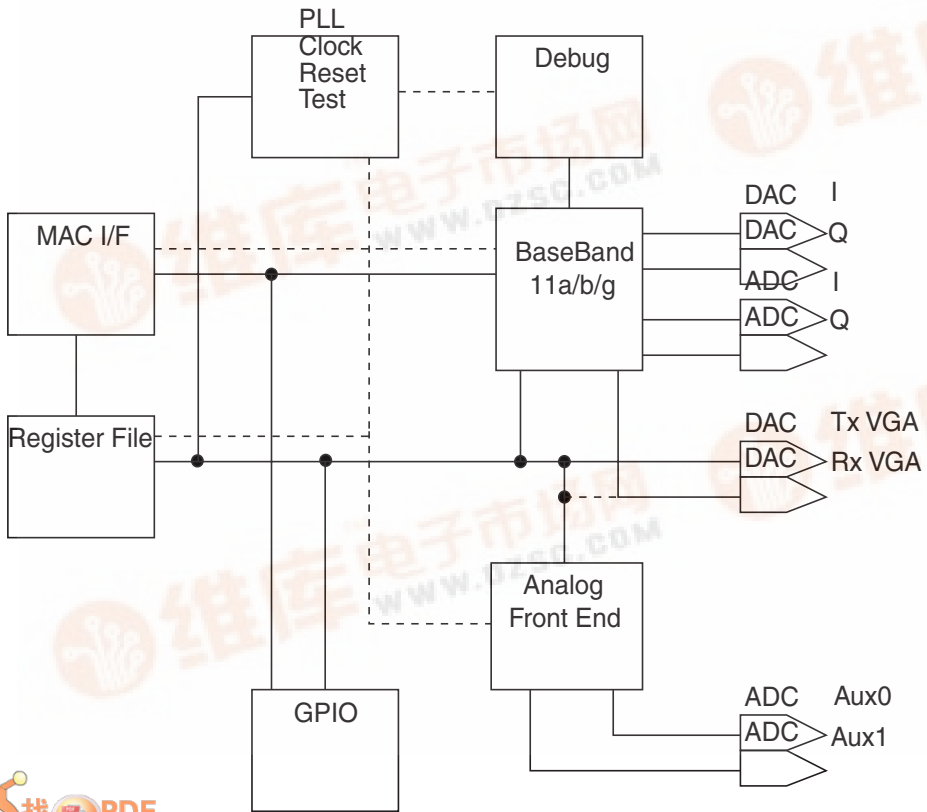
## Features

- On-chip OFDM Baseband Supports All the Transmission Modes of the IEEE 802.11a Specification and the OFDM Modes of the IEEE 802.11g Specification (6, 9, 12, 18, 24, 36, 48, and 54 Mbps)
- On-chip DSSS/CCK Baseband Supports All Transmission Modes of the IEEE 802.11b Specification (1, 2, 5.5, 11 Mbps)
- Single 20 MHz or 40 MHz Input Clock Generates the Internal System Clock and the 44 MHz Clock for the DSSS/CCK Baseband
- Low Pin Count Flexible MAC Layer Interface
- Flexible RF Interface Allows Glueless Communication with Various Dual Mode (802.11a/g) RF Devices
- On-chip Automatic Gain Control
- On-chip DC Offset Remove Mechanism
- Analog and Digital Gain Vector for the RF Transceiver
- SPI Interface for Configuration/Control
- 8 GPIO to Control External 11a/g PAs, On/Off of RF Devices and Antenna Diversity
- Digital or Analog Interface to the RF Devices
- Up to 4 Auxiliary Analog to Digital Converters (Depending On the Package)
- Up to 2 Auxiliary Purpose Digital to Analog Converters
- 1.8 Volt Core Voltage Supply
- 3.3 Volt I/O Voltage Supply
- 100-ball TFBGA Package

## 802.11a/b/g BaseBand Controller




# 802.11a/b/g Baseband Controller

# AT76C517 Summary

**NOTE:** This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office.

5642AS–WLAN–07/06

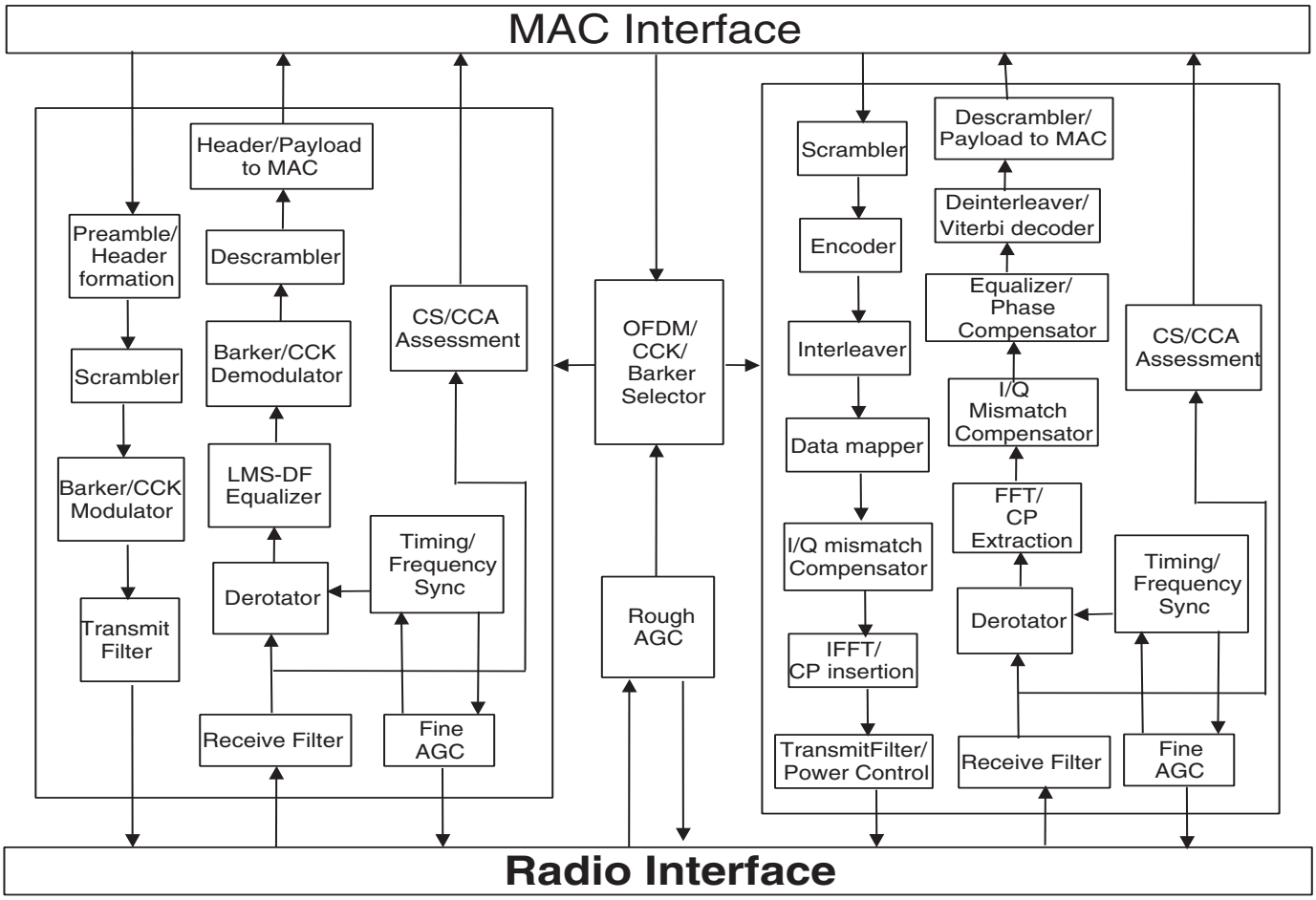
## 1. Description

The AT76C517 provides complete modem functionality for an 802.11a/b/g wireless LAN chip set. It contains signal processing functionality for both DSSS/CCK and OFDM modulation/demodulation. It supports both short and long PLCP preamble formats for 802.11b rates, while it incorporates efficient compensation algorithms for improving the performance of the OFDM modem part.

The AT76C517 provides an interface to a MAC processor consisting of a bi-directional data bus, data synchronization signals and a serial-to-parallel port interface. The AT76C517 can exchange either payload data or TX/RX vector and payload data with the MAC over a bi-directional data bus in a half-duplex fashion using data synchronization signals. The interface allows the baseband and the MAC controllers to operate at different speeds incorporating FIFOs in both directions. The serial-to-parallel port interface provides access to all internal registers and is able to run up to 20 MHz.

The AT76C517 is able to interface with various 802.11a/g radio devices using analog or proprietary digital I/Q interface, analog or digital signals for automatic gain control, gain lock indication, antenna diversity control, LNA “gain on” and various other signals which depict the state of internal critical circuits related to the front-end logic of the modem.

## 2. Functional diagram



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