

## Features

### General

- High-performance, Low-power 32-bit ARM®-SC100™ Enhanced RISC Architecture
- Von Neumann Load / Store Architecture
  - single 32-bit Data Bus for Instructions and Data
- Memory Protection unit
- Internal Oscillator (VFO) (up to 50 MHz)
- ESD Protection to ± 2000V (± 6000V on the ISO interfaces)
- Operating Ranges: 3.3V (+/- 10%)
- Compliant with EMV Level 1, VISA PED, APACS, ZKA, Common Criteria (EAL4+), FINREAD

### Memory

- 256 bits of Key Storage (battery backup)
- 32K Bytes of internal ROM Memory (BOOT, library)
- 256K Bytes of Internal EEPROM, Including 128 OTP Bytes and 384-byte Bit-addressable Bytes
  - 1 to 128-byte Program/Erase
  - 2 ms Program, 2 ms Erase
  - Endurance: 500,000 Write/Erase Cycles at temperature of 25 degrees C
  - 10 Years Data Retention
- 100K Bytes of Internal RAM (4KB Crypto RAM)
- up to 16M Bytes of External Memory (accessed by page)

### Peripherals

- Page Unit to access External Memory Page
- Static Memory Controller
- Two ISO 7816 controllers with DC/DC (one of them can be multiplexed to address 4 SAM)
- USB 2.0 Full Speed (8 endpoints)
- SPI Controller (up to 24 Mbps)
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
- Triple Track Magstripe Logical Interface
- 5 8-bit I/O Port Interface (LEDs, Keyboard, LCD, spare...)
- Real Time Clock (RTC) with Alarm interrupt
- System Timer including a 16-bit Counter, Watchdog and Second Counter
- Six-channel 16-bit Timer/counter
- 2-level, 28-interrupt Controller
- Hardware DES and Triple DES DPA Resistant
- Hardware AES 128-192-256
- Hardware SHA-1, SHA-256
- True Random Number Generator (RNG)
- Two CRC 16 Engines and one CRC 32 Engine (Compliant with ISO/IEC 3309)
- AdvX - Advanced crypto multiplier for cryptography and authentication (including RSA, DSA, Key Generation, ECC)

### Security

- Dedicated Hardware for Protection Against SPA/DPA Attacks
- Advanced Protection Against Physical Attack, Including Active Shield
- Intrusion sensors (mesh and switches).
- Environmental Protection Systems (Voltage, Frequency, UV and Temperature)
- Secure Memory Management/Access Protection (MPU)
- Real time clock and battery back up
- Compliant with EMV standard, VISA PED and FINREAD



## Secure Microcontroller for Electronic Transaction Terminal / Reader

AT91SO100/101

## Summary

6514BS-SMIC-26Oct05



Note: This is a summary document. A complete document will be available under NDA. For more information, please contact your local Atmel sales office.



## Description

**AT91SO100** is a low-power, high-performance, SC100 32-bit microcontroller based on the ARM® enhanced RISC architecture. This new SC100 core allows the linear addressing of up to 1M bytes of code and data as well as a number of new functional and security features. A 3-level instruction pipeline allows the performance of one instruction in a single clock cycle, the AT91SO100 achieves throughputs close to 1 MIPS per MHz. The SC100 processor employs a unique architectural strategy known as Thumb® a super reduced instruction set that is ideally suited for high volume applications with memory restrictions and applications where code density is an important factor.

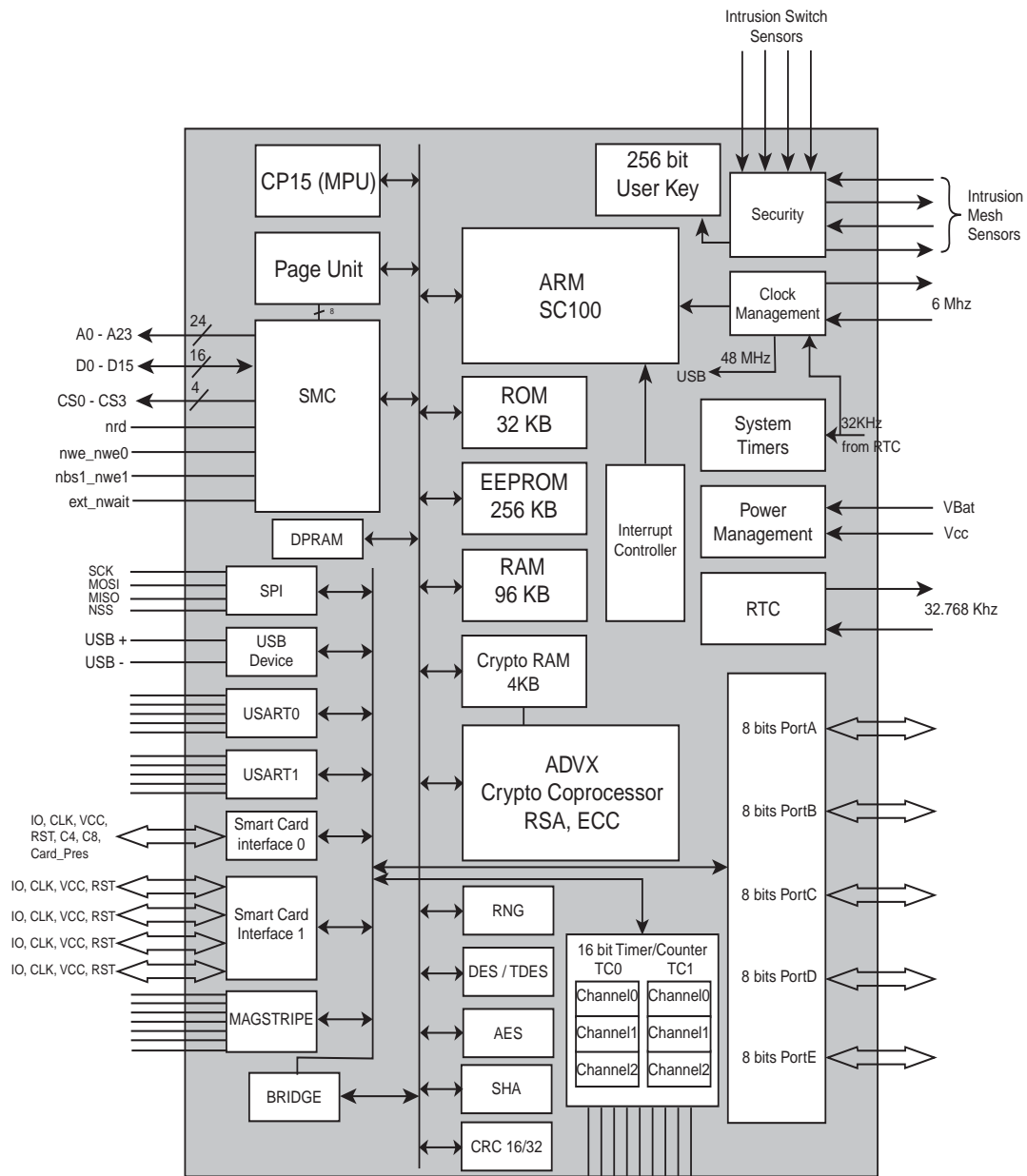
**AT91SO100** has internal EEPROM that can be used as program or data memory. It also includes a ROM (for the boot and some native functions) and a large SRAM. **AT91SO100** can also address, via pages, up to 16Mbytes of external memory.

The **AT91SO100** also comprises of strong security mechanisms and has a impressive set of cryptography features , hardware DES/TDES, hardware AES, hardware SHA-n, hardware cryptography accelerator for asymmetric algorithms (RSA, Elliptic Curve, Key generation) and a true random number generator.

**AT91SO100** includes a lot of dedicated peripherals as smart card and magnetic stripe card interface, as well as USB, SPI, UARTs and I/O ports.

The **AT91SO101** is a single package solution in BGA256 embedding two chips, the **AT91SO100** and the **AT83C26** which physically interface with up to five smart cards.

Figure 1. Block Diagram.





## Atmel Corporation

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 487-2600

## Regional Headquarters

### Europe

Atmel Sarl  
Route des Arsenaux 41  
Case Postale 80  
CH-1705 Fribourg  
Switzerland  
Tel: (41) 26-426-5555  
Fax: (41) 26-426-5500

### Asia

Room 1219  
Chinachem Golden Plaza  
77 Mody Road Tsimshatsui  
East Kowloon  
Hong Kong  
Tel: (852) 2721-9778  
Fax: (852) 2722-1369

### Japan

9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chuo-ku, Tokyo 104-0033  
Japan  
Tel: (81) 3-3523-3551  
Fax: (81) 3-3523-7581

## Atmel Operations

### Memory

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway  
San Jose, CA 95131, USA  
Tel: 1(408) 441-0311  
Fax: 1(408) 436-4314

La Chantrerie  
BP 70602  
44306 Nantes Cedex 3, France  
Tel: (33) 2-40-18-18-18  
Fax: (33) 2-40-18-19-60

### ASIC/ASSP/Smart Cards

Zone Industrielle  
13106 Rousset Cedex, France  
Tel: (33) 4-42-53-60-00  
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park  
Maxwell Building  
East Kilbride G75 0QR, Scotland  
Tel: (44) 1355-803-000  
Fax: (44) 1355-242-743

### RF/Automotive

Theresienstrasse 2  
Postfach 3535  
74025 Heilbronn, Germany  
Tel: (49) 71-31-67-0  
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.  
Colorado Springs, CO 80906, USA  
Tel: 1(719) 576-3300  
Fax: 1(719) 540-1759

### Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine  
BP 123  
38521 Saint-Egreve Cedex, France  
Tel: (33) 4-76-58-30-00  
Fax: (33) 4-76-58-34-80

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## Literature Requests

[www.atmel.com/literature](http://www.atmel.com/literature)

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