AU6395

USB2.0 to SATA Bridge Controller

Technical Reference Manual

AU6395

USB2.0 to SATA Bridge Controller

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Revision History

Date	Revision	Description
Dec 2007	1.00W	Official Release

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1. Introduction

1.1 Description

The AU6395 is a single chip controller designed for bridging USB 2.0 to SATA bus interface. It is used as the primary controller of building an external USB 2.0 hard disk or CD/DVD drives.
To maximize the data throughput and achieve the best compatibility, AU6395 is equipped with Alcor's proprietary automatic speed negotiation (ASN) algorithm. The ASN algorithm allows AU6395 to select optimized operating mode that device can best support a reliable data transfer. The silicon would work with the default device driver from Windows ME, Windows 2000, Windows XP and Mac OS X, however, vendor device driver provided by Alcor Micro would enable the built device working under Windows 98, Windows 2000 (SP1/SP2) and Mac OS 9.

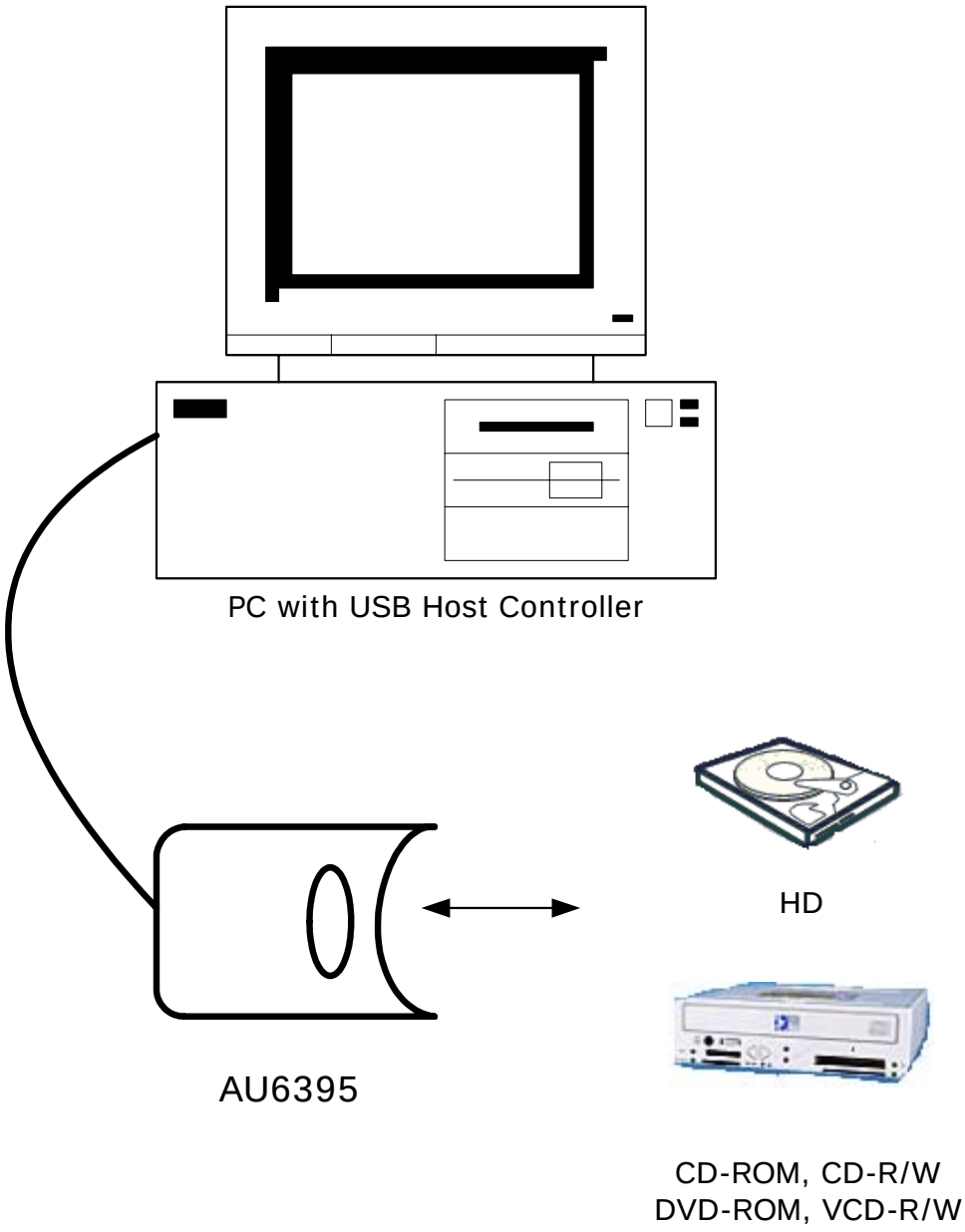
1.2 Features

- Supports USB 2.0 specification and USB Device Class Definition for Mass Storage, Bulk-Transport V1.0.
- Support SATA 1.5G/3.0G Speed Negotiation
- Support SATAII Asynchronous Signal Recovery (Hot Plug) feature.
- Support 480Mbps High Speed (HS) and 12Mbps Full Speed USB operation.
- Supports SATA specification Revision 2.5.
- Support ATA/ATAPI LBA48 bit addressing mode.
- Hardware DMA engine integrated inside for performance enhancement
- Works with default device driver from ME/2000/XP and Mac OS.
- Built in 3.3V to 1.8V Voltage Regulator.
- One spared LED pin for disk access indication
- 64-pin LQFP package
- 48-pin LQFP package

2. Application Block Diagram

The following picture is an application diagram of a typical removable USB2.0 SATA device. With such kinds of devices, users can exchange recorded digital content between SATA device and PC (Notebook) via USB.

Figure 2.1 Block Diagram



3. Pin Assignment

There are two different form factor packages available to choose from. The following figure shows signal names for each pin and the table in the page after describes each pin in details.

Figure 3.1 AU6395-MBLPin Assignment Diagram

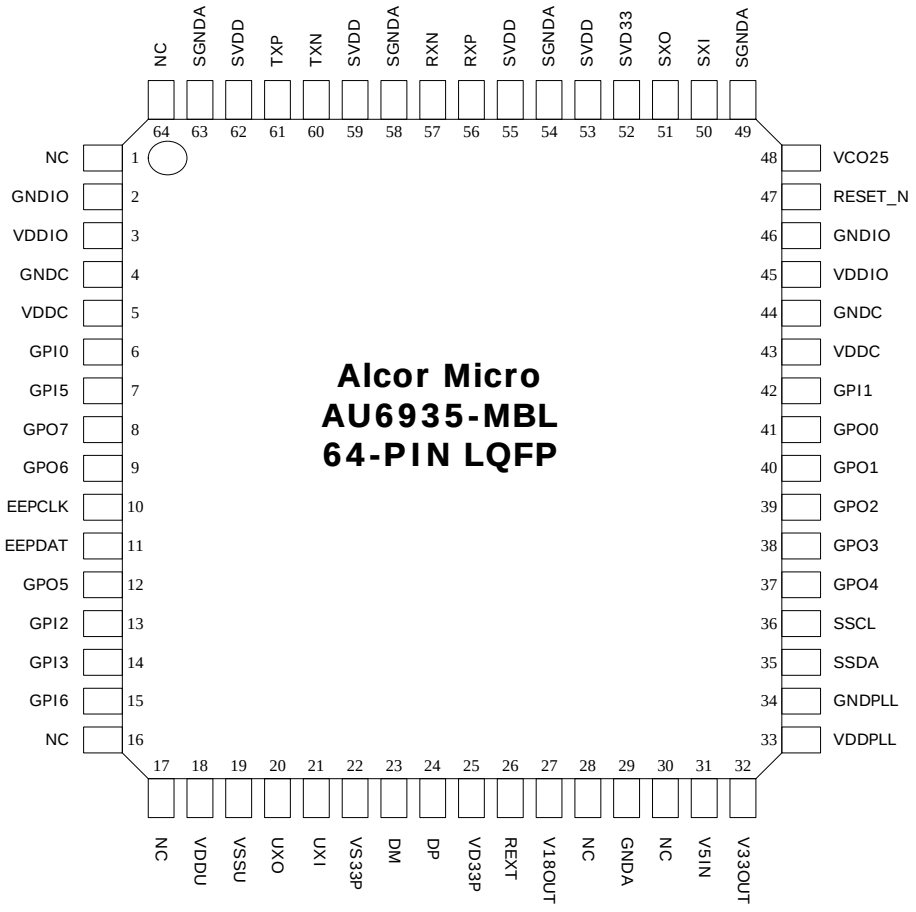


Table 3.1 AU6395-MBL Pin Descriptions

Pin #	Pin Name	I/O	Description
1	NC		
2	GNDIO	PWR	I/O gnd
3	VDDIO	PWR	I/O vdd
4	GNDC	PWR	Core logic gnd
5	VDDC	PWR	Core logic vdd
6	GPI0	I	General purpose input 0
7	GPI5	I	General purpose input 5
8	GPO7	O	General purpose output 7
9	GPO6	O	General purpose output 6
10	EEPCLK	O	EEPROM I2C clock
11	EEPDAT	I/O	EEPROM I2C data
12	GPO5	O	General purpose output 5
13	GPI2	I	General purpose input 2
14	GPI3	I	General purpose input 3
15	GPI6	I	General purpose input 6
16	NC		
17	NC		
18	VDDU	PWR	USB vdd
19	VSSU	PWR	USB gnd
20	UXO	O	USB crystal output
21	UXI	I	USB crystal input
22	VS33P	PWR	USB gnd
23	DM	I/O	USB D-
24	DP	I/O	USB D+
25	VD33P	PWR	USB vdd
26	REXT	I	USB external resistor
27	V18OUT	PWR	Regulator 1.8V output
28	NC		
29	GNDA	PWR	Regulator gnd
30	NC		
31	V5IN	PWR	Regulator 5V input
32	V33OUT	PWR	Regulator 3.3V output
33	VDDPLL	PWR	PLL vdd
34	GNDPLL	PWR	PLL gnd
35	SSDA	I/O	SATA I2C data

Pin #	Pin Name	I/O	Description
36	SSCL	I	SATA I2C clock
37	GPO4	O	General purpose output 4
38	GPO3	O	General purpose output 3
39	GPO2	O	General purpose output 2
40	GPO1	O	General purpose output 1
41	GPO0	O	General purpose output 0
42	GPI1	I	General purpose input 1
43	VDDC	PWR	Core logic vdd
44	GNDC	PWR	Core logic gnd
45	VDDIO	PWR	I/O vdd
46	GNDIO	PWR	I/O gnd
47	RESET_N	I	Chip reset_n
48	VCO25	O	PLL 25 MHz output
49	SGNDA	PWR	
50	SXI	I	SATA crystal input
51	SXO	O	SATA crystal output
52	SVDD33	PWR	SATA vdd
53	SVDD	PWR	SATA vdd
54	SGNDA	PWR	SATA gnd
55	SVDD	PWR	SATA vdd
56	RXP	I	SATA rx+
57	RXN	I	SATA rx-
58	SGNDA	PWR	SATA gnd
59	SVDD	PWR	SATA vdd
60	TXN	O	SATA tx-
61	TXP	O	SATA tx+
62	SVDD	PWR	SATA vdd
63	SGNDA	PWR	SATA gnd
64	NC		

The following figure shows signal names of each pin of the 48 LQFP package and the table in the page after describes each pin in details.

Figure 3.2 AU6395-MCL Pin Assignment Diagram

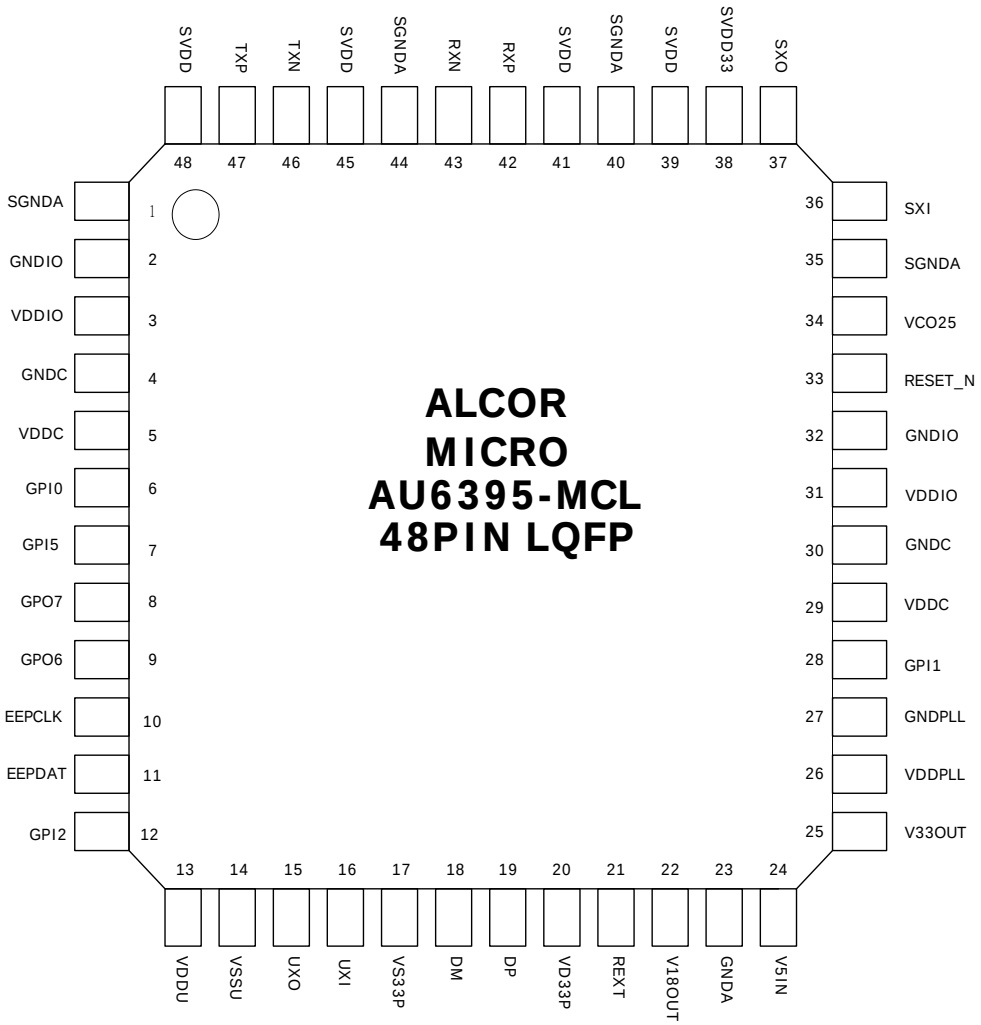


Table 3.2 AU6395-MCL Pin Descriptions

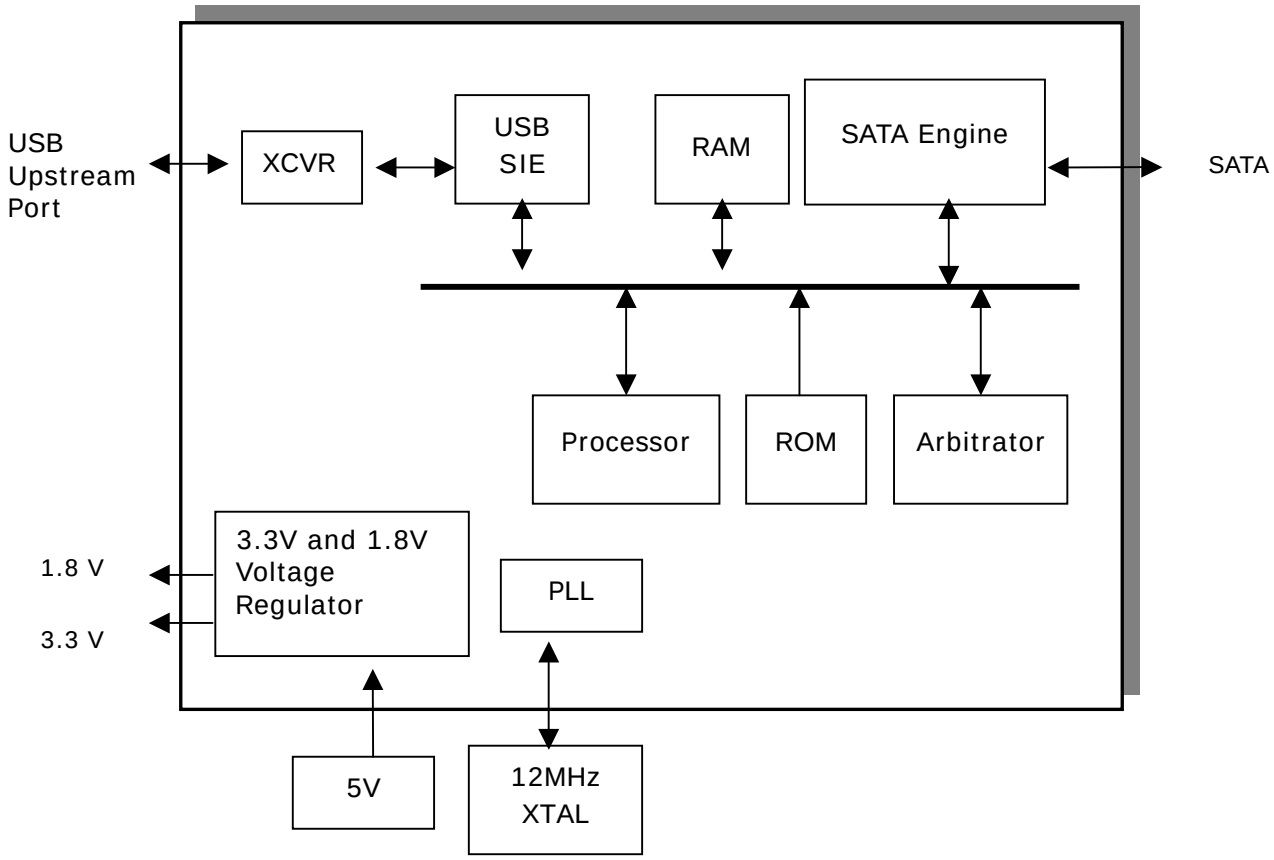
Pin #	Pin Name	I/O	Description
1	SGNDA	PWR	SATA gnd
2	GNDIO	PWR	I/O gnd
3	VDDIO	PWR	I/O vdd
4	GNDC	PWR	Core logic gnd
5	VDDC	PWR	Core logic vdd
6	GPI0	I	General purpose input 0
7	GPI5	I	General purpose input 5
8	GPO7	O	General purpose output 7
9	GPO6	O	General purpose output 6
10	EEPCLK	O	EEPROM I2C clock
11	EEPDAT	I/O	EEPROM I2C data
12	GPI2	I	General purpose input 2
13	VDDU	PWR	USB vdd
14	VSSU	PWR	USB gnd
15	UXO	O	USB crystal output
16	UXI	I	USB crystal input
17	VS33P	PWR	USB gnd
18	DM	I/O	USB D-
19	DP	I/O	USB D+
20	VD33P	PWR	USB vdd
21	REXT	I	USB external resistor
22	V18OUT	PWR	Regulator 1.8V output
23	GNDA	PWR	Regulator gnd
24	V5IN	PWR	Regulator 5V input
25	V33OUT	PWR	Regulator 3.3V output
26	VDDPLL	PWR	PLL vdd
27	GNDPLL	PWR	PLL gnd
28	GPI1	I	General purpose input 1
29	VDDC	PWR	Core logic vdd
30	GNDC	PWR	Core logic gnd
31	VDDIO	PWR	I/O vdd
32	GNDIO	PWR	I/O gnd

Pin #	Pin Name	I/O	Description
33	RESET_N	I	chip reset_n
34	VCO25	O	PLL 25 MHz output
35	SGNDA	PWR	
36	SXI	I	SATA crystal input
37	SXO	O	SATA crystal output
38	SVDD33	PWR	SATA vdd
39	SVDD	PWR	SATA vdd
40	SGNDA	PWR	SATA gnd
41	SVDD	PWR	SATA vdd
42	RXP	I	SATA rx+
43	RXN	I	SATA rx-
44	SGNDA	PWR	SATA gnd
45	SVDD	PWR	SATA vdd
46	TXN	O	SATA tx-
47	TXP	O	SATA tx+
48	SVDD	PWR	SATA vdd

4. System Architecture and Reference Design

4.1 AU6395 Block Diagram

Figure 4.1 AU6395 Block Diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{5IN}	Power Supply	-0.3 to 5.25	V
V_{DDH}	Power Supply	-0.3 to 3.6	V
V_{IN}	Input Signal Voltage	-0.3 to V_{DDH} +0.3	V
T_{STG}	Storage Temperature	-40 to 150	^{O}C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V5IN	Power Supply	4.75	5.0	5.25	V
V_{DDH}	Power Supply	3.0	3.3	3.6	V
V_{DD} V_{18}	Digital Supply	1.62	1.8	1.98	V
V_{IN}	Input Signal Voltage	0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input current	No pull-up or pull-down	-10	±1	10	μA
I_{OZ}	Tri-state leakage current		-10	±1	10	μA
C_{IN}	Input capacitance	Pad Limit		2.8		ρF
C_{OUT}	Output capacitance	Pad Limit		2.8		ρF
C_{BID}	Bi-directional buffer capacitance	Pad Limit		2.8		ρF

5.4 DC Electrical Characteristics of 3.3V I/O Cells

Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

SYMBOL	PARAMETER	CONDITIONS	Limits			UNIT
			MIN	TYP	MAX	
V_{DDHM}	Power supply	3.3V I/O	3.0	3.3	3.6	V
V_{il}	Input low voltage	LVTTL			0.8	V
V_{ih}	Input high voltage		2.0			V
V_{ol}	Output low voltage	$\lvert I_{ol} \rvert$ =2~16mA			0.4	V
V_{oh}	Output high voltage	$\lvert I_{oh} \rvert$ =2~16mA	2.4			V
R_{pu}	Input pull-up resistance	PU=high, PD=low	55	75	110	KΩ
R_{pd}	Input pull-down resistance	PU=low, PD=high	40	75	150	KΩ
I_{in}	Input leakage current	V_{in}= V_{DDHM} or 0	-10	±1	10	μA
I_{oz}	Tri-state output leakage current		-10	±1	10	μA

5.5 USB Transceiver Characteristics

Table 5.5 Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD33	Analog supply Voltage		3.0	3.3	3.6	V
VDD V18	Digital supply Voltage		1.62	1.8	1.98	V
I_{CC}	Operating supply current	High speed operating at 480 MHz			55	mA

Table 5.6 Static characteristic：Digital pin

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input levels						
V_{IL}	Low-level input voltage				0.8	V
V_{IH}	High-level input voltage		2.0			V
Output levels						
V_{OL}	Low-level output voltage				0.2	V
V_{OH}	High-level output voltage		VDDH-0.2			V

Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
USB2.0 Transceiver（HS）						
Input Levels（differential receiver）						
V_{HSDIFF}	High speed differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$ measured at the connection as application circuit	300			mV
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
V_{HSSQ}	High speed squelch detection threshold	Squelch detected			100	mV
		No squelch detected	150			mV
V_{HSDSC}	High speed disconnection detection threshold	Disconnection detected	625			mV
		Disconnection not detected			525	mV
Output Levels						
V_{HSOI}	High speed idle level output voltage(differential)		-10		10	mV
V_{HSOL}	High speed low level output voltage(differential)		-10		10	mV
V_{HSOH}	High speed high level output voltage(differential)		-360		400	mV
V_{CHIRPJ}	Chirp-J output voltage（differential）		700		1100	mV
V_{CHIRPK}	Chirp-K output voltage（differential）		-900		-500	mV
Resistance						
R_{DRV}	Driver output impedance	Equivalent resistance used as internal chip only	3	6	9	Ω

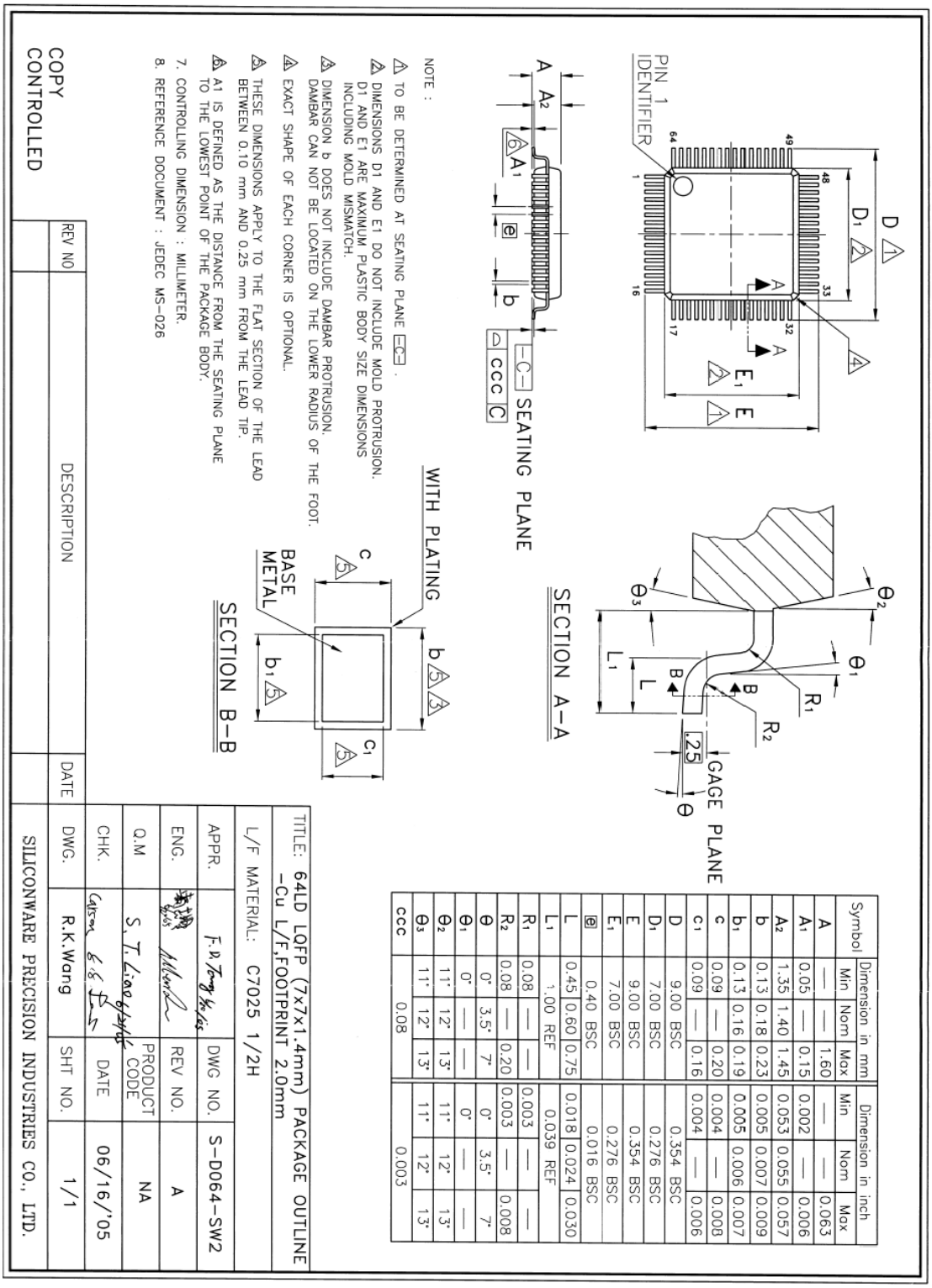
		Overall resistance including external resistor	40.5	45	49.5	
Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU		3.0		3.6	V
USB1.1 Transceiver（FS）						
Input Levels（differential receiver）						
V_{DI}	Differential input sensitivity	$\lvert V_{I(DP)}-V_{I(DM)} \rvert$	0.2			V
V_{CM}	Differential common mode voltage		0.8		2.5	V
Input Levels（single-ended receivers）						
V_{SE}	Single ended receiver threshold		0.8		2.0	V
Output levels						
V_{OL}	Low-level output voltage		0		0.3	V
V_{OH}	High-level output voltage		2.8		3.6	V

Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Driver Characteristics						
High-Speed Mode						
t_{HSR}	High-speed differential rise time		500			ps
t_{HSF}	High-speed differential fall time		500			ps
Full-Speed Mode						
t_{FR}	Rise time	CL=50pF；10 to 90% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FF}	Fall time	CL=50pF；90 to 10% of $\lvert V_{OH}-V_{OL} \rvert$；	4		20	ns
t_{FRMA}	Differential rise/fall time matching（t_{FR} / t_{FF}）	Excluding the first transition from idle mode	90		110	%
V_{CRS}	Output signal crossover voltage	Excluding the first transition from idle mode	1.3		2.0	V

6. Mechanical Information

Figure 6.1 64 LQFP Mechanical Information Diagram



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	9.00 BSC			0.354 BSC		
D_1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E_1	7.00 BSC			0.276 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

TITLE: 64LD LQFP (7x7x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm

L/F MATERIAL: C7025 1/2H

APPR.	F.D.Tong	DWG NO.	S-D064-SW2
ENG.	M.W.Chen	REV NO.	A
Q.M	S.T.Liao	PRODUCT CODE	NA
CHK.	C.S.Chen	DATE	06/16/'05
DWG.	R.K.Wang	SHT NO.	1/1

REV NO	DESCRIPTION	DATE

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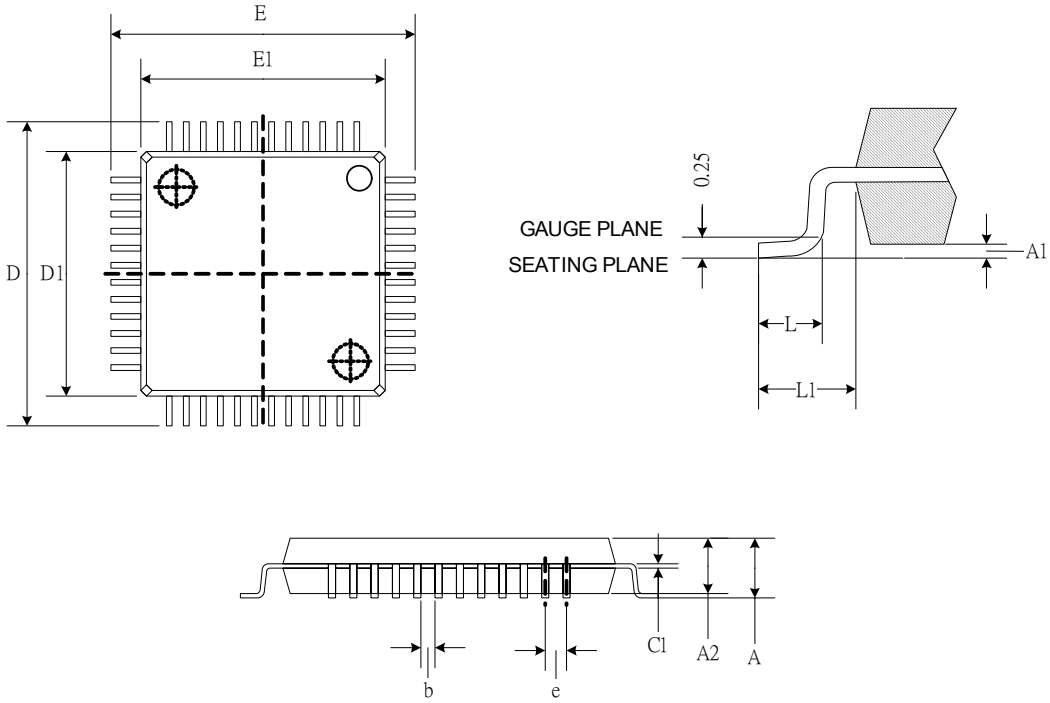
Figure 6.2 48 LQFP Mechanical Information Diagram



SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm

7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

SIE	Serial Interface Engine
SATA	Serial Advanced Technology Attachment
UTMI	USB Transceiver Macrocell Interface

About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.