

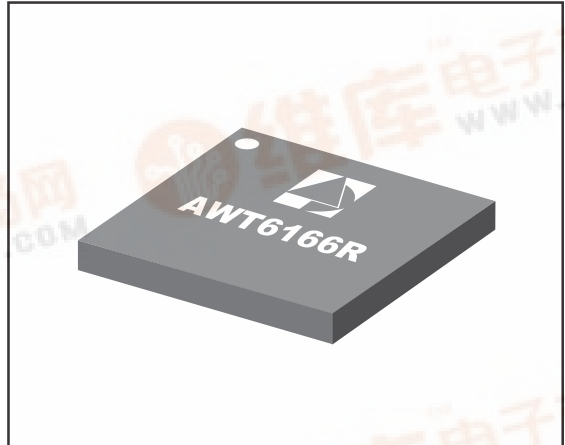


GSM850/GSM900/DCS/PCS Quad Band Power Amplifier Module With Integrated Power Control

Data Sheet - Rev 2.0

FEATURES

- Integrated Vreg (regulated supply)
- Harmonic Performance ≤ -20 dBm
- High Efficiency (PAE) at Pmax:
 - GSM850, 53%
 - GSM900, 55%
 - DCS, 53%
 - PCS, 53%
- +35 dBm GSM850/900 Output Power at 3.5 V
- +33 dBm DCS/PCS Output Power at 3.5 V
- 55 dB Dynamic Range
- GPRS Class 12 Capable
- RoHS Compliant Package, 250°C MSL-3



M15 Package
18 Pin 6 mm x 6 mm x 1.3 mm
Amplifier Module

APPLICATIONS

- Dual/Tri/Quad Band Handsets & PDAs

PRODUCT DESCRIPTION

As with previous generations, the AWT6166R integrated CMOS power control scheme simplifies the design of the transmitter by eliminating the need for external power control circuitry.

reducing the number of external components required in the final application. Both PA die, GSM850/900 and DCS/PCS, are fabricated using state of the art InGaP HBT technology, known for its proven reliability and temperature stability.

The AWT6166R input and output terminals are internal matched to 50 ohms and DC blocked,

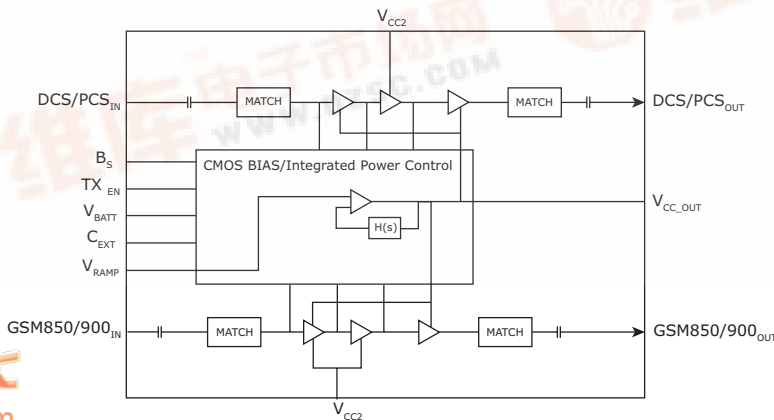


Figure 1: Block Diagram



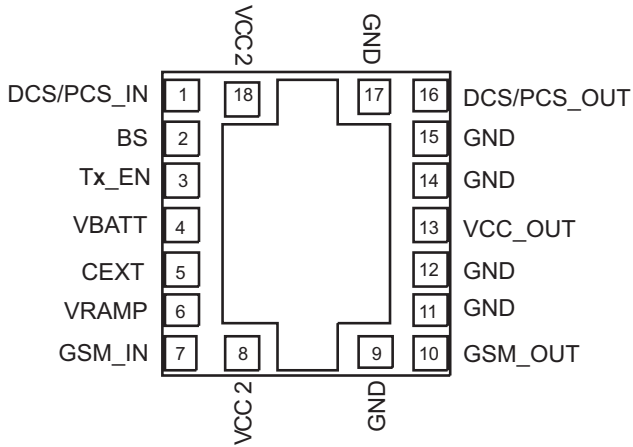


Figure 2: Pinout (X-ray Top View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DCS/PCS_IN	DCS/PCS RF Input	10	GSM_OUT	GSM850/900 RF Output
2	BS	Band Select Logic Input	11	GND	Ground
3	Tx_EN	TX Enable Logic Input	12	GND	Ground
4	V _{BATT}	Battery Supply Connection	13	V _{CC_OUT}	Control Voltage Output which must be connected to V _{CC2}
5	C _{EXT}	Bypass	14	GND	Ground
6	V _{RAMP}	Analog Signal used to control the output power	15	GND	Ground
7	GSM_IN	GSM850/900 RF Input	16	DCS/PCS_OUT	DCS/PCS RF Output
8	V _{CC2}	VCC Control Input for GSM850/900 Pre-amplifier	17	GND	Ground
9	GND	Ground	18	V _{CC2}	Vcc Control Input for DCS/PCS Pre-amplifier

ELECTRICAL CHARACTERISTICS

Table 2: Absolute Minimum and Maximum Ratings

PARAMETER	MIN	MAX	UNIT
Supply Voltage (V_{BATT})	-	+7	V
RF Input Power (RF_{IN})	-	11	dBm
Control Voltages (V_{RAMP})	-0.3	1.8	V
Storage Temperature (T_{STG})	- 55	150	°C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 3: Digital Inputs

PARAMETER	MIN	TYP	MAX	UNIT
Logic High Voltage (V_{IH})	1.2	-	3.0	V
Logic Low Voltage (V_{IL})	-	-	0.5	V
Logic High Current (I_{IH})	-	-	30	μA
Logic Low Current (I_{IL})	-	-	30	μA

Table 4: Control Logic Table

MODE	Tx_EN	BS
PA Enable	HIGH	X
GSM850/900 Mode	HIGH	LOW
DCS/PCS Mode	HIGH	HIGH
PA Disable	LOW	X

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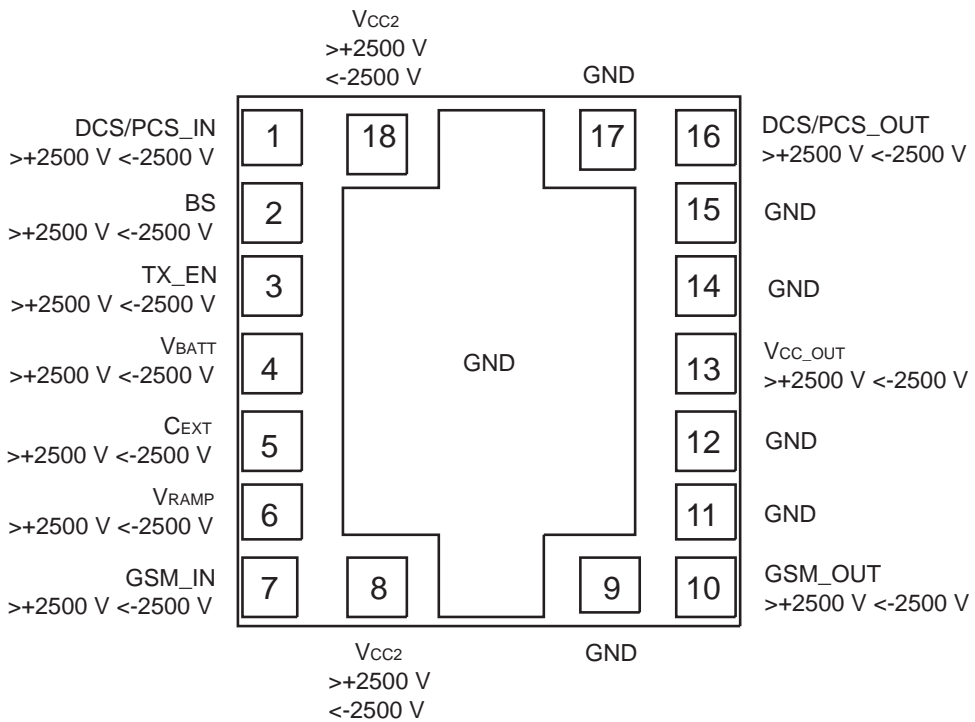


Figure 3: ESD Pin Rating

ELECTROSTATIC DISCHARGE SENSITIVITY

The AWT6166R part was tested to determine the ESD sensitivity of each package pin with respect to ground. All the package pins were subjected to an ESD pulse event using the Human Body Model outlined in MIL-STD-883E Method 3015.7 in either

polarity with respect to ground. The pre and post test I-V characteristics of each pin are recorded. The ratings on each pin require that it sustain the ESD event and show no degradation.

Table 5: Operating Ranges

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Case Temperature (T_C)	-20	-	85	°C	
Supply Voltage (V_{BATT})	3.0	3.5	4.8	V	
Power Supply Leakage Current	-	1	10	μ A	$V_{BATT} = 4.8$ V, $V_{RAMP} = 0$ V, TX_EN = LOW, No RF applied
Control Voltage Range	0.2	-	1.6	V	
Turn on time (T_{ON})	-	-	1	μ s	$V_{RAMP} = 0.2$ V, TX_EN = LOW \rightarrow High $P_{IN} = 5$ dBm
Turn off time (T_{OFF})	-	-	1	μ s	$V_{RAMP} = 0.2$ V, TX_EN = HIGH \rightarrow LOW $P_{IN} = 5$ dBm
Rise Time (T_{RISE})	-	-	1	μ s	$P_{OUT} = -10$ dBm $\rightarrow P_{MAX}$ (within 0.2 dB)
Fall Time (T_{FALL})	-	-	1	μ s	$P_{OUT} = P_{MAX} \rightarrow -10$ dBm (within 0.2 dB)
V_{RAMP} Input Capacitance	-	3	-	pF	
V_{RAMP} Input Current	-	-	10	μ A	
Duty Cycle	-	-	50	%	

The device may be operated safely over these conditions; however, parametric performance is guaranteed only over the conditions defined in the electrical specifications.

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Table 6: Electrical Characteristics for GSM850

Unless otherwise stated ($V_{BATT} = 3.5\text{ V}$, $P_{IN} = 3.0\text{ dBm}$, Pulse Width = 1154 μs , Duty 25%,
 $Z_{IN} = Z_{OUT} = 50\ \Omega$, $T_C = 25\ ^\circ\text{C}$, $V_{RAMP} = 1.6\text{ V}$, BS = LOW, TX_EN = HIGH)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F _o)	824	-	849	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P _{MAX}	34.5	35.0	-	dBm	Freq = 824 to 849 MHz
Degraded Output Power	32.5	33.5	-	dBm	$V_{BATT} = 3.0\text{ V}$, $T_C = 85\ ^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$
PAE @ P _{MAX}	48	53	-	%	Freq = 824 to 849 MHz
Forward Isolation 1	-	-40	-35	dBm	TX_EN = LOW, $V_{RAMP} = 0.2\text{ V}$ $P_{IN} = 5\text{ dBm}$
Forward Isolation 2	-	-25	-20	dBm	TX_EN = HIGH, $V_{RAMP} = 0.2\text{ V}$, $P_{IN} = 5\text{ dBm}$
Cross Isolation (Coupling of GSM 2fo and 3fo to DCS/PCS port)	-	-26	-18	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Harmonics 2fo, 3fo $n \cdot F_o$, ($n \geq 4$), $F_o \leq 12.75\text{ GHz}$	-	-27	-10	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Stability	VSWR = 8:1 All Phases, $P_{OUT} \leq 34.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$
Ruggedness	-	-	10:1	VSWR	All load phases, $P_{OUT} \leq 34.5\text{ dBm}$
RX Noise Power	-	-87	-83	dBm	$F_{TX} = 849\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 869\text{ to }894\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
Input VSWR	-	1.5:1	2.5:1	-	$P_{OUT} \leq 34.5\text{ dBm}$

Table 7: Electrical Characteristics for GSM900

Unless otherwise stated ($V_{BATT} = 3.5\text{ V}$, $P_{IN} = 3.0\text{ dBm}$, Pulse Width = 1154 μs , Duty 25%,
 $Z_{IN} = Z_{OUT} = 50\ \Omega$, $T_C = 25\ ^\circ\text{C}$, $V_{RAMP} = 1.6\text{ V}$, BS = LOW, TX_EN = HIGH)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency (F_o)	880	-	915	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P_{MAX}	34.5	35.0	-	dBm	Freq = 880 to 915 MHz
Degraded Output Power	32.5	33.5	-	dBm	$V_{BATT} = 3.0\text{ V}$, $T_C = 85\ ^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	50	55	-	%	Freq = 880 to 915MHz
Forward Isolation 1	-	-38	-33	dBm	TX_EN = LOW, $V_{RAMP} = 0.2\text{ V}$ $P_{IN} = 5\text{ dBm}$
Forward Isolation 2	-	-25	-20	dBm	TX_EN = HIGH, $V_{RAMP} = 0.2\text{ V}$, $P_{IN} = 5\text{ dBm}$
Cross Isolation (Coupling of GSM 2fo and 3fo to DCS/PCS port)	-	-23	-17	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Harmonics 2fo, 3fo $n \cdot F_o$, ($n \geq 4$), $F_o \leq 12.75\text{ GHz}$	- -	-22 -30	-10 -10	dBm	$P_{OUT} \leq 34.5\text{ dBm}$
Stability	VSWR = 8:1 All Phases, $P_{OUT} \leq 34.5\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$
Ruggedness	-	-	10:1	VSWR	All load phases, $P_{OUT} \leq 34.5\text{ dBm}$
RX Noise Power	-	-84	-77	dBm	$F_{TX} = 915\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 925\text{ to }935\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
	-	-87	-83	dBm	$F_{TX} = 915\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 935\text{ to }960\text{ MHz}$, $P_{OUT} \leq 34.5\text{ dBm}$
Input VSWR	-	1.5:1	2.5:1	-	$P_{OUT} \leq 34.5\text{ dBm}$

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Table 8: Electrical Characteristics for DCS

Unless otherwise stated ($V_{BATT} = 3.5\text{ V}$, $P_{IN} = 3.0\text{ dBm}$, Pulse Width = 1154 μs , Duty 25%,
 $Z_{IN} = Z_{OUT} = 50\ \Omega$, $T_C = 25\ ^\circ\text{C}$, $V_{RAMP} = 1.6\text{ V}$, BS = HIGH, TX_EN = HIGH)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1710	-	1785	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	30	31	-	dBm	$V_{BATT} = 3.0\text{ V}$, $T_C = 85\ ^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	45	53	-	%	Freq = 1710 to 1785 MHz
Forward Isolation 1	-	-40	-35	dBm	TX_EN = LOW, $V_{RAMP} = 0.2\text{ V}$ $P_{IN} = 5\text{ dBm}$
Forward Isolation 2	-	-22	-17	dBm	TX_EN = HIGH, $V_{RAMP} = 0.2\text{ V}$, $P_{IN} = 5\text{ dBm}$
Harmonics 2 F_o , 3 F_o n* F_o , (n \geq 4), $F_o \leq 12.75\text{ GHz}$	- -	-22 -20	-10 -8	dBm	$P_{OUT} \leq 32\text{ dBm}$
Stability	VSWR = 8:1 All Phases, $P_{OUT} \leq 32\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$
Ruggedness	-	-	10:1	VSWR	All load phases, $P_{OUT} \leq 32\text{ dBm}$
RX Noise Power	-	-86	-80	dBm	$F_{TX} = 1785\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 1805\text{ to }1880\text{ MHz}$, $P_{OUT} \leq 32\text{ dBm}$
Input VSWR	-	1.5:1	2.5:1		$P_{OUT} \leq 32\text{ dBm}$

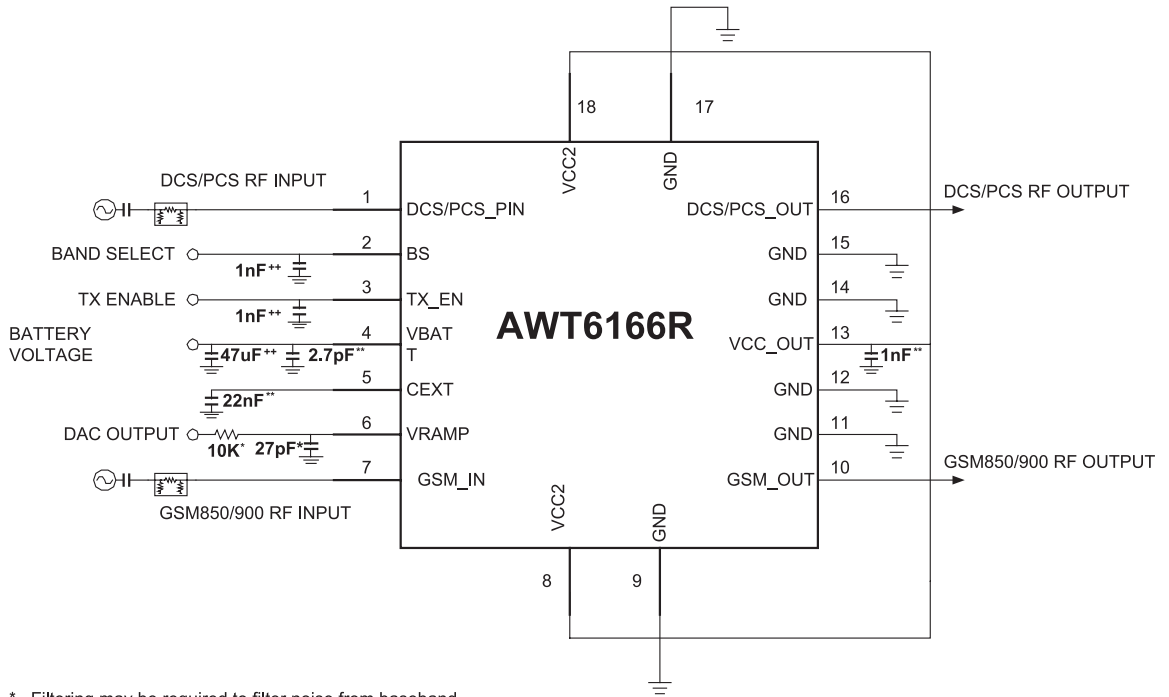
Table 9: Electrical Characteristics for PCS

Unless otherwise stated ($V_{BATT} = 3.5\text{ V}$, $P_{IN} = 3.0\text{ dBm}$, Pulse Width = 1154 μs , Duty 25%,
 $Z_{IN} = Z_{OUT} = 50\ \Omega$, $T_C = 25\ ^\circ\text{C}$, $V_{RAMP} = 1.6\text{ V}$, BS = HIGH, TX_EN = HIGH)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Operating Frequency	1850	-	1910	MHz	
Input Power	0	3.0	5	dBm	
Output Power, P_{MAX}	32	33	-	dBm	
Degraded Output Power	30	31	-	dBm	$V_{BATT} = 3.0\text{ V}$, $T_C = 85\ ^\circ\text{C}$, $P_{IN} = 0\text{ dBm}$
PAE @ P_{MAX}	45	53	-	%	Freq = 1850 to 1910 MHz
Forward Isolation 1	-	-40	-33	dBm	TX_EN = LOW, $V_{RAMP} = 0.2\text{ V}$ $P_{IN} = 5\text{ dBm}$
Forward Isolation 2	-	-22	-17	dBm	TX_EN = HIGH, $V_{RAMP} = 0.2\text{ V}$, $P_{IN} = 5\text{ dBm}$
Harmonics 2 F_o , 3 F_o n* F_o , (n \geq 4), $F_o \leq 12.75\text{ GHz}$	- - -	-25 -20	-10 -5	dBm	$P_{OUT} \leq 32\text{ dBm}$
Stability	VSWR = 8:1 All Phases, $P_{OUT} \leq 32\text{ dBm}$				
	-	-	-36	dBm	$F_{OUT} < 1\text{ GHz}$
	-	-	-30	dBm	$F_{OUT} > 1\text{ GHz}$
Ruggedness	-	-	10:1	VSWR	All load phases, $P_{OUT} \leq 32\text{ dBm}$
RX Noise Power	-	-86	-80	dBm	$F_{TX} = 1910\text{ MHz}$, RBW = 100 kHz, $F_{RX} = 1930\text{ to }1990\text{ MHz}$, $P_{OUT} \leq 32\text{ dBm}$
Input VSWR	-	1.5:1	2.5:1		$P_{OUT} \leq 32\text{ dBm}$

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APPLICATION INFORMATION



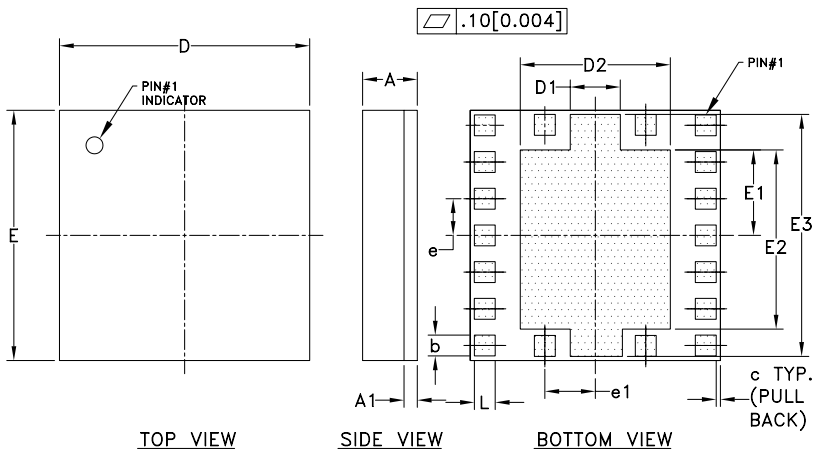
* Filtering may be required to filter noise from baseband.

** This component should be placed as close to the device pin as possible.

++ These components are recommended as good design practice for improving noise rejection characteristics. The values specified are not critical as they may not be required in the final application.

Figure 4: Application Schematic

PACKAGE OUTLINE



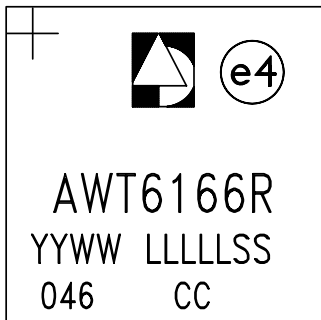
DIM.	MILLIMETERS			INCHES			NOTE
	MIN.	NO.M.	MAX.	MIN.	NO.M.	MAX.	
A	1.16	1.31	1.46	0.045	0.051	0.057	-
A1	0.25	0.30	0.38	0.010	0.012	0.015	-
b	0.47	-	0.53	0.019	-	0.021	-
c	-	0.10	-	-	0.004	-	-
D	5.88	6.00	6.12	0.231	0.236	0.240	-
D1	1.13	-	1.25	0.044	-	0.049	-
D2	3.52	-	3.64	0.139	-	0.143	-
E	5.88	6.00	6.12	0.231	0.236	0.240	-
E1	2.02	-	2.08	0.080	-	0.082	-
E2	4.24	-	4.36	0.167	-	0.172	-
E3	5.72	-	5.84	0.225	-	0.230	-
e	-	0.89	-	-	0.035	-	-
e1	-	1.22	-	-	0.048	-	-
L	0.47	-	0.53	0.019	-	0.021	-

NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.

Figure 5: M15 Package Outline - 18 Pin 6 mm x 6 mm x 1.3 mm Amplifier Module

TOP BRAND



NOTES:

1. ANADIGICS LOGO SIZE: X=0.080±0.010 Y=0.095±0.010
2. PART # AWT6166R
3. YEAR AND WORK WEEK: YYWW: YY = YEAR, WW = WORK WEEK
4. LOT - WAFER I.D.: LLLLL = LOT#(USE U3 LOT#), SS = WAFER I.D.
5. PIN 1 INDICATOR: LASER MARK
6. BOM # 046
7. COUNTRY CODE: CC = TH -for- THAILAND, TW -for- TAIWAN, PH -for- PHILIPPINES, CH -for- CHINA, ID -for- INDONESIA, HK -for- HONG KONG
8. TYPE : ELITE
SIZE : AS LARGE AS POSSIBLE

Figure 6: Branding Specification

AWT6166R

ORDERING INFORMATION

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE DESCRIPTION	COMPONENT PACKAGING
AWT6166RM15P8	-20 °C to +85 °C	RoHS Compliant 18 Pin 6 mm x 6 mm x 1.3 mm	Tape and Reel, 2500 per reel



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