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USB to Fast Ethernet/HomePNA Controller

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Features

- Single chip USB to 10/100Mbps Fast Ethernet and 1/10Mbps HomePNA and HomePlug Network Controller
- Compliant with USB specification 1.0 and 1.1 and 2.0
- Full/High Speed USB Device with bus power capability
- Support 4 endpoints on USB
- IEEE 802.3u 100BASE-T, TX, and T4 Compatible
- Embedded 7K*16 bit SRAM, 256*16 bit SRAM and 8 FIFOs
- Support both full-duplex or half-duplex operation on Fast Ethernet
- Provides a MII port for both Ethernet and HomePNA/ HomePlug PHY interface
- Supports suspended mode and remote wakeup (link_up or magic packet or external pin)
- Optional PHY power down mode for power saving
- Support (94c56/93c66) 256/512 bytes serial EEPROM (used for saving USB Descriptors)
- Support automatic loading of Ethernet ID, USB Descriptors and Adapter Configuration from EEPROM on power-on initialization
- External PHY loop-back diagnostic capability
- Small form factor with 80-pin LQFP package
- Single 12MHz clock input, pure 3.3V operation

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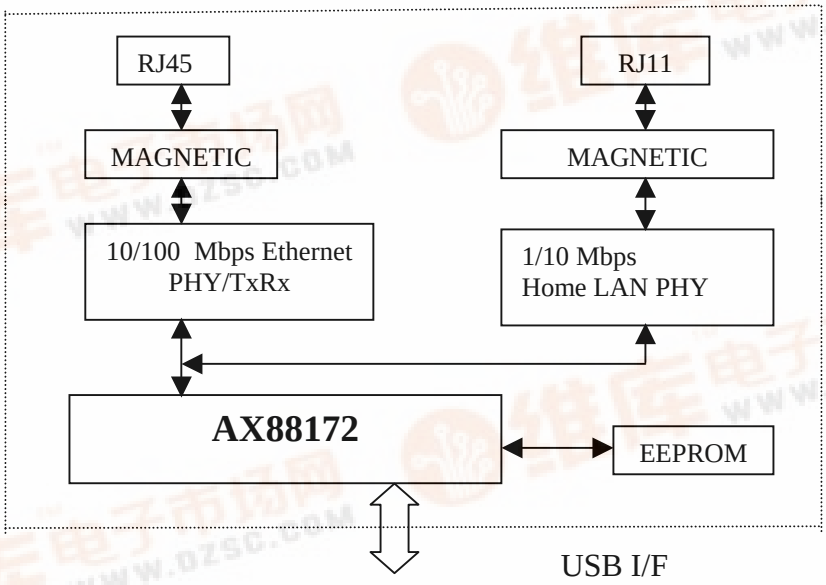
Product description

The AX88172 USB to Fast Ethernet/HomePNA/HomePlug Controller is a high performance and highly integrated Controller with embedded 7K*16 bit SRAM. The AX88172 contains a USB interface to host CPU and compliant with USB Standard V1.0, V1.1 and V2.0. The AX88172 could be used for both 10M/100Mbps Fast Ethernet function based on IEEE802.3 / IEEE802.3u LAN standard and 1M/10M HomePNA standard. The AX88172 supports media-independent interface (MII) to simplify the design on implementing Fast Ethernet and HomePNA functions.

System Block Diagram



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1.0 Introduction

1.1 General Description:

The AX88172 USB to Fast Ethernet Controller is a high performance and highly integrated USB bus Ethernet Controller with embedded 7K*16 bit SRAM. The AX88172 supported Full/High Speed USB Device with bus power capability. The AX88172 implements both 10Mbps and 100Mbps Ethernet function based on IEEE802.3/ IEEE802.3u LAN standard. The AX88172 supports media-independent interface (MII) to simplify the design on implementing Fast Ethernet and HomePNA functions.

AX88172 uses 80-pin LQFP low profile package, 12MHz operation for USB and 25MHz operation for Ethernet, CMOS process with pure 3.3V operation.

1.2 AX88172 Block Diagram:

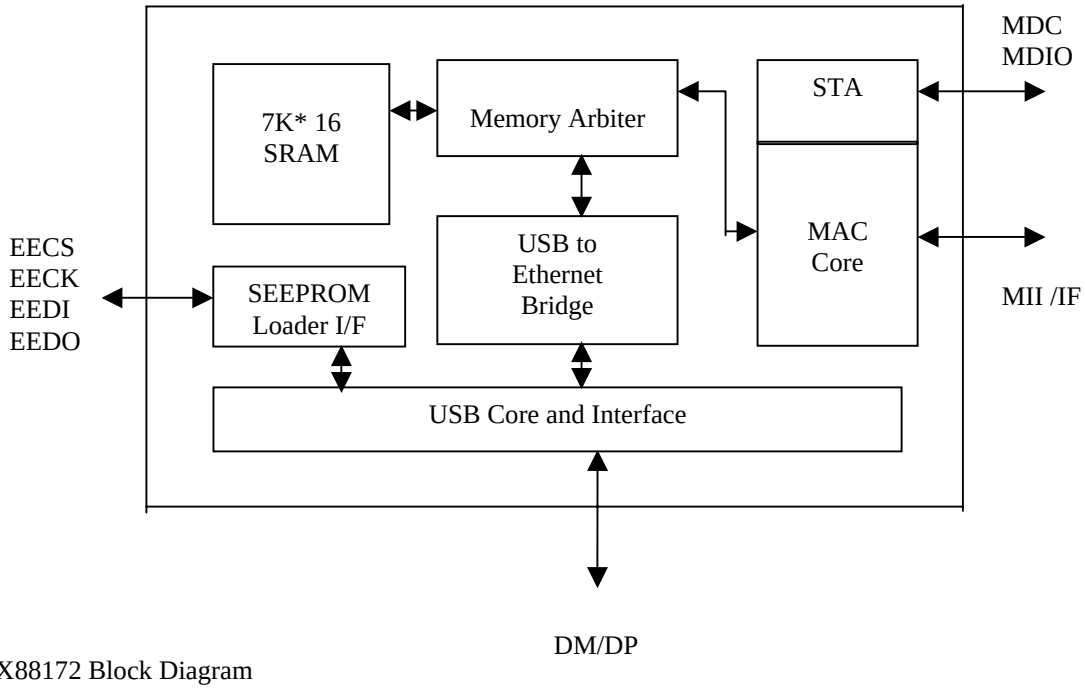


Fig – 1 AX88172 Block Diagram

1.3 AX88172 Pin Connection Diagram

The AX88172 is housed in the 80-pin plastic light quad flat pack.

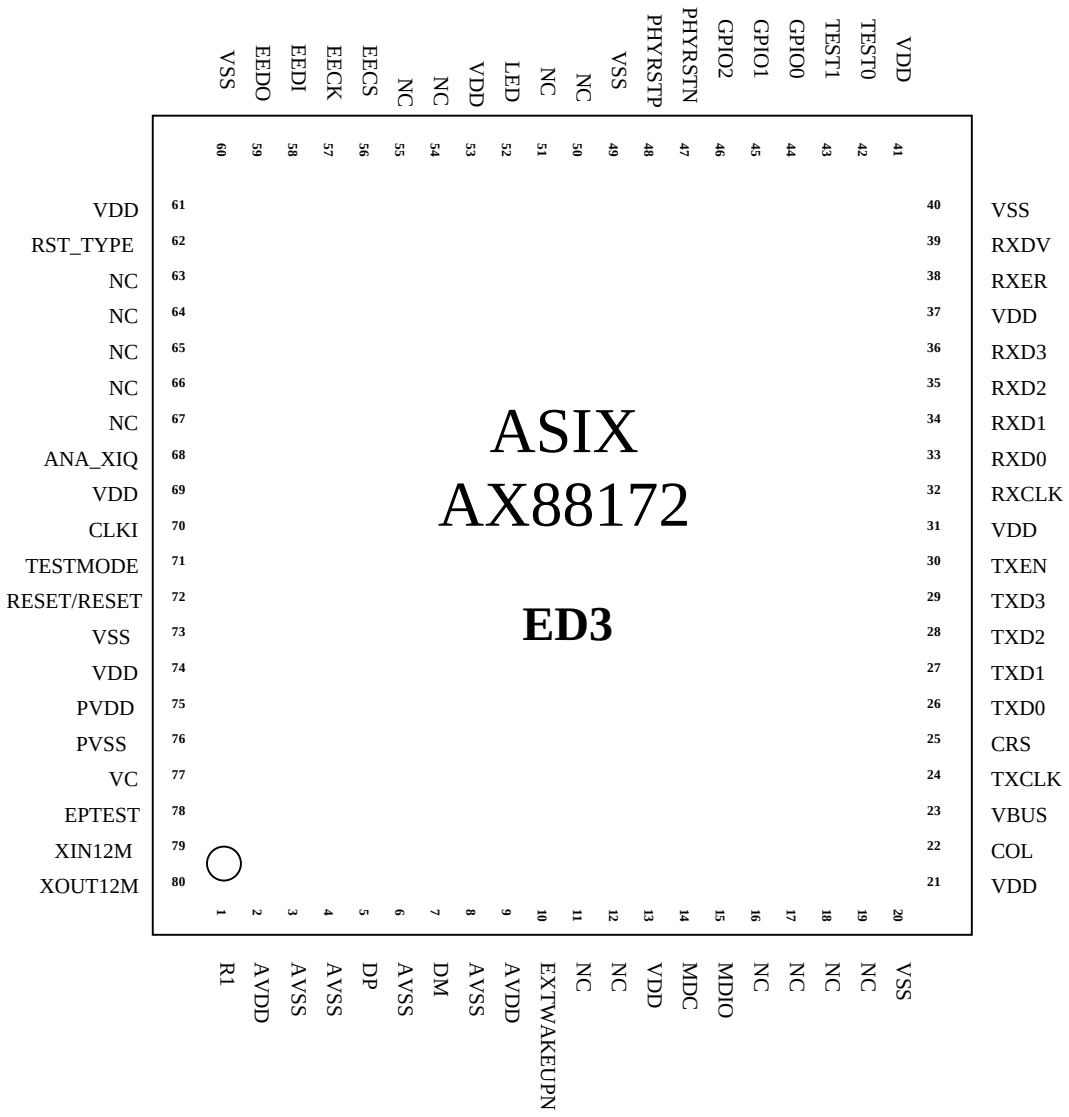


Fig – 2 AX88172 Pin Connection Diagram

2.0 Signal Description

The following terms describe the AX88172 pin-out:
All pin names with the "/" suffix are asserted low.
The following abbreviations are used in following Tables.

I	**Input**	**PU**	**Internal Pull Up (100K)**
O	**Output**	**PD**	**Internal Pull Down (100K)**
I/O	**Input/Output**	**P**	**Power Pin**
OD	**Open Drain**		

SIGNAL	TYPE	PIN NO.	DESCRIPTION
R1	I	1	Constant-votage pin A 6.2K± 1% resistors is connected to AVSS. Be sure to make the line between R1 and each resistor as short as possible.
AVDD	P	2	Power supply pin for analog circuits +3.3V DC
AVSS	P	3	Power supply pin for analog circuits Ground
AVSS	P	4	Power supply pin for analog circuits Ground
DP	B	5	USB data line Data+
AVSS	P	6	Power supply pin for analog circuits Ground
DM	B	7	USB data line Data-
AVSS	P	8	Power supply pin for analog circuits Ground
AVDD	P	9	Power supply pin for analog circuits +3.3V DC
/EXTWAKEUP	I/PU	10	Remote-wakeup trigger from external pin. It active low and should be keep low over 2 clocks (12MHz)
NC	B	11	For testing
NC	B	12	For testing
VDD	P	13	Power Supply for logic circuits: +3.3V DC.
MDC	O	14	Station Management Data Clock: The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock. MDC is a 2.5MHz frequency clock output.
MDIO	I/O/PU	15	Station Management Data Input/Output: Serial data input/output transfers from/to the PHYs. The transfer protocol conforms to the IEEE 802.3u MII specification.
NC	O	16	For testing
NC	O	17	For testing
NC	O	18	For testing
NC	O	19	For testing
VSS	P	20	Power Supply: +0V DC or Ground Power.
VDD	P	21	Power Supply for logic circuits: +3.3V DC.
COL	I	22	Collision: this signal is driven by PHY when collision is detected.
NC		23	No connection
TX_CLK	I	24	Transmit Clock: TX_CLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TX_EN and TXD[3:0] signals from the MII port to the PHY.
CRS	I	25	Carrier Sense: Asynchronous signal CRS is asserted by the PHY when either the transmit or receive medium is non-idle.
TXD[3:0]	O	29, 28, 27, 26	Transmit Data: TXD[3:0] is transition synchronously with respect to the rising edge of TX_CLK. For each TX_CLK period in which TX_EN is asserted, TXD[3:0] are accepted for transmission by the PHY.

TX_EN	O	30	Transmit Enable: TX_EN is transition synchronously with respect to the rising edge of TX_CLK. TX_EN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
VDD	P	31	Power Supply for logic circuits: +3.3V DC.
RX_CLK	I	32	Receive Clock: RX_CLK is a continuous clock that provides the timing reference for the transfer of the RX_DV, RXD[3:0] and RX_ER signals from the PHY to the MII port of the MAC.
RXD[3:0]	I	36, 35, 34, 33	Receive Data: RXD[3:0] is driven by the PHY synchronously with respect to RX_CLK.
VDD	P	37	Power Supply for logic circuits: +3.3V DC.
RX_ER	I	38	Receive Error: RX_ER is driven by PHY and synchronous to RX_CLK, is asserted for one or more RX_CLK periods to indicate to the port that an error has detected.
RX_DV	I	39	Receive Data Valid: RX_DV is driven by the PHY synchronously with respect to RX_CLK. Asserted high when valid data is present on RXD [3:0].
VSS	P	40	Power Supply: +0V DC or Ground Power.
VDD	P	41	Power Supply for logic circuits: +3.3V DC.
TEST0	I/PU	42	Test Pin: This pin for test purpose only. Pull up the pin or keep no connection for normal operation.
TEST1	I/PU	43	Test Pin: This pin for test purpose only. Pull up the pin or keep no connection for normal operation.
GPIO[2:0]	I/O/PU	46, 45, 44	General Purpose Input/ Output Pins.
/PHYRST	O	47	Output for reset PHY active low
PHYRST	O	48	Output for reset PHY active high
VSS	P	49	Power Supply: +0V DC or Ground Power.
NC	I/PD	50	For testing
NC	I/PD	51	For testing
LED	O	52	LED indicator: When link FS, drives logic high always. When link HS, the pin drives logic low. and it will drives high/low a period when line has activity (data transfer).
VDD	P	53	Power Supply for logic circuits: +3.3V DC.
NC	I/PD	54	For testing
NC	ID	55	For testing
EECS	O	56	EEPROM Chip Select: EEPROM chip select signal.
EECK	O	57	EEPROM Clock: Signal connected to EEPROM clock pin.
EEDI	O	58	EEPROM Data In: Signal connected to EEPROM data input pin.
EEDO	I/PD	59	EEPROM Data Out: Signal connected to EEPROM data output pin.
VSS	P	60	Power Supply: +0V DC or Ground Power.
VDD	P	61	Power Supply for logic circuits: +3.3V DC.
RST_TYPE	I/PU	62	This pin define the assert level of Reset (pin 72) When =’1’ or NC, reset signal is active High When =’0’, reset signal is active Low
NC	I/PD	63, 64, 65, 66, 67	For testing
ANA_XIQ	I	68	Sets the IQ mode This pin is used during testing. It must be set to low in IQ measurement mode. 0: IQ mode 1: Normal operation mode
VDD	P	69	Power Supply for logic circuits: +3.3V DC.
CLKI	I/PD	70	External 60MHz input
TESTMODE	I/PD	71	For testing (TESTMODE) 0: Normal operation mode 1: External clock Synchronization mode

RESET/RESET	I	72	Reset/Reset Reset is active high/low depend on RST_TYPE (pin 62) definition. When assert, place AX88172 into reset mode immediately. Reset complete loads the EEPROM data.
VSS	P	73	Power Supply: +0V DC or Ground Power.
VDD	P	74	Power Supply for logic circuits: +3.3V DC.
PVDD	P	75	Power supply pin for PLL and oscillator circuits +3.3V DC
PVSS	P	76	Power supply pin for PLL and oscillator circuits +0V DC or Ground Powe
VC	I	77	Monitor pin for two PLL charge pumps Connect to GND on PCB when actually using
PTEST	I	78	Charge pump monitor ON/OFF: Connect to GND on PCB when actually using
XIN12M	I	79	12M crystal oscillator input
XOUT12M	O	80	12M crystal oscillator output

Tab - 1 PIN signals

3.0 EEPROM Memory Mapping

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00H	RESERVED	WORD COUNT FOR PRELOAD
01H	*FLAG	
02H	HIGH-SPEED LENGTH OF DEVICE DESCRIPTOR (BYTE)	HIGH-SPEED EEPROM OFFSET OF DEVICE DESCRIPTOR
03H	HIGH-SPEED LENGTH OF CONFIGURATION DESCRIPTOR (BYTE)	HIGH-SPEED EEPROM OFFSET OF CONFIGURATION DESCRIPTOR
04H	NODE ID 1	NODE ID 0
05H	NODE ID 3	NODE ID 2
06H	NODE ID 5	NODE ID 4
07H	LANGUAGE ID HIGH BYTE	LANGUAGE ID LOW BYTE
08H	LENGTH OF STRING INDEX 1	EEPROM OFFSET OF STRING INDEX 1
09H	LENGTH OF STRING INDEX 2	EEPROM OFFSET OF STRING INDEX 2
0AH	LENGTH OF STRING INDEX 3	EEPROM OFFSET OF STRING INDEX 3
0BH	LENGTH OF STRING INDEX 4	EEPROM OFFSET OF STRING INDEX 4
0CH	LENGTH OF STRING INDEX 5	EEPROM OFFSET OF STRING INDEX 5
0DH	LENGTH OF STRING INDEX 6	EEPROM OFFSET OF STRING INDEX 6
0EH	LENGTH OF STRING INDEX 7	EEPROM OFFSET OF STRING INDEX 7
0FH	RESERVED	RESERVED
10H	MAX PACKETSIZE HIGH BYTE	MAX PACKET LOW BYTE
11H	**(PHY TYPE[7:5]) (SECONDARY PHY ID[4:0])	**(PHY TYPE[7:5])(FIRST PHY ID[4:0])
12H	PAUSE PACKET HIGH WATER LEVEL	PAUSE PACKET LOW WATER LEVEL
13H	FULL-SPEED LENGTH OF DEVICE DESCRIPTOR (BYTE)	FULL-SPEED EEPROM OFFSET OF DEVICE DESCRIPTOR
14H	FULL-SPEED LENGTH OF CONFIGURATION DESCRIPTOR (BYTE)	FULL-SPEED EEPROM OFFSET OF CONFIGURATION DESCRIPTOR
15H-1FH	RESERVED	RESERVED

Tab - 2 EEPROM Memory Mapping

Note:
*FLAG:

- Bit0 ➔ Self Powered (for USB GetStatus) 1: self power ; 0 : bus power
- Bit 1 ➔ Reserved
- Bit 2 ➔ RemoteWakeUP support
- Bit 3 ➔ 1
- Bit 4 –5 ➔ Reserved
- Bit 6 ➔ RX drop CRC Enable
- Bit 7 ➔ TX append CRC enable
- Bit 8 ➔ Capture Effective Mode
- Bit 9 – F ➔ Reserved

** PHY TYPE[7:5]

3'b000 = 10/100 Ethernet PHY or 1M HOME PHY (Link report as normal case)
3'b100 = special case 1 (Link report always active)
3'b101 = reserved
3'b111 = No supported PHY
FOR EXAMPLE: EEPROM OFFSET 11 HIGH BYTE IS "E0" MEAN IS NO SUPPORTED SECONDARY PHY.

***Unicode MAC Address:

If the MAC's NODE ID is 01,23,45,67,89,ABh respect to NODE ID 0, NODE ID 1, … NODE ID5
Then the unicode will be 30-31,32-33,34-35,36-37,38-39,41-42h respects to BYTE 1 OF UNICODE MAC ADDRESS- BYTE 2 OF UNICODE MAC ADDRESS, …-BYTE 12 OF UNICODE MAC ADDRESS.

Isolate 2 PHY step procedure by hardware when every hardware reset

1. write 0 PHY_ID isolate and power down
2. write PRIMARILY PHY ID isolate and power down
3. write SECONDARY PHY ID isolate and power down

4.0 USB Commands

There are three command groups for Endpoint 0 in AX88172:

- The USB standard commands
- USB Communication Class commands
- USB vendor commands.

4.1 USB standard commands

- The Language ID is 0x0904 for English
- PPLL means buffer length
- CC means configuration number
- I I means Interface number

SETUP COMMAND	DATA IN/OUT	DESCRIPTION
80 06 00 01 00 00 LL PP	Data PPLL bytes	Get Device Descriptor
80 06 00 02 00 00 LL PP	Data PPLL bytes	Get Configuration Descriptor
80 06 00 03 00 00 LL PP	Data 2 bytes	Get Supported Language ID
80 06 01 03 09 04 LL PP	Data PPLL bytes	Get Manufacture String
80 06 02 03 09 04 LL PP	Data PPLL bytes	Get Product String
80 06 03 03 09 04 LL PP	Data PPLL bytes	Get Serial Number String
80 06 04 03 09 04 LL PP	Data PPLL bytes	Get Configuration String
80 06 05 03 09 04 LL PP	Data PPLL bytes	Get Interface 0 String
80 06 06 03 09 04 LL PP	Data PPLL bytes	Get Interface 1/0 String
80 06 07 03 09 04 LL PP	Data PPLL bytes	Get Interface 1/1 Stirng
80 06 08 03 09 04 LL PP	Data 12 bytes	Get Ethernet Address String
80 08 00 00 00 00 01 00	Data 1 bytes	Get Configuration
00 09 CC 00 00 00 00 00	No Data	Set Configuration
81 0A 00 00 I I 00 01 00	Data 1 byte	Get Interface
01 0B AS 00 00 00 00 00	No Data	Set Interface

Tab - 3 USB stabdard commands

4.2 USB Vendor Commands

SETUP COMMAND	DATA IN/OUT	DESCRIPTION
C0 02 XX YY 0M 00 02 00	Data 2 bytes	Read Rx/Tx SRAM M = 0 : Rx, M=1 : Tx
40 03 XX YY PP QQ 00 00	No Data	Write Rx SRAM
40 04 XX YY PP QQ 00 00	No Data	Write Tx SRAM
40 06 00 00 00 00 00 00	No Data	Software MII Operation
C0 07 PI 00 RG 00 02 00	Data 2 Bytes	Read MII Register
40 08 PI 00 RG 00 02 00	Data 2 Bytes	Write MII Register
C0 09 00 00 00 00 01 00	Data 1 Bytes	Read MII Operation Mode
40 0A 00 00 00 00 00 00	No Data	Hardware MII Operation
C0 0B DR 00 00 00 02 00	Data 2 Bytes	Read SROM
40 0C DR 00 MM SS 00 00	No Data	Write SROM
40 0D 00 00 00 00 00 00	No Data	Write SROM Enable
40 0E 00 00 00 00 00 00	No Data	Write SROM Disable
C0 0F 00 00 00 00 02 00	Data 2 Bytes	Read Rx Control Register
40 10 RR 00 00 00 00 00	No Data	Write Rx Control Register
C0 11 00 00 00 00 03 00	Data 3 Bytes	Read IPG/IPG1/IPG2 Register
40 12 II 00 00 00 00 00	No Data	Write IPG Register
40 13 II 00 00 00 00 00	No Data	Write IPG1 Register
40 14 II 00 00 00 00 00	No Data	Write IPG2 Register
C0 15 00 00 00 00 08 00	Data 8 Bytes	Read Multi-Filter Array
40 16 00 00 00 00 08 00	Data 8 Bytes	Write Multi-Filter Array
C0 17 00 00 00 00 06 00	Data 6 Bytes	Read Node ID
C0 19 00 00 00 00 02 00	Data 2 Bytes (*)	Read Ethernet/HomePNA PhyID
C0 1A 00 00 00 00 01 00	Data 1 Byte	Read Medium Status (**)
40 1B MM 00 00 00 00 00	No Data	Write Medium Mode (**)
C0 1C 00 00 00 00 01 00	Data 1 Byte	Get Monitor Mode Status (***)
40 1D MM 00 00 00 00 00	No Data	Set Monitor Mode On/Off (***)
C0 1E 00 00 00 00 01 00	Data 1 Byte	Read GPIOs (****)
40 1F MM 00 00 00 00 00	No Data	Write GPIOs (****)

* Note1: read 1st byte is Secondary PHY ID; 2nd byte is Primarily PHY ID

** Read / Write Medium status

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read	X	X	X	Flow_Control_En		TxAbortAllow	Full_Duplex	
Write	X	X	X	Flow_Control_En	X	TxAbortAllow	Full_Duplex	X

*** Read / Write Monitor Mode

	Bit7-5	Bit4	Bit3	Bit2	Bit1	Bit0
Read	3'b101	HS/FS	X	Magic_Packet_En	Link_UP_Wake	Monitor_Mode
Write	X	X	X	Magic_Packet_En	Link_UP_Wake	Monitor_Mode

**** Read / Write GPIO

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Read			GPI2	GPO2EN	GPI1	GPO1EN	GPI0	GPO0EN
Write			GPO2	GPO2EN	GPO1	GPO1EN	GPO0	GPO0EN

Interrupt endpoint frame format

Byte Number		
Byte 0	A1	Fixed value 00
Byte 1	00	Fixed value 00
Byte 2	NN	Bit_1: SECONDARY PHY Link state (active high), Bit_0: PRIMARILY PHY LINK STATE
Byte 3	00	Fixed value 00
Byte 4	00	Fixed value 00
Byte 5	80	90h
Byte 6	00	Fixed value 00
Byte 7	00	Fixed value

5.0 USB Configuration Structure

5.1 USB Configuration.

The AX88172 supports 1 Configuration only.

5.2 USB Interface.

The AX88172 supports 2 interfaces, the interface 0 is Data Interface and interface 1 is for Communication Interface.

5.3 USB Endpoints.

The AX88172 supports 4 endpoints.
Endpoint 0 ➔ Control endpoint, it is for configuring device.
Endpoint 1 ➔ (optional) Interrupt endpoint, it is for reporting status
Endpoint 2➔ Bulk Out endpoint, it is for Transmitting Ethernet Packet.
Endpoint 3 ➔ Bulk In endpoint, it is for Receiving Ethernet Packet.

6.0 Electrical Specification and Timings

6.1 Absolute Maximum Ratings

Description	SYM	Min	Max	Units
Operating Temperature	Ta	0	+85	°C
Storage Temperature	Ts	-65	+150	°C
Supply Voltage	Vdd	-0.3	+3.6	V
Input Voltage	Vin	-0.3	Vdd+0.3	V
Output Voltage	Vout	-0.3	Vdd+0.3	V
Lead Temperature (soldering 10 seconds maximum)	Tl	-55	+240	°C

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.

6.2 General Operation Conditions

Description	SYM	Min	Tpy	Max	Units
Operating Temperature	Ta	0	25	+70	°C
Supply Voltage	Vdd	+3.0	+3.30	+3.6	V

6.3 DC Characteristics

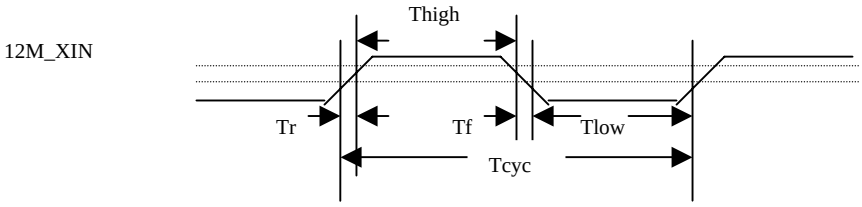
(Vdd=3.0V to 3.6V, Vss=0V, Ta=0°C to 70°C)

Description	SYM	Min	Tpy	Max	Units
Low Input Voltage	Vil	-		0.3*Vdd	V
High Input Voltage	Vih	0.7*Vdd		-	V
Low Output Voltage	Vol	-		0.4	V
High Output Voltage	Voh	2.4		-	V
Input Leakage Current	Iil	-1		+1	uA
Output Leakage Current	Iol	-10		+10	uA
Input Pull-up / down resistance	Ri		75		K ohm

Description	SYM	Min	Tpy	Max	Units
Power Consumption (3.3V)	SPt3v		150		mA

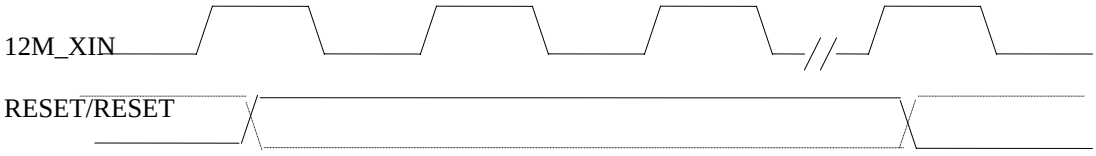
6.4 A.C. Timing Characteristics

6.4.1 12M_XIN (CL=16pF, +/-50ppm)



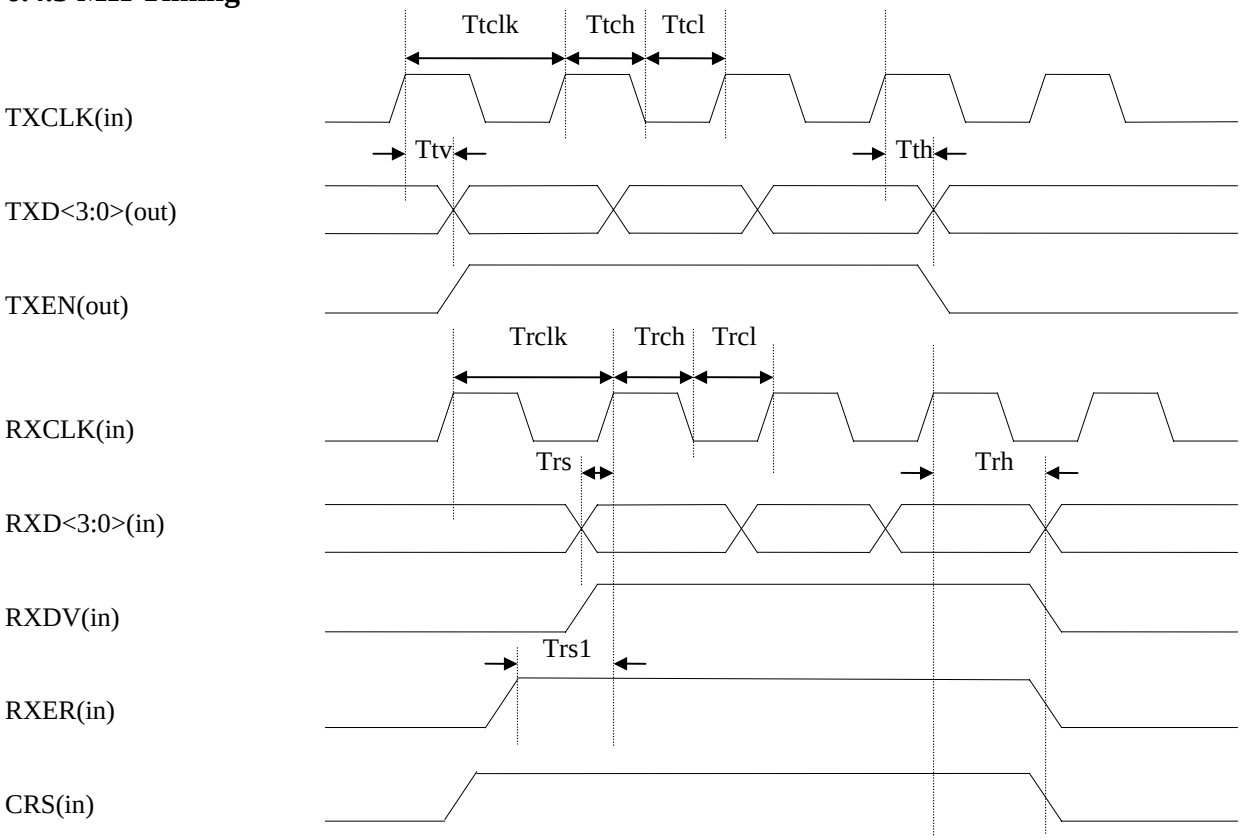
Symbol	Description	Min	Typ.	Max	Units
Tcyc	CYCLE TIME		83.33		ns
Thigh	CLK HIGH TIME	34.71	41.66	49.99	ns
Tlow	CLK LOW TIME	34.71	41.66	49.99	ns
Tr/Tf	CLK SLEW RATE	1	-	4	ns

6.4.2 Reset Timing



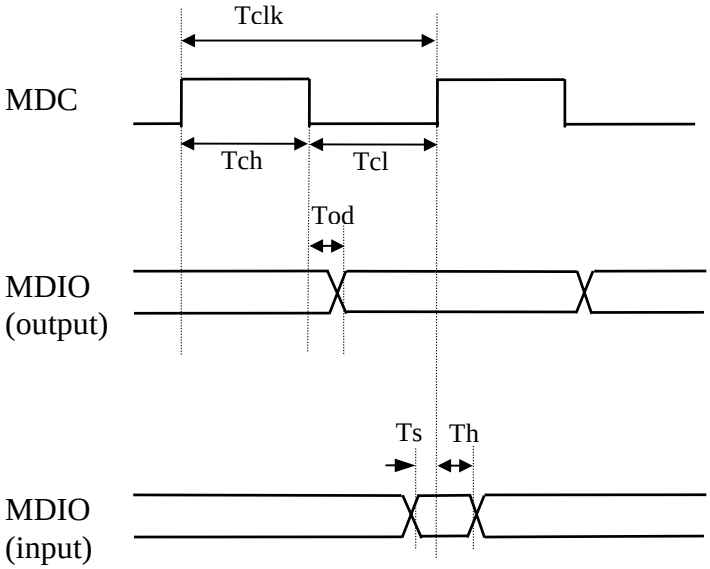
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width (6ms ~10ms)	100	-	-	12M _XIN

6.4.3 MII Timing



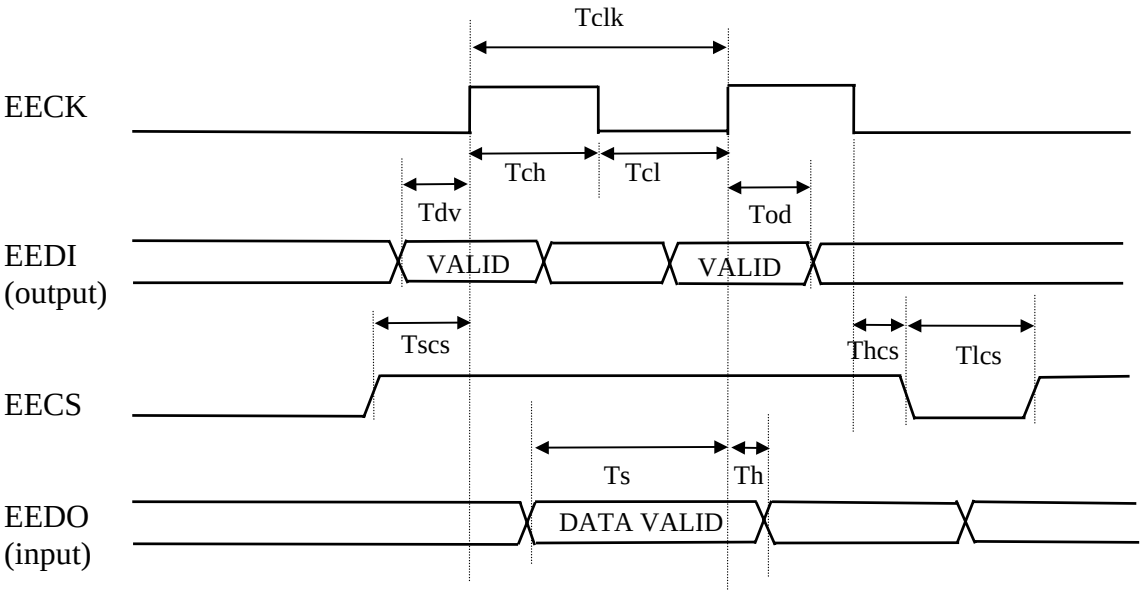
Symbol	Description	Min	Typ.	Max	Units
Ttclk	Cycle time(100Mbps)	-	40	-	ns
Ttclk	Cycle time(10Mbps)	-	400	-	ns
Ttch	high time(100Mbps)	14	-	26	ns
Ttch	high time(10Mbps)	140	-	260	ns
Trch	low time(100Mbps)	14	-	26	ns
Trch	low time(10Mbps)	140	-	260	ns
Ttv	Clock to data valid	3	-	10	ns
Tth	Data output hold time	3	-	10	ns
Trclk	Cycle time(100Mbps)	-	40	-	ns
Trclk	Cycle time(10Mbps)	-	400	-	ns
Trch	high time(100Mbps)	14	-	26	ns
Trch	high time(10Mbps)	140	-	260	ns
Trcl	low time(100Mbps)	14	-	26	ns
Trcl	low time(10Mbps)	140	-	260	ns
Trs	data setup time	6	-	-	ns
Trh	data hold time	6	-	-	ns
Trs1	RXER data setup time	6	-	-	ns

6.4.4 STATION MANAGEMENT TIMING



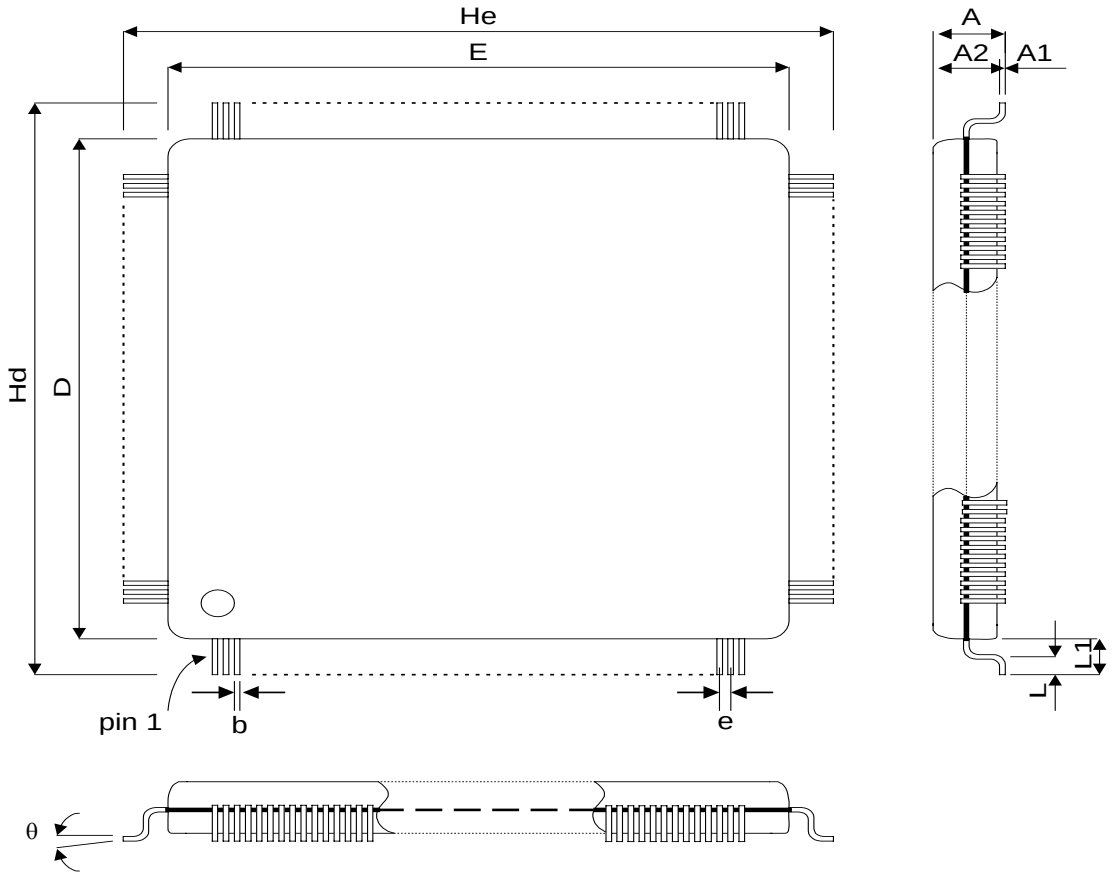
Symbol	Description	Min	Typ.	Max	Units
Tclk	MDC Clock Cycle Time		375		KHz
Tch	MDC Clock High Time		1328		ns
Tcl	MDC Clock Low Time		1328		ns
Tod	Clock Falling Edge to Output Valid Delay	0		2	ns
Ts	Data In Setup Time	10			ns
Th	Data In Hold Time	100			ns

6.4.5 SERIAL EEPROM TIMING



Symbol	Description	Min	Typ.	Max	Units
Tclk	EECK Clock Cycle Time		187.5		KHz
Tch	EECK Clock High Time		2666		ns
Tcl	EECK Clock Low Time		2666		ns
Tdv	EEDI Data Valid Output to EECK High Time	2666			ns
Tod	EECK High to EEDI Data Output Delay Time	2666			ns
Tscs	EECS Valid to EECK High Time	2666			ns
Thcs	EECK Low to EECS Invalid Time	0			ns
Tlcs	Minimum EECS Low Time	23904			ns
Ts	Data Input Setup Time	10			ns
Th	Data Input Hold Time	100			ns

7.0 Package Information

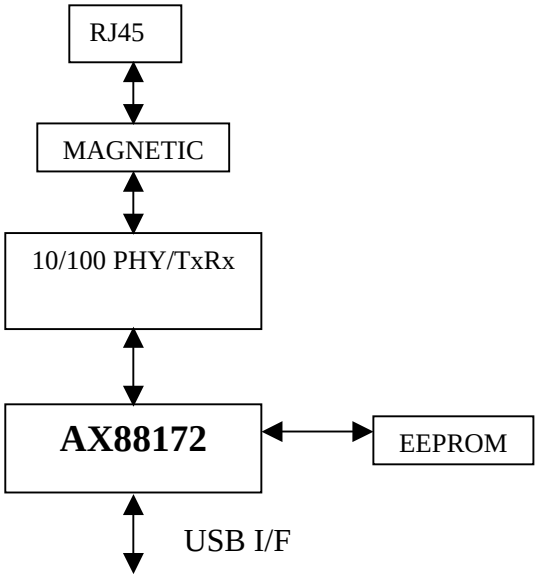


SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.1	0.15
A2	1.3	1.40	1.5
A			1.70
b	0.175	0.18	0.28
D	11.9	12.00	12.1
E	11.9	12.00	12.1
e		0.5	
Hd	13.6	14.00	14.4
He	13.6	14.00	14.4
L	0.3	0.50	0.7
L1		1.00	
θ	0°		10°

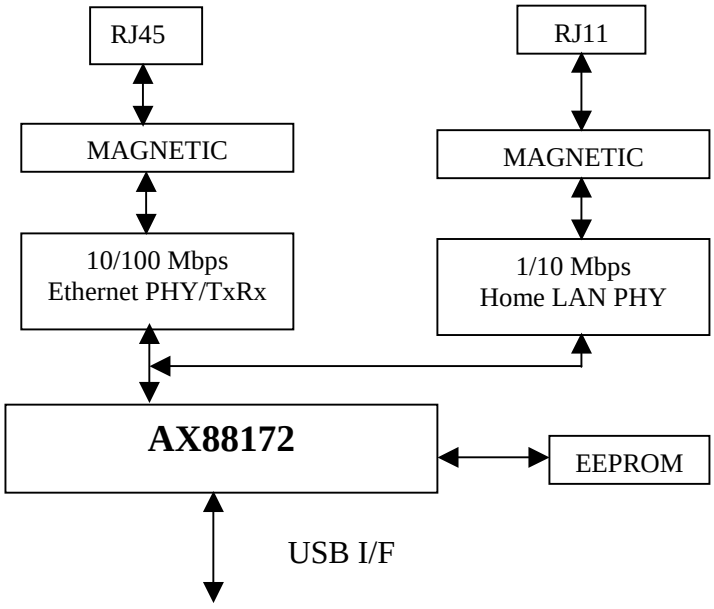
Appendix A: System Applications

Some typical applications for AX88170 are illustrated bellow.

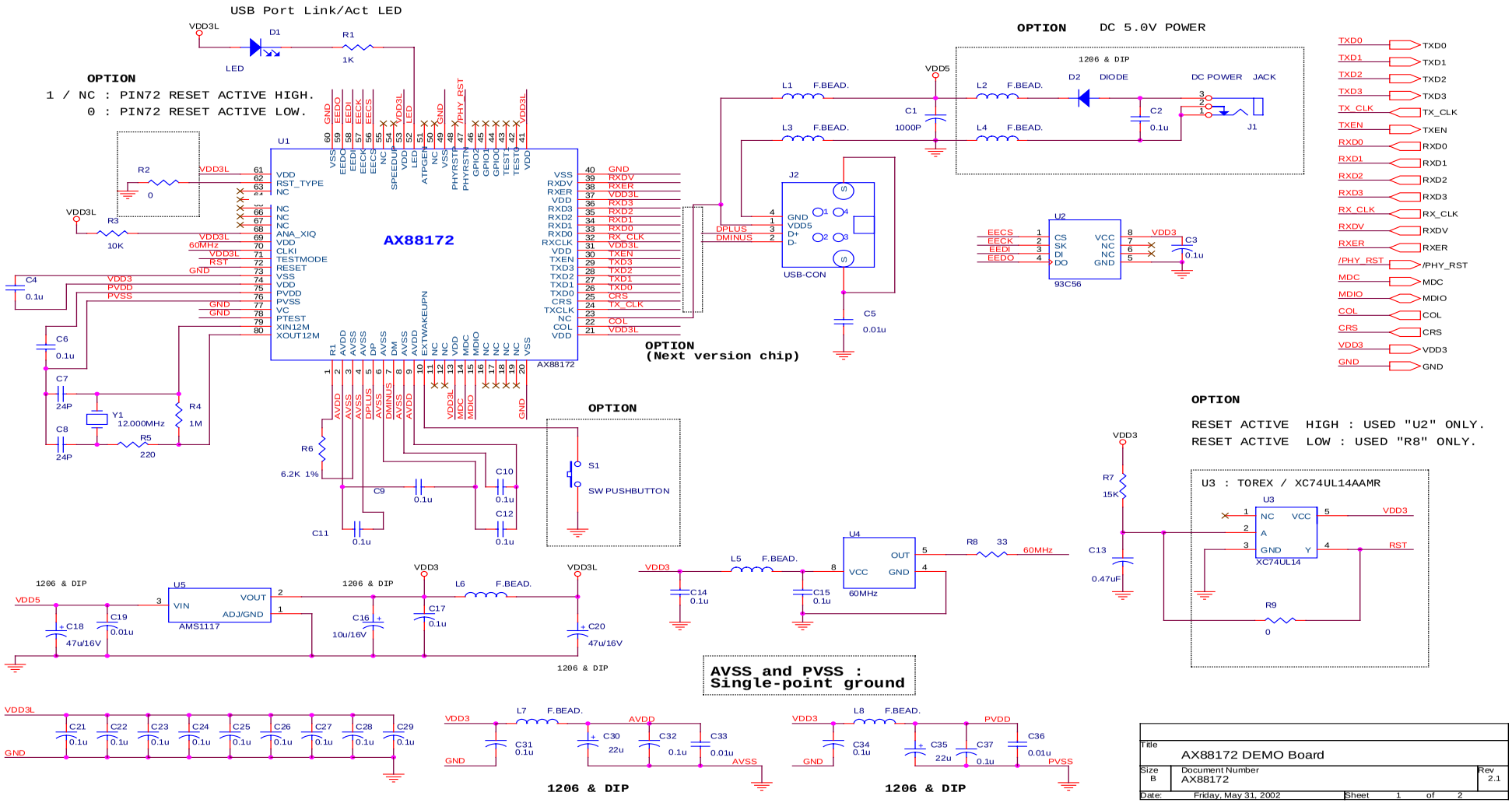
A.1 USB to Fast Ethernet Converter

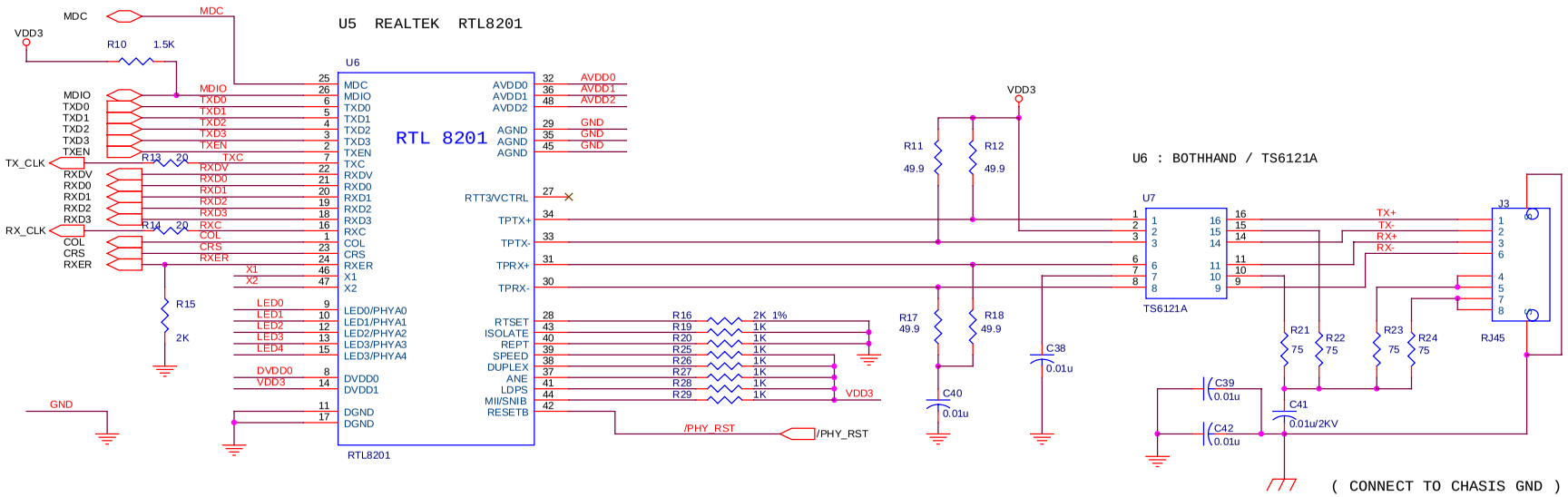


A.2 USB to Fast Ethernet and/or HomeLAN Combo solution

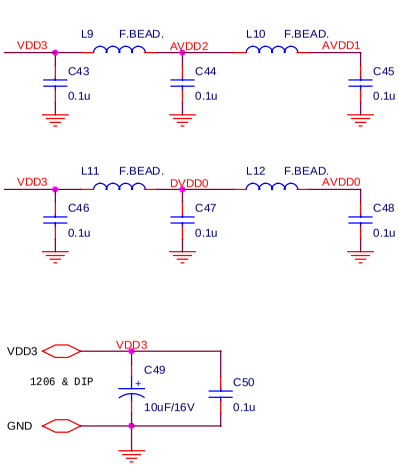


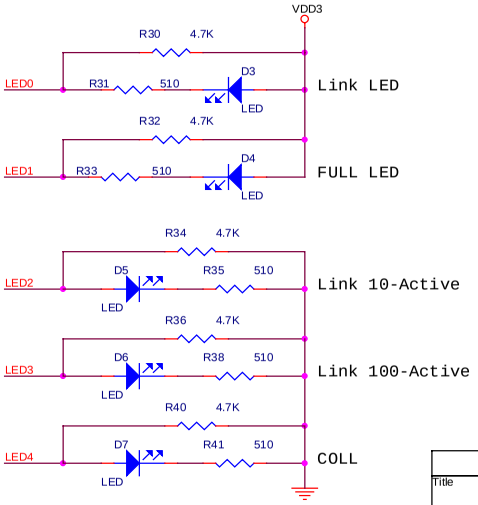
Demonstration Circuit A: AX88172 (ED2 version) + Ethernet PHY(8201L)





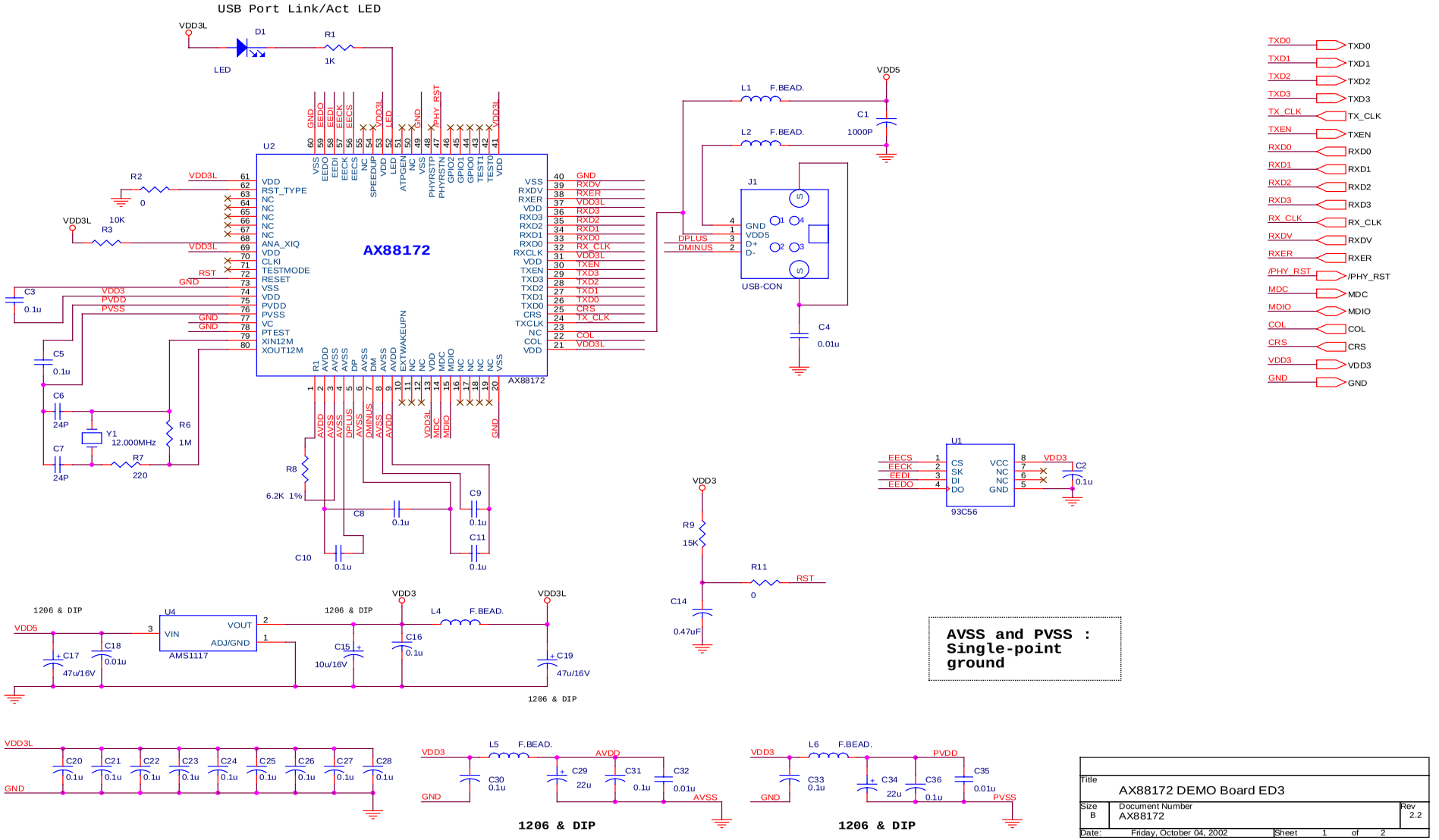
Set PHY ADDRESS TO 00011

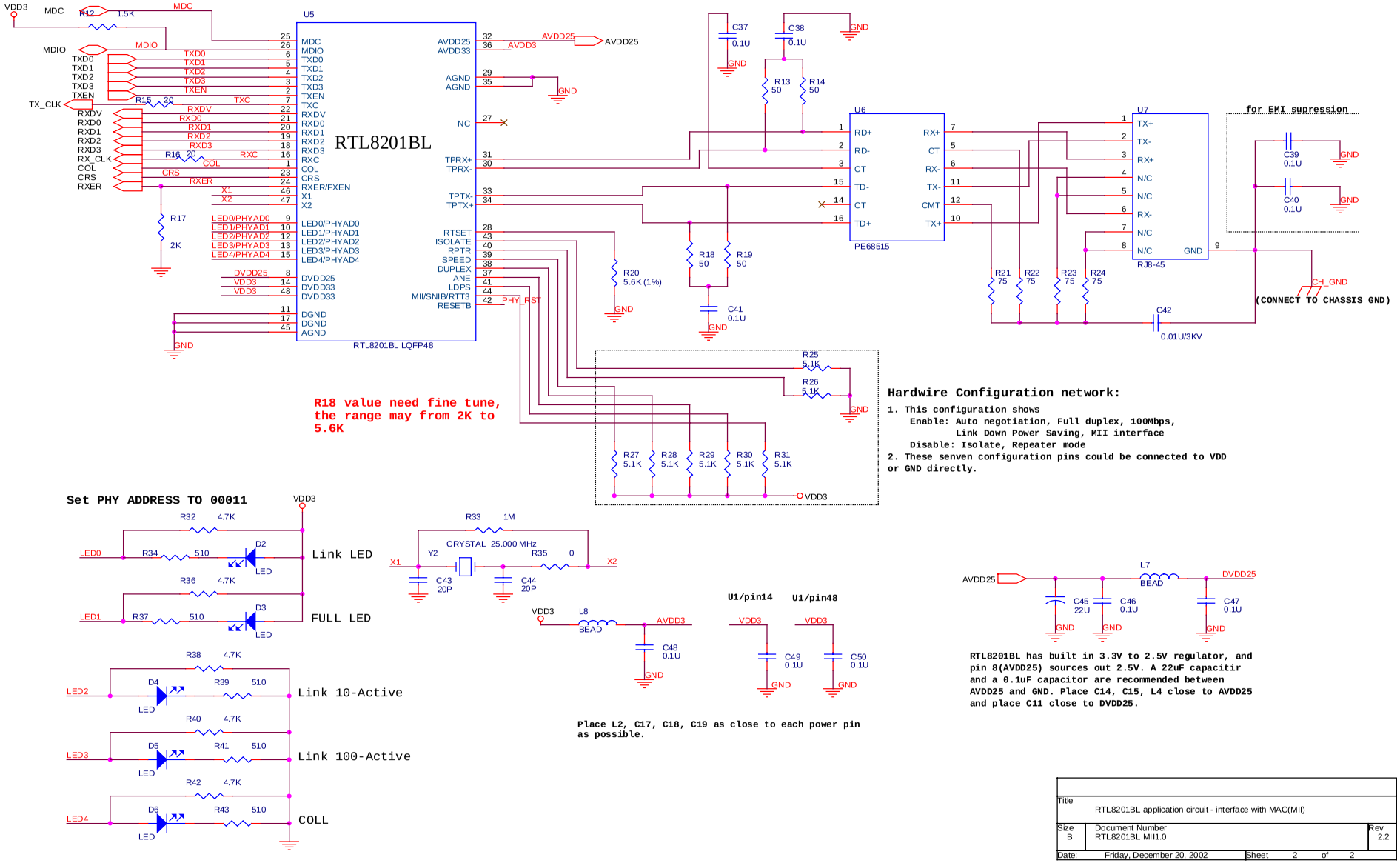




Title: AX88172 DEMO Board		
Size: B	Document Number: RTL8201-TS6121A	Rev: 2.1
Date: Friday, May 31, 2002	Sheet 2 of 2	

Demonstration Circuit B: AX88172 (ED3 version) + Ethernet PHY (8201LBL)





Title	RTL8201BL application circuit - interface with MAC(MII)		
Size B	Document Number RTL8201BL MII1.0		Rev 2.2
Date: Friday, December 20, 2002		Sheet 2 of 2	

Remark:

The schematic change between ED2 and ED3 are shown following:

1. 60MHZ oscillator is no longer needed
2. AX88172 Pin 23 need coonect to VBUS in ED3
3. Pin 70 (CLKI) changes from 60MHz OSC to NC,
4. Pin 71 (test mode) from VDD3L to NC.

Revisions history

Revision	Date	Comment
V. 1.0	12/25/01	Initial Release
V.1.1	12/28/01	Pin 62 change from “SROM size to NC” R1 change from 6K +/-1% to 6.2K+/-1% Power on reset specific 6ms ~10ms “Primary”PHY ID change to “First” PHY ID in EEPROM memory mapping
V.1.2	2002/2/25	Pin 62 change from “NC” to “RST_TYPE” Pin 72 change from “RESET” to”RESET/RESET” On page 12 modify following: USB vendor command modify from “disable H/W MII operation” to “Software MII operation” USB vendor command modify from “Enable H/W MII operation” to “Hardware MII operation” Read/write Mointor mode at read bit 7-5 change from 100 to 101” Add /Reset timing Reference design schematic updated BOM update
V.1.3	2002/5/7	Chip ED2 new schematic with external 60 MHZ Add RTl 8201 BL version schematic Remove BOM
V.1.4	2002/12/20	Add ED3 reference design with RTL 8201BL version PHY and remark the difference Add 12M osc spec

ASIX Electronics Corporation.

4F, NO.8, HSIN ANN RD., SCIENCE-BASED
INDUSTRIAL PARK, HSINCHU, TAIWAN, R.O.C.

TEL: 886-3-5799500
FAX: 886-3-5799558

Email: support@asix.com.tw
Web: http://www.asix.com.tw