High-Performance Non-PCI Single-Chip 32-bit 10/100M Fast Ethernet Controller

Document No: AX88780/V1.4

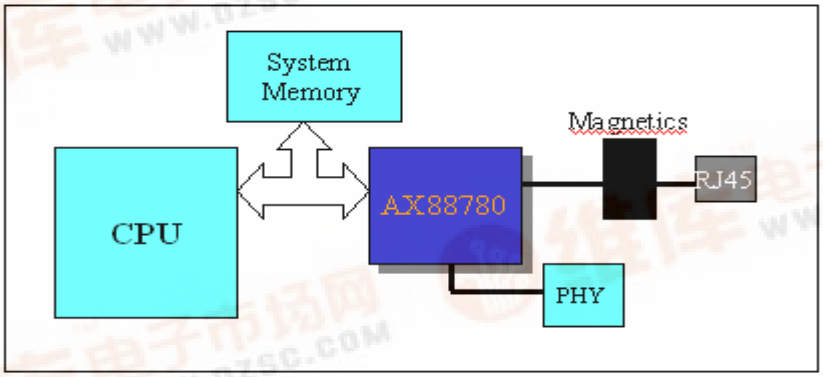
Features

- High-performance non-PCI local bus
  - 16/32-bit SRAM-like host interface
  - Support big/little endian data bus type
  - Large embedded SRAM for packet buffers
    - 32K bytes for receive buffer
    - 8K bytes for transmit buffer
  - Support IP/TCP/UDP checksum offloads
  - Support interrupt with high or low active trigger mode
- Single-chip Fast Ethernet controller
  - Compatible with IEEE802.3, 802.3u standards
  - Integrated Fast Ethernet MAC/PHY transceiver in one chip
  - Support 10Mbps and 100Mbps data rate
  - Support full and half duplex operations
  - Support 10/100Mbps N-way Auto-negotiation operation
  - Support IEEE 802.3x flow control for full-duplex operation
  - Support back-pressure flow control for half-duplex operation
  - Support packet length set by software
  - Support MII interface for external Ethernet PHY and HomePNA/HomePlug PHY applications
- Support Wake-on-LAN function by following events
  - Detection of network link-up state
  - Receipt of a Magic Packet
- Support Magic Packet detection for remote wake-up after power–on reset
- Support EEPROM interface
- Support PCMCIA in 16-bit mode
- Support synchronous or asynchronous mode to host MCU
- Support LED pins for various network activity indications
- Integrated voltage regulator from 3.3V to 2.5V
- 2.5V for core and 3.3V I/O with 5V tolerance
- 128-pin LQFP with CMOS process, RoHS package
- US patent approved (NO 6799231)

Product Description

The AX88780 is a high-performance and cost-effective single-chip Fast Ethernet controller for various embedded systems including consumer electronics and home network markets that require a higher level of network connectivity. The AX88780 supports 16/32-bit SRAM-like host interface and integrates on-chip Fast Ethernet MAC and PHY, which is IEEE802.3 10Base-T and IEEE802.3u 100Base-T compatible. The AX88780 supports full-duplex or half-duplex operation at 10/100Mbps speed with auto-negotiation or manual setting. The AX88780 integrates large embedded SRAM for packet buffers to accommodate high bandwidth applications and supports IP/TCP/UDP checksum to offload processing loading from microprocessor/microcontroller in an embedded system.

System Block Diagram



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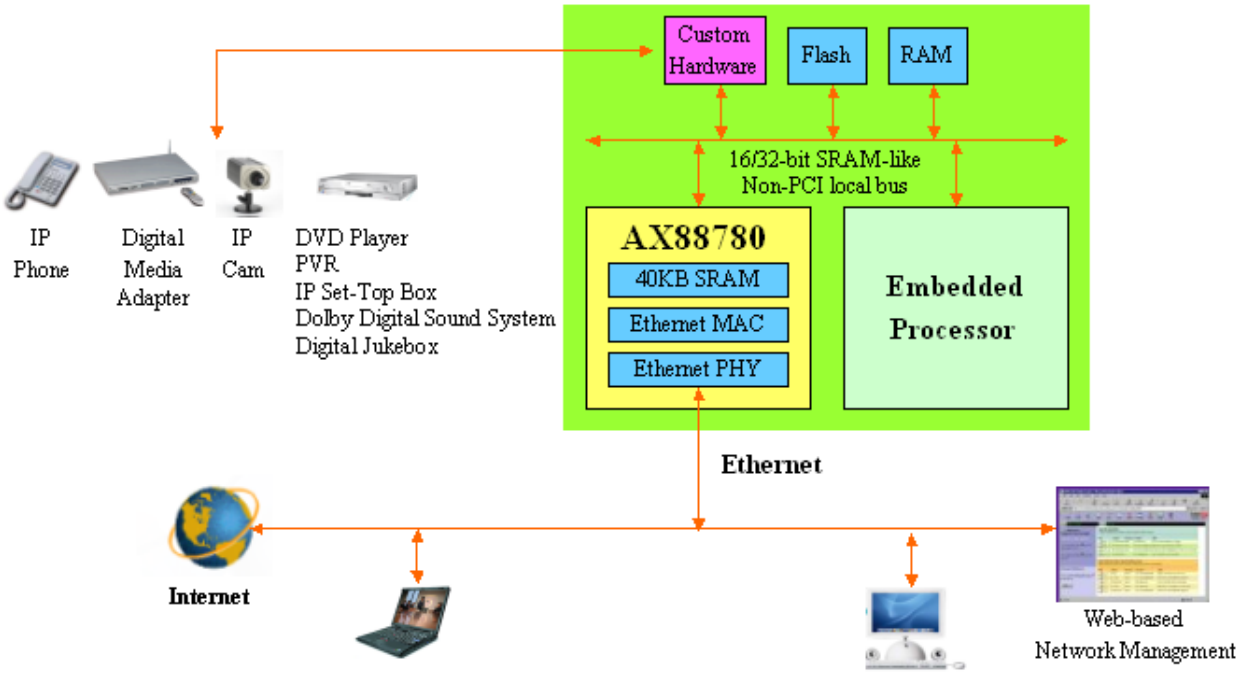
Target Applications

- Multimedia applications
  - Content distribution application
    - Audio distribution system (Whole-house audio)
    - Video-over IP solutions, IP PBX and video phone
    - Video distribution system, multi-room PVR
  - Cable, satellite, and IP set-top box
  - Digital video recorder
  - DVD recorder/player
  - High definition TV
  - Digital media client/server
  - Home gateway
  - IPTV for triple play
- Others
  - Printer, kiosk, security system
  - Wireless router & access point

Applications



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1.0 Introduction

1.1 General Description

AX88780 supports full-duplex or half-duplex operation at 10/100 Mbps speed with auto-negotiation or manual setting. The AX88780 has two built-in synchronous SRAMs for buffering packet. The one is 32K bytes for receiving packets from Ethernet; the other is 8K-bytes for transmitting packets from host system to Ethernet. The AX88780 also has 256 bytes built-in configuration registers. For software programming, the total address space used in AX88780 is 64K bytes in 32-bit mode and at least (8K + 8) bytes in 16-bit mode.

Because AX88780 is a SRAM-like device, AX88780 could be treated as a SRAM device and be attached to SRAM controller of system. Therefore, system can execute DMA cycles to gain the highest performance. AX88780 needs 2 clock sources, one is HCLK and another one is XTLP. The HCLK clock can be from the host system clock or from a stand-along OSC, and the XTLP/XTLN clock is 25Mhz for internal PHY.

1.2 AX88780 Block Diagram

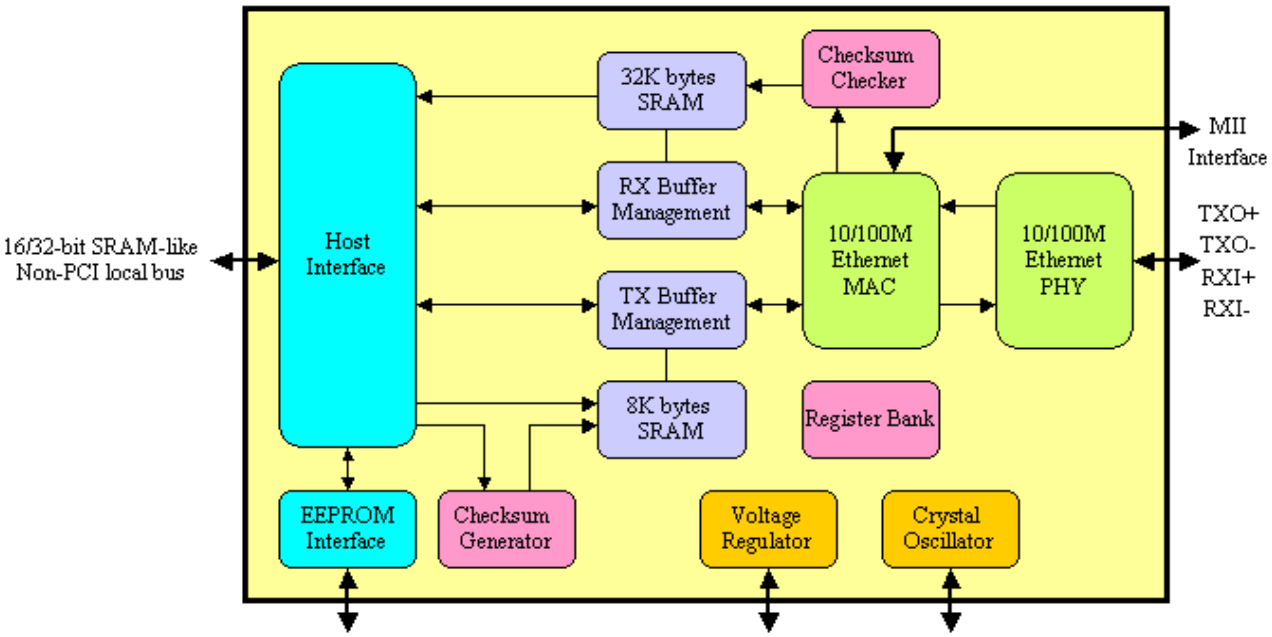


Figure 1: AX88780 block diagram

1.3 AX88780 Pinout Diagram

The AX88780 is housed in the 128-pin LQFP package.

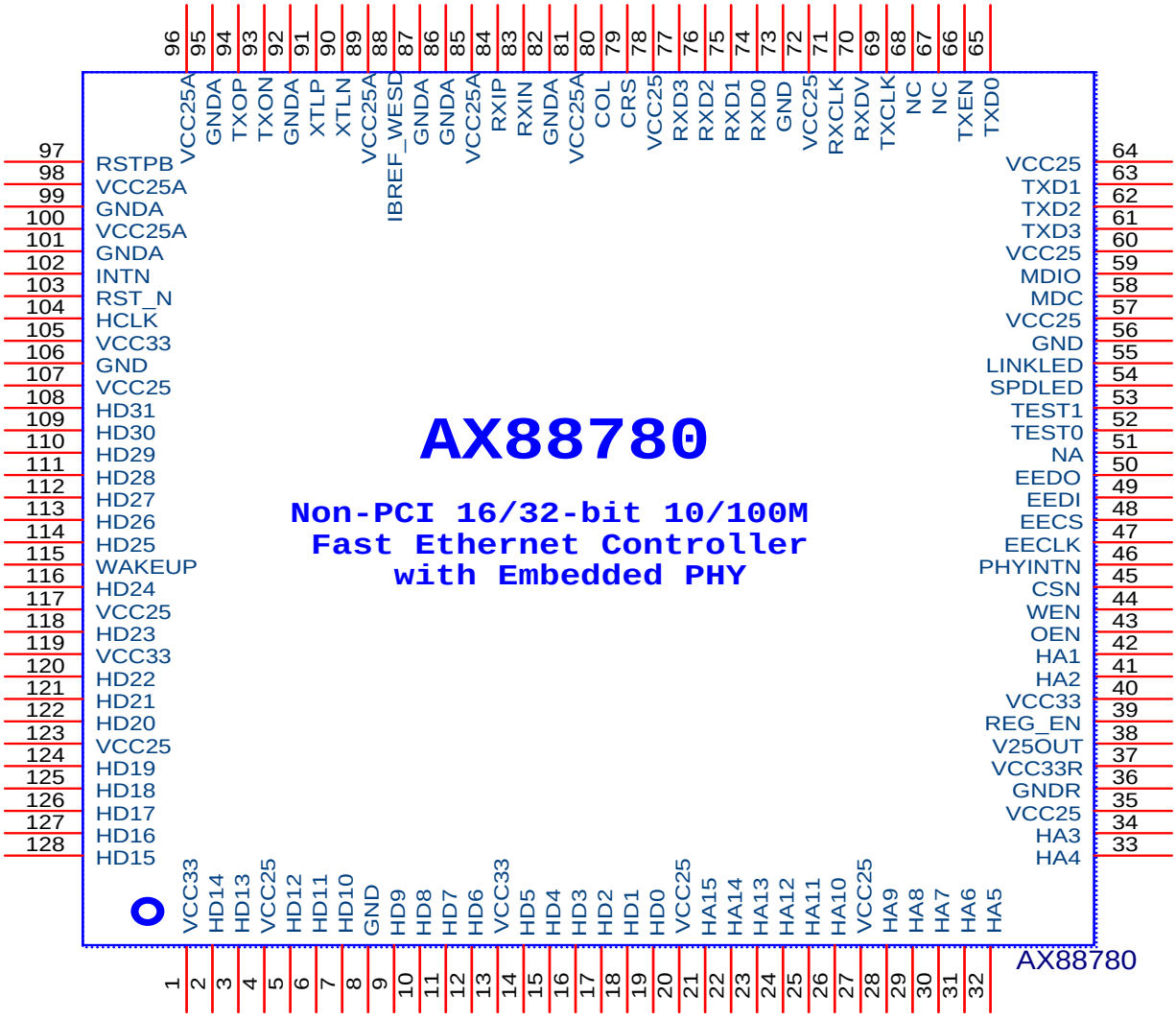


Figure 2: AX88780 pin connection diagram

2.0 Signal Description

2.1 Signal Type Definition

I3:	Input, 3.3V with 5V tolerance
I2:	Input, 2.5V with 3.3V tolerance
I25	Input, 2.5V only
O3:	Output, 3.3V
O2:	Output, 2.5V
IO3:	Input/Output, input 3.3V with 5V tolerance
IO2	Input/Output, input 2.5V with 3.3V tolerance
TSO:	Tri-State Output
OD:	Open Drain allows multiple devices to share as a wire-OR
PD:	Internal 75K Pull Down
PU:	Internal 75K Pull Up
GND:	Ground
VCC3:	3.3V power
VCC2:	2.5V power
I:	Input only
O:	Output only
IO:	Input/Output

2.2 Host Interface

Table 1 : Host Interface signals group

Pin Name	Type	Pin NO	Pin Description
INTN	TSO, 8mA	102	Interrupt to host system When the polarity is active high, this signal must be pulled low, otherwise pulled high in active low environment. Software set the bit6 of command register (CMD) to response the polarity.
RST_N	I3	103	Reset signal: active low.
HCLK	I3	104	Reference Clock. This clock may be from host (synchronous mode) or the output of stand-alone OSC (asynchronous mode).
WAKEUP	TSO, 8mA	115	Wake-up signal to system. When the polarity of system is active high, this signal must be pulled low, otherwise pulled high in active low environment. Software set the bit0 of command register (CMD) to response the polarity.
HD0	IO3, 8mA	19	Data bus bit0.
HD1	IO3, 8mA	18	Data bus bit1.
HD2	IO3, 8mA	17	Data bus bit2.
HD3	IO3, 8mA	16	Data bus bit3.
HD4	IO3, 8mA	15	Data bus bit4.
HD5	IO3, 8mA	14	Data bus bit5.
HD6	IO3, 8mA	12	Data bus bit6.
HD7	IO3, 8mA	11	Data bus bit7.
HD8	IO3, 8mA	10	Data bus bit8.
HD9	IO3, 8mA	9	Data bus bit9.
HD10	IO3, 8mA	7	Data bus bit10.
HD11	IO3, 8mA	6	Data bus bit11.
HD12	IO3, 8mA	5	Data bus bit12.
HD13	IO3, 8mA	3	Data bus bit13.
HD14	IO3, 8mA	2	Data bus bit14.
HD15	IO3, 8mA	128	Data bus bit15.
HD16	IO3, 8mA	127	Data bus bit16, internal pull down. *
HD17	IO3, 8mA	126	Data bus bit17, internal pull down. *
HD18	IO3, 8mA	125	Data bus bit18, internal pull down. *

HD19	IO3, 8mA	124	Data bus bit19, internal pull down. *
HD20	IO3, 8mA	122	Data bus bit20, internal pull down. *
HD21	IO3, 8mA	121	Data bus bit21, internal pull down. *
HD22	IO3, 8mA	120	Data bus bit22, internal pull down. *
HD23	IO3, 8mA	118	Data bus bit23, internal pull down. *
HD24	IO3, 8mA	116	Data bus bit24, internal pull down. *
HD25	IO3, 8mA	114	Data bus bit25, internal pull down. *
HD26	IO3, 8mA	113	Data bus bit26, internal pull down. *
HD27	IO3, 8mA	112	Data bus bit27, internal pull down. *
HD28	IO3, 8mA	111	Data bus bit28, internal pull down. *
HD29	IO3, 8mA	110	Data bus bit29, internal pull down. *
HD30	IO3, 8mA	109	Data bus bit30, internal pull down. *
HD31	IO3, 8mA	108	Data bus bit31, internal pull down. *
HA1	I3	42	Address bus bit1.
HA2	I3	41	Address bus bit2.
HA3	I3	34	Address bus bit3.
HA4	I3	33	Address bus bit4.
HA5	I3	32	Address bus bit5.
HA6	I3	31	Address bus bit6.
HA7	I3	30	Address bus bit7.
HA8	I3	29	Address bus bit8.
HA9	I3	28	Address bus bit9.
HA10	I3	26	Address bus bit10.
HA11	I3	25	Address bus bit11.
HA12	I3	24	Address bus bit12.
HA13	I3	23	Address bus bit13.
HA14	I3	22	Address bus bit14.
HA15	I3	21	Address bus bit15.
WEN	I3	44	Data Write Enable Host drives WEN and it is active low.
CSN	I3	45	Chip Select Enable Host drives CSN and it is active low.
OEN	I3	43	Data Output Enable Host drives OEN and it is active low.

*Note: The internal Pull-down of HD16 to HD31 will be disabled in 32-bit mode.

2.3 EEPROM Interface

Table 2: EEPROM Interface signals group

Pin Name	Type	Pin NO	Pin Description
EECLK	O3, 12mA	47	A low speed clock to EEPROM
EECS	O3, 12mA	48	Chip select to EEPROM device. This pin will be treated as full-duplex indicator when bit10 of PHY_CTRL register is set to high. It is active high in full-duplex mode, and low in half-duplex mode.
EEDI	O3, 12mA	49	Data to EEPROM, valid in EECS is high and EECLK in rising edge. This pin will be treated as collision indicator when bit10 of PHY_CTRL register is set to high. It is active high in collision indicator.
EEDO	I3, PD	50	Data from EEPROM

2.4 Regulator Interface

Table 3: Regulator signals group

Pin Name	Type	Pin No.	Pin Description
VCC33R	VCC3	37	3.3V power to internal regulator
GNDR	GND	36	Ground pin for internal regulator
REG_EN	I3	39	High to enable internal regulator. Low to disable internal regulator.
V25OUT	O2	38	2.5V output from internal regulator, max 250mA, when REG_EN pin is high.

2.5 10/100M PHY Interface

Table 4: 10/100M Twisted-pair signals group

Pin Name	Type	Pin No.	Pin Description
RXIN	I	83	Differential received input signal for both 10BASE-T and 100BSE-TX modes. (Note: please refer to Section 6.1.7 for detailed Transmission Characteristics)
RXIP	I	84	Differential received input signal for both 10BASE-T and 100BSE-TX modes.
TXON	O	93	Differential transmitted output signal for both 10BASE-T and 100BASE-TX modes. (Note: please refer to Section 6.1.6 for detailed Reception Characteristics)
TXOP	O	94	Differential transmitted output signal for both 10BASE-T and 100BASE-TX modes

2.6 MII Interface

Table 5: MII Interface signals group

Pin Name	Type	Pin No.	Pin Description
TXEN	O2, 12mA	66	Transmit Enable: TXEN is transition synchronously with respect to the rising edge of TXCLK. TXEN indicates that the port is presenting nibbles on TXD [3:0] for transmission.
TXD[3:0]	O2, 12mA	61,62, 63,65	Transmit Data: TXD[3:0] is transition synchronously with respect to the rising edge of TXCLK.
TXCLK	I2	69	Transmit Clock: TXCLK is a continuous clock from PHY. It provides the timing reference for the transfer of the TXEN and TXD[3:0] signals from the MII port of PHY.
RXCLK	I2	71	Receive Clock: RXCLK is a continuous clock from PHY. It provides the timing reference for the transfer of the RXDV, RXD[3:0] signals from MII port of PHY.
RXD[3:0]	I2	77,76,75, 74	Receive Data: RXD[3:0] is driven by the PHY synchronously with respect to RXCLK.
RXDV	I2	70	Receive Data Valid: RXDV is driven by the PHY synchronously with respect to RXCLK. Asserted high when valid data is present on RXD [3:0].
COL	I2	80	Collision signal: This signal is driven by PHY when collision is detected.
CRS	I2	79	Carrier Sense: Asynchronous signal CRS is asserted by the PHY when either the transmitted or receive medium is non-idle.
MDIO	IO2, 8mA,PU	59	Station Management Data Input /Output: Serial data input/Output transfers from/to the PHY. The transfer protocol conforms to the IEEE 802.3u MII specification.
MDC	O2, 8mA	58	Station Management Data Clock: The timing reference for MDIO. All data transfers on MDIO are synchronized to the rising edge of this clock.
PHYINTN	I2	46	An interrupt signal from PHY, active low.

2.7 Miscellaneous

Table 6: Miscellaneous signals group

Pin Name	Type	Pin No.	Pin Description
LINKLED	IO3, 12mA, PD	55	In power-on reset phase, this pin will be latched by AX88780 to determine that system operates in 32 or 16-bit mode. High state is 16-bit mode and low state is 32-bit mode. The default is in 32-bit mode. Upon finishing reset status, if bit11 of PHY_CTRL register is enabled, this pin stands for: Link: indicates a good link status, active low in 16-bit mode and active high in 32-bit mode. The link indicator only works under bit11 of PHY_CTRL register set by driver. Traffic: indicates the traffic status and flashes while in TX or RX state.
SPDLED	IO3, 12mA, PD	54	In power-on reset phase, this pin will be latched by AX88780 to determine whether AX88780 swaps the data or not. If the high state, AX88780 will swap the data (big-endian). The default is little-endian. Upon finishing reset stage, if bit12 PHY_CTRL register is enabled, this pin stands for speed mode. In little-endian mode, low indicates that PHY is in 10BASE-TX mode, and high state indicates PHY is in 100BASE-T mode. In big-endian mode, low indicates that PHY is in 100Mbase-T mode and high state indicates PHY is in 10Base-TX mode. The speed indicator only works under bit12 of PHY_CTRL register set by driver.
NA	I3	51	This pin is tied to ground for normal operation.
TEST0	I3, PD	52	Pull down (by 4.7K) or floating for normal operation.
TEST1	I3, PD	53	Pull down (by 4.7K) or floating for normal operation.
XTLN	I25	90	25Mhz crystal or oscillator clock input. The recommended reference frequency is 25Mhz +/- 0.005% (i.e. 25Mhz +/- 1250hz). This input pin is only 2.5V tolerant and should not apply 3.3V clock signal directly to this pin if an external oscillator is used.
XTLP	O2	91	25MHz crystal clock output. For 25MHz oscillator clock, this pin should be kept floating.
RSTPB	I25	97	Pull-up for normal operation.
IBREF_WESD	I25	88	Connect a 12.3Kohm resistor to ground.
NC	O	67,68	No connection

2.8 Power/ground pin

Table 7: Power/Ground pins group

Pin Name	Type	Pin No.	Pin Description
VCC33	VCC3	1,13,40, 105, 119	Digital 3.3V power
VCC25	VCC2	4,20,27,35,57,60,64,72,78,107,117,123	Digital 2.5V power
GND	GND	8, 56, 73,106	Digital ground
VCC25A	VCC2	81,85,89,96,98,100	2.5V power for PHY analog part
GNDA	GND	82,86,87,92,95,99,101	Analog ground

3.0 Functional Description

3.1 Host Interface

AX88780 supports a very simple SRAM-like interface. There are only 3 control signals to operate the read or write. For write operation, host activates CSN and WEN to low with address and data bus. AX88780 will decode and latched the data into internal buffer. For normal operation, the WEN needs at least 4 clocks duration for one 32/16-bit write operation. The CSN can always be driven, but WEN must at least be de-asserted 1 clock before next access. For read operation, host asserts CSN and OEN at least 5 clocks to AX88780, the data will be valid after 4 clocks. AX88780 also support burst mode if host reads/writes AX88780 by continuous access. Note: The burst mode only supports in TX/RX, not supports in register read/write. That is, read RX area from XXXX_0000 to XXXX_7FFF or write TX area from XXXX_8000 to XXXX_FBFF can be accessed by burst mechanism.

3.2 System Address Range

AX88780 is suitable to attach to SRAM controller, so it needs 64K memory space to operate. The designer can allocate any block (64K) in system space. From offset 0x0000 to 0x7FFF is for RX operation, and offset 0x8000 to 0xFBFF is for TX operation. The internal configuration register of AX88780 is allocated in offset 0xFC00 to 0xFCFF. Below is the mapping of addressing.

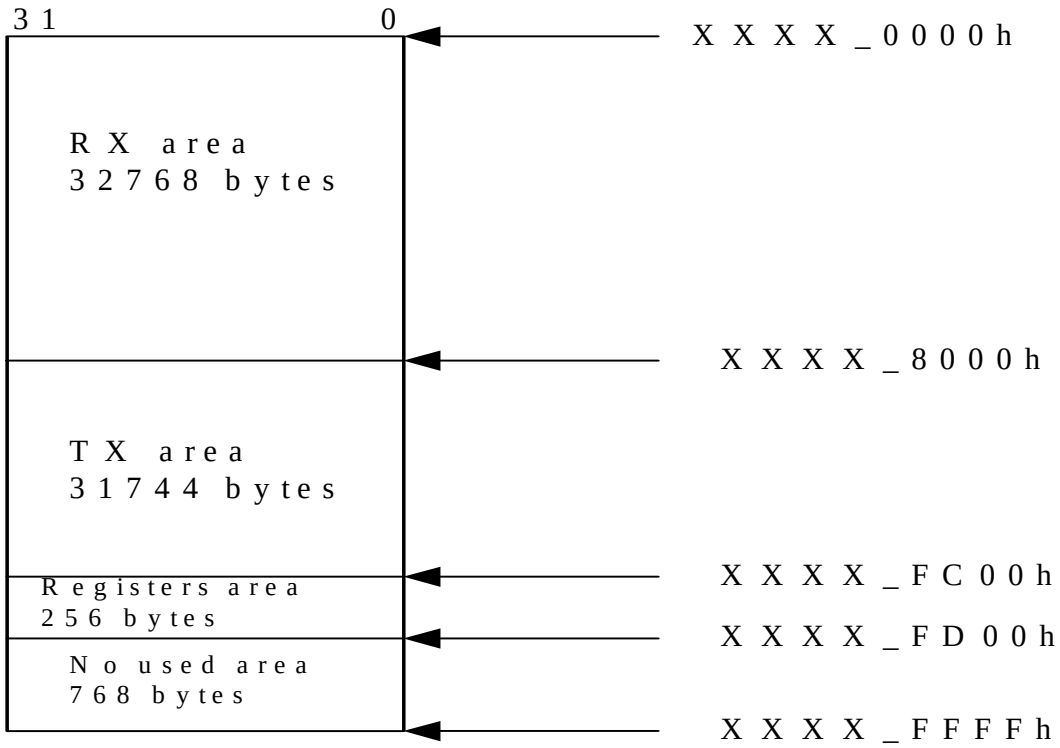


Figure 3: 32-bit mode address mapping

3.3 TX Buffer Operation

AX88780 employs 4 descriptors to maintain transmit information, such as packet length, start bit. These descriptors are located in offset 0xFC20, 0xFC24, 0xFC28 and 0xFC2C. Driver can choose any descriptor whenever there is data need to be transmitted. Since there are only 4 descriptors, upon running out of descriptors, driver must wait for the descriptor is to be released by AX88780.

3.4 RX Buffer Operation

AX88780 is built a 32K SRAM for RX operation. It utilizes ring structure to maintain the input data from PHY and read out to host. There are two pointer registers located in offset 0xFC34 and 0xFC38. AX88780 will maintain RXCURT register. Upon it receives a valid packet from PHY it will update RXCURT according to the packet length. Driver reads data from AX88780 and maintains the RXBOUND register. When driver finishes reading packet, it must update RXBOUND according to the packet length. AX88780 utilizes RXCURT and RXBOUND to provide receive buffer status, full or empty.

3.5 Flow Control

In full duplex mode, AX88780 supports the standard flow control mechanism defined in IEEE 802.3x standard. It enables the stopping of remote node transmissions via a PAUSE frame information interaction. When space of the packet buffer is less than the threshold values (RXBTHD0, RXBTHD1), AX88780 will send out a PAUSE-ON packet to stop the remote node transmission. And then AX88780 will send out a PAUSE-OFF packet to inform the remote node to retransmit packet if it has enough space to receive packets.

3.6 Checksum Offloads and Wake-up

To reduce the computing loading of CPU, AX88780 is built checksum operator for IP, UDP or TCP packet. AX88780 will detect the packet whether it is IP, UDP or TCP packet. If it is an IP packet, AX88780 will calculate the checksum of header and put the result in checksum filed of IP. Then it continuously checks the packet whether it is UDP or TCP. It will perform the checksum operation whenever it is a UDP or TCP packet. AX88780 also automatically skip the VLAN tag when checksum is executed. AX88780 also supports to detect magic packet or link-up to wake up system when system is in sleep state or needs to cold start by magic packet.

3.7 Fast-Mode support

To improve the throughput in embedded system, AX88780 supports fast-mode for TX/RX buffer access. Host can access AX88780 by driving CSN to low and toggle WEN (write) or OEN (read). AX88780 can support the burst until whole packet access. The access timing can refer to section 6.2.4 and 6.2.6. This mechanism is only for TX/RX buffer access. For configuration register access, it must use single access.

3.8 Big/Little-endian support

AX88780 supports “Big” or “Little” endian data format. The default is Little-endian. Designer can pull-up SPDLED pin to high to swap the data format. Below table can depict the relation. This swap is only valid in 32-bit mode.

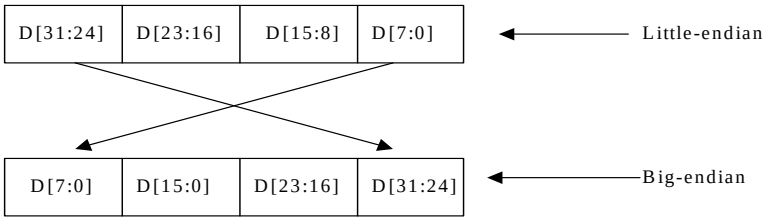


Figure 4: data swap block

3.9 10/100BASE-TX PHY

AX88780 integrates high performance PHY that is fully compliant with 10/100BASE-TX Ethernet standards such as IEEE 802.3, IEEE 802.3u and ANSI X3.263-1995. It’s main features can described below.

Adaptive equalizer

This equalizer mainly eliminates the distortions caused by inter-symbol interference (ISI) by automatically adjusting the mathematical coefficient to match the cable length.

Baseline wander correct

The transmitter sends DC and AC signals as a pair. The receiving device and transmitting device each have a transformer that blocks the Dc signal. When the AC signal loses its DC component, the AC signal becomes distorted. The Baseline-Wander correct ill restores the DC component to AC signal and delivers it as a complete signal to receiver.

Link monitor/signal detect

This feature is used to detect the signal’s level. If the detected signal is above 400mV in 100BASE-TX mode, it will generate a Signal Detected (SD) to MAC. If the level is below 400mV, the SD signal will be de-asserted 1ms.

Carrier detect and 4B/5B coding

The Physical Coding Sub-layer (PCS) checks with Physical Medium Attachment (PMA) data to see if the packets meet IEEE 802.3u defined preamble (J/K/packets in 100BASE-TX) standards. If the packets meet the standards, the PCS sub-layer will start to process the data and send to MAC engine. The PCS converts received/transmitted data according IEEE 802.3u defined coding standards, such as 4B/5B and scrambling/de-scrambling.

3.9 16-bit Mode

AX88780 also supports 16-bit mode operation. AX88780 driver should request at least (8K + 8) bytes space for TX, RX and register access. For example, the driver requests a 16K bytes space from system and then sets the new window base address to MEMBAS6 register. After that, driver should set bit 0 (DECODE_EN) of MEMBASE register to start decoding for TX buffer, RX buffer and registers access. (Note: AX88780 H/W only decodes low 16-bit offset address.)

MEMBASE--Memory base Address

Field	Name	Type	Default	Description
15:1	-	R/W	-	Reserved. The output value is undefined if software read this field.
0	DECODE_EN	R/W	0	16-bit decode enable Set to '1' to start decoding.

MEMBAS6--Memory base Address + 6

Field	Name	Type	Default	Description
15:8	-	R/W	-	Reserved. The output value is undefined if software read this field.
7:0	WINSIZE	R/W	0x00	Window Base Pointer. (The MSB of new window base address) This field defines another new windows base address for TX, RX and register access. The total size is 8K bytes. TX areas occupy 3840 bytes Registers occupy 256 bytes. RX areas occupy 4096 bytes.

Note: The WINSIZE field of this address is used to define the MSB of new window base address, the TX buffer, RX buffer and registers should be accessed through this new window base address in 16-bit mode. Please refer to below mapping mechanism for details.

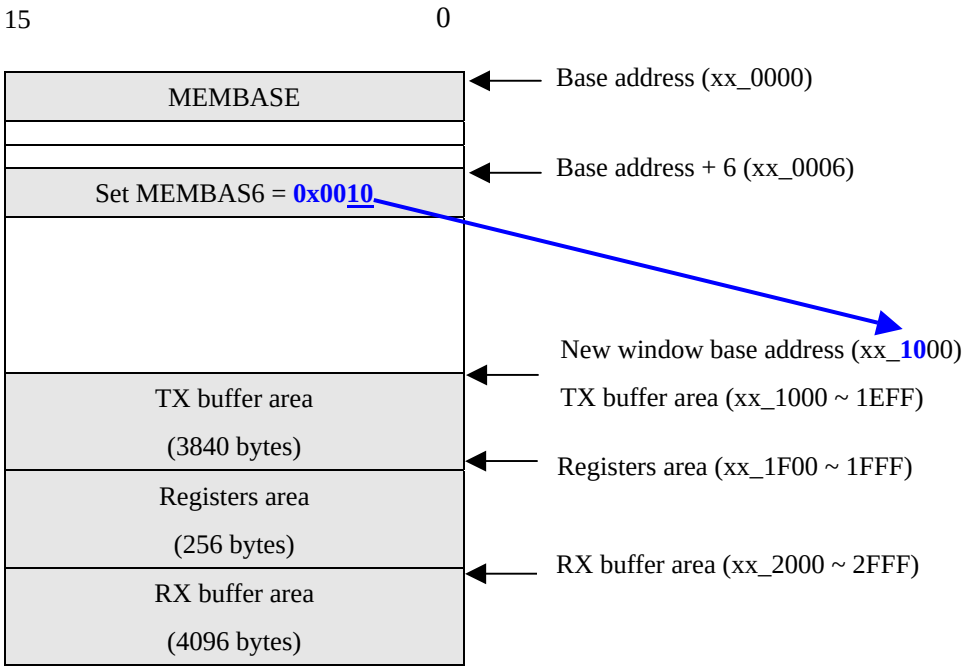


Figure 5: 16-bit mode address mapping

The following is an example to indicate how to define a new window base address in 16-bit mode by configuring the MEMBAS6 register. If AX88780 is allocated at the memory base address 0x20_0000 by hardware (i.e. the MEMBASE register is allocated at 0x20_0000) and users would like to set the new window base address to 0x20_1000, the driver should write 0x0010 to the MEMBAS6 register (offset 0x20_0006). In this case, the TX buffer area will be allocated from 0x20_1000 to 0x20_1EFF; the registers area will be allocated from 0x20_1F00 to 0x20_1FFF and the RX buffer area will be allocated from 0x20_2000 to 0x20_2FFF.

3.11 EEPROM Format

AX88780 will auto-load data from EEPROM device after hardware reset. If the EEPROM device is not attached, the loading operation will be discarded. The EEPROM mainly provides MAC address information and CIS information if it is used in PCMCIA environment. Below table is the format if EEPROM device is employed. Note: If the MAC address is 12 34 56 78 9A BC (MSB-LSB) then driver should set MACID0=0x9ABC, MACID1=0x5678 and MACID2=0x1234.

Address	Description
0	Pointer to CIS area starting address. Set this field to 0x0070 to shorten the download EEPROM if there is no CIS needed. AX88780 only supports 93C56-16bit mode, thus the max value of this field is 0x007F. This field should not be set to 0x0000 or 0xFFFF; otherwise, AX88780 will not recognize the EEPROM during hardware reset.
1	MACID0 data
2	MACID1 data
3	MACID2 data
4	Reserved, keep all 0's
5	Bit0: When LINKLED is set to '1' in reset stage, this bit indicates AX88780 whether or not it is in the environment of PCMCIA. 0 = General 16-bit mode, 1= Special for PCMCIA environment of 16-bit mode. Bit1: 0 = Use external PHY, 1 = Use internal PHY. This function is independent from PHY_EN bit of PHY_CTRL register. Either of both is set will force AX88780 to select internal PHY. Others bit set to 0s for normal operation
6 ~ 11	Reserved, keep all 0's
12 ~ 127	CIS area, if it used in PCMCIA system, otherwise don't care these fields

4.0 Register Description

There are some registers located from offset 0xFC00 to 0xFCFF. All of the registers are 32-bit boundary alignment, but only low 16-bit are available (exception 0xFC54). For reserved bits, don't set them in normal operation.

Table 8: MAC Register Mapping

Offset	Name	Description	Default value
0xFC00	CMD	Command Register	0x0000_0201
0xFC04	IMR	Interrupt Mask Register	0x0000_0000
0xFC08	ISR	Interrupt Status Register	0x0000_0000
0xFC10	TX_CFG	TX Configuration Register	0x0000_0040
0xFC14	TX_CMD	TX Command Register	0x0000_0000
0xFC18	TXBS	TX Buffer Status Register	0x0000_0000
0xFC1C	PHY_CTRL	Internal PHY Control Register*	0x0000_0000
0xFC20	TXDES0	TX Descriptor0 Register	0x0000_0000
0xFC24	TXDES1	TX Descriptor1 Register	0x0000_0000
0xFC28	TXDES2	TX Descriptor2 Register	0x0000_0000
0xFC2C	TXDES3	TX Descriptor3 Register	0x0000_0000
0xFC30	RX_CFG	RX Configuration Register	0x0000_0101
0xFC34	RXCURT	RX Current Pointer Register	0x0000_0000
0xFC38	RXBOUND	RX Boundary Pointer Register	0x0000_07FF
0xFC40	MAC_CFG0	MAC Configuration0 Register	0x0000_8157
0xFC44	MAC_CFG1	MAC Configuration1 Register	0x0000_6000
0xFC48	MAC_CFG2	MAC Configuration2 Register	0x0000_0100
0xFC4C	MAC_CFG3	MAC Configuration3 Register	0x0000_060E
0xFC54	TXPAUT	TX Pause Time Register	0x001F_E000
0xFC58	RXBTHD0	RX Buffer Threshold0 Register	0x0000_0300
0xFC5C	RXBTHD1	RX Buffer Threshold1 Register	0x0000_0600
0xFC60	RXFULTHD	RX Buffer Full Threshold Register	0x0000_0100
0xFC68	MISC	Misc. Control Register	0x0000_0013
0xFC70	MACID0	MAC ID0 Register*	0x0000_0000
0xFC74	MACID1	MAC ID1 Register*	0x0000_0000
0xFC78	MACID2	MAC ID2 Register*	0x0000_0000
0xFC7C	TXLEN	TX Length Register	0x0000_05FC
0xFC80	RXFILTER	RX Packet Filter Register	0x0000_0004
0xFC84	MDIOCTRL	MDIO Control Register	0x0000_0000
0xFC88	MDIODP	MDIO Data Port Register	0x0000_0000
0xFC8C	GPIO_CTRL	GPIO Control Register*	0x0000_0003
0xFC90	RXINDICATOR	Receive Indicator Register	0x0000_0000
0xFC94	TXST	TX Status Register	0x0000_0000
0xFCA0	MDCLKPAT	MDC Clock Pattern Register	0x0000_8040
0xFCA4	RXCHKSUMCNT	RX IP/UDP/TCP Checksum Error Counter	0x0000_0000
0xFCA8	RXCRCNT	RX CRC Error Counter	0x0000_0000
0xFCAC	TXFAILCNT	TX Fail Counter	0x0000_0000
0xFCB0	PROMDPR	EEPROM Data Port Register	0x0000_0000
0xFCB4	PROMCTRL	EEPROM Control Register	0x0000_0000
0xFCB8	MAXRXLEN	MAX. RX packet Length Register	0x0000_0600
0xFCC0	HASHTAB0	Hash Table0 Register*	0x0000_0000
0xFCC4	HASHTAB1	Hash Table1 Register*	0x0000_0000
0xFCC8	HASHTAB2	Hash Table2 Register*	0x0000_0000
0xFCCC	HASHTAB3	Hash Table3 Register*	0x0000_0000
0xFCE0	DOGTHD0	Watch Dog Timer Threshold0 Register	0x0000_FFFF
0xFCE4	DOGTHD1	Watch Dog Timer Threshold1 Register	0x0000_0000
0xFCEC	SOFTRST	Software Reset Register	0x0000_0003

***Note: It is not affected by software reset**

4.1 CMD--Command Register

Offset Address = 0xFC00 Default = 0x0000_0201

Field	Name	Type	Default	Description
31:16	-	R/W	All 0's	Reserved
15	RXVLAN	R/W	0	RX VLAN indicator Driver enables this bit to indicate AX88780 that the received packet will include 4 bytes VLAN tag; AX88780 will skip 4 bytes when it calculates the checksum of IP, TCP or UDP packet. 1 = enable 0 = disable
14	TXVLAN	R/W	0	TX VLAN indicator Driver enables this bit to indicate AX88780 that the transmitted packet will include 4 bytes VLAN tag; AX88780 will skip 4 bytes when it calculates the checksum of IP, TCP or UDP packet. 1 = enable 0 = disable
13:10	-	R/W	All 0's	Reserved
9	RXEN	R/W	1	RX Function Enable When this bit is enabled, MAC starts to receive packets. 1 = enable 0 = disable
8	TXEN	R/W	0	TX Function Enable When this bit is enabled, MAC could start to transmit packet to Ethernet. 1 = enable 0 = disable
7	-	R/W	0	Reserved
6	INTMOD	R/W	0	Interrupt Active Mode Driver sets this bit to indicate AX88780 that the interrupt of system is activated high or low. 1: Active high 0: Active low
5:1	-	R/W	All 0's	Reserved
0	WAKEMOD	R/W	1	WAKEUP pin polarity Driver sets this bit to indicate AX88780 that the polarity of system wake-up signal is activated high or low. 1: Active high 0: Active low

4.2 IMR--Interrupt Mask Register

Offset Address = 0xFC04 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	PHYMASK	R/W	0	PHY interrupt Mask When this bit is enabled, an interrupt request from PHY set in bit 5 of Interrupt Status Register will make AX88780 to issue an interrupt to host. 1 = enable 0 = disable
4	PRIM	R/W	0	Packet Received Interrupt Mask When this bit is enabled, a received interrupt request set in bit 4 of Interrupt Status Register will make AX88780 to issue an interrupt to host. 1 = enable 0 = disable
3	PTIM	R/W	0	Packet Transmitted Interrupt Mask When this bit is enabled, a transmitted interrupt request set in bit 3 of Interrupt Status Register will make AX88780 issue an interrupt to host.

				1 = enable 0 = disable
2	-	R/W	0	Reserved
1	DOGIM	R/W	0	Watch Dog Timer Interrupt Mask When this bit is enabled, a watch dog timer expired interrupt request set in bit1 of Interrupt Status Register will make AX88780 to issue an interrupt to host 1 = enable 0 = disable
0	RXFULIM	R/W	0	Rx Buffer Full Interrupt Mask When this bit is enabled, a RX buffer full interrupt request set in bit 0 of Interrupt Status Register will make AX88780 to issue an interrupt to host. 1 = enable 0 = disable

4.3 ISR--Interrupt Status Register

Offset Address = 0xFC08 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	PHYIG	R/W	0	PHY Interrupt Generation If this bit is set to '1' it means there is an interrupt request from PHY. MAC will forward this interrupt to system. Meantime driver should poll PHY and adopt proper procedure. Write '1' to this bit to clear this request status. 1 = have interrupt request 0 = no interrupt request
4	RPIG	R/W	0	Receive Packet Interrupt Generation If this bit is set to '1' it means MAC receives a packet or (packets) from cable. The packet is kept in RX buffer. Write '1' to this bit to clear this request status. 1 = have received packet 0 = no received packet
3	FTPI	R/W	0	Finish Transmitting Packet Interrupt If this bit is set to '1' it means MAC had transmitted packet to cable. Write '1' to this bit to clear this request status. 1 = finish transmitting 0 = none
2	-	R/W	0	Reserved
1	WDTEI	R/W	0	Watch Dog Timer Expired Interrupt If this bit is set to '1' it means the WATCH DOG timer is expired. AX88780 will issue an interrupt to host. Write '1' to this bit to clear this request status. The expired duration can refer to DOGTHD0 and DOGTHD1 registers. 1 = timer expired happens 0 = none
0	RXFULI	R/W	0	RX Buffer Full Interrupt If this bit is set to '1' it means RX buffer is full and no more packets will be received until packets are read out. Write '1' to this bit to clear this request status. 1 = RX buffer full 0 = None

4.4 TX_CFG--TX Configuration Register

Offset Address = 0xFC10 Default = 0x0000_0040

Field	Name	Type	Default	Description
31:7	-	R	All 0's	Reserved
6	TXCRCAP	R/W	1	TXCRC Auto-Append When this bit is enabled, AX88780 will append CRC to the transmitted packet in FCS field. 1 = enable 0 = disable
5	-	R/W	0	Reserved.
4	TXCHKSUM	R/W	0	TX Checksum Generation When this bit is enabled, AX88780 will append checksum to the transmitted packet that is IP or TCP or UDP packet. 1 = enable 0 = disable
3:2	-	R	00	Reserved
1:0	TXDS	R	00	TX Description Status AX88780 reports which descriptor is transmitted now Default: 00

4.5 TX_CMD--TX Command Register

Offset Address = 0xFC14 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	HWI	R/W	0	Host Writes Indication Before host begins to send a packet to TX buffer, this bit should be set. At the end of host writes the packet, this bit should be cleared. 1 = Start Writing 0 = End Writing
14:13	TXDP	R/W	00	TX Descriptor Pointer To specify which TX descriptor to be written.
12	-	R/W	0	Reserved
11:0	DATALEN	R/W	All 0's	Byte Count. Data length is written to transmitted buffer.

4.6 TXBS--TX Buffer Status Register

Offset Address = 0xFC18 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:4	-	R	All 0's	Reserved
8	INTXDS	R	0	Internal TX descriptor status. This bit reports the TX descriptor status. When there is data to be transmitted, this bit will be set to '1' otherwise it will be '0' 1 = have data in TX buffer 0 = all data are transmitted to cable
7:6	-	R	00	Reserved
5:4	TXDUSE	R	00	TX Descriptor In Transmitting These status bits indicate which descriptor is transmitting now. 00: Descriptor 0 in transmitting 01: Descriptor 1 in transmitting 10: Descriptor 2 in transmitting 11: Descriptor 3 in transmitting
3	TXD3O	R/W	0	TX Descriptor 3 Occupied Driver set this bit to '1' to indicate that it had used TX descriptor3. When the

				transmission is finished, AX88780 will auto-clear this bit.
2	TXD2O	R/W	0	TX Descriptor 2 Occupied Driver set this bit to '1' to indicate that it had used TX descriptor2. When the transmission is finished, AX88780 will auto-clear this bit.
1	TXD1O	R/W	0	TX Descriptor 1 Occupied Driver set this bit to '1' to indicate that it had used TX descriptor1. When the transmission is finished, AX88780 will auto-clear this bit.
0	TXD0O	R/W	0	TX Descriptor 0 Occupied Driver set this bit to '1' to indicate that it had used TX descriptor0. When the transmission is finished, AX88780 will auto-clear this bit.

4.7 PHY_CTRL-- Internal PHY Control Register

Offset Address = 0xFC1C Default = 0x0000_0000

Field	Name	Type	Default	Description
31:13	-	R	All 0's	Reserved
12	SPD_GPIO1	R/W	0	Speed LED or GPIO1 When this bit is enabled, pin54 is as speed indicator, otherwise it is as GPIO1 function and controlled by GPIO_CTRL register. 1= enable 0= disable
11	LNK_GPIO0	R/W	0	Link LED or GPIO0 When this bit is enabled, pin55 is as link/traffic indicator, otherwise it is as GPIO0 function and controlled by GPIO_CTRL register. 1 = enable 0 = disable
10	FUL_EECS	R/W	0	EECS Pin as Full-Duplex LED When this bit is enabled, EECS pin will be as full-duplex indicator and EEDI pin will be as collision indicator. 1 = enable 0 = disable
9	PWDN	R/W	0	Power down PHY When this bit is enabled, AX88780 will turn off (disable) internal PHY. 1 = enable 0 = disable
8	PHY_EN	R/W	0	PHY Selection When this bit is enabled, AX88780 will select internal PHY, otherwise it will select external PHY. 1 = enable 0 = disable
7	-	R	0	Reserved
6:4	PHYOPMODE	R/W	000	Internal 10/100M PHY operation mode Driver can set these bits to control internal PHY operation mode. 000 = auto-negotiation enable with all capability 001 = auto-negotiation with 100BASE-TX FDX/HDX ability 010 = auto-negotiation with 10BASE-T FDX/HDX ability 011 = Reserved 100 = Manual selection of 100BASE-TX FDX 101 = Manual selection of 100BASE-TX HDX 110 = Manual selection of 10BASE-T FDX 111 = Manual selection of 10BASE-T HDX
3:1	-	R	000	Reserved
0	-	R/W	0	Reserved, must to be 0

4.8 TXDES0--TX Descriptor0 Register

Offset Address = 0xFC20 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD0_EN	R/W	0	Transmit TX descriptor 0 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, data had been written to TX descriptor0. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD0_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88780 how many bytes will be transmitted.

4.9 TXDES1--TX Descriptor1 Register

Offset Address = 0xFC24 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD1_EN	R/W	0	Transmit TX descriptor 1 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, data had been written to TX descriptor1. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD1_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88780 how many bytes will be transmitted.

4.10 TXDES2--TX Descriptor2 Register

Offset Address = 0xFC28 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD2_EN	R/W	0	Transmit TX descriptor 2 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, data had been written to TX descriptor2. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD2_LEN	R/W	All 0's	TX packet length (unit: byte) Driver set this field to indicate AX88780 how many bytes will be transmitted.

4.11 TXDES3--TX Descriptor3 Register

Offset Address = 0xFC2C Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	TXD3_EN	R/W	0	Transmit TX descriptor 3 If this bit is enabled, MAC will begin to transmit data that are stored in TX buffer. In former, data had been written to TX descriptor3. This bit will be cleared by hardware when MAC finished the transmission. 1= enable 0= disable
14:13	-	R	00	Reserved
12:0	TXD3_LEN	R/W	All 0's	TX Packet Length (unit: byte) Driver set this field to indicate AX88780 how many bytes will be transmitted.

4.12 RX_CFG--RX Configuration Register

Offset Address = 0xFC30h Default = 0x0000_0101

Field	Name	Type	Default	Description
31:9	-	R	All 0's	Reserved
8	RXBME	R/W	1	RX Buffer Monitor Enable When this bit is enable, MAC will monitor the status of the receive buffer. 1 = enable 0 = disable
7:5	-	R/W	000	Reserved.
4	RXCHKSUM	R/W	0	RX Packet TCP/IP Checksum When this bit is set, AX88780 will check the checksum of the received packet that is IP, TCP or UDP packet. If there is checksum error, AX88780 will drop the packet and RXCHKSUMCNT counter will add 1. 1 = enable 0 = disable
3:1	-	R/W	000	Reserved
0	RXBUFPRO	R/W	1	RX Buffer Protection When this bit is enabled, MAC will protect the RX buffer to avoid overrun. For normal operation, this bit should be enabled in initial stage. 1= enable 0= disable

4.13 RXCURT--RX Current Pointer Register

Offset Address = 0xFC34 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXCURPTR	R/W	All 0's	RX Line Current Pointer. Point to the last line that will be written by hardware. The unit of line is 16 bytes. MAC will maintain this register.

4.14 RXBOUND--RX Boundary Pointer Register

Offset Address = 0xFC38 Default = 0x0000_07FF

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXBUNPTR	R/W	0x7FF	RX Line Boundary Pointer. Point to the last line that has been read by driver. The unit of line is 16 bytes. When driver finished reading packet from RX buffer, it must update this field.

4.15 MAC_CFG0--MAC Configuration0 Register

Offset Address = 0xFC40 Default = 0x0000_8157

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	SPEED100	R/W	1	Line Speed Mode When this bit is enabled, The MAC of AX88780 will operate in 100M speed, otherwise it will operate in 10M speed. The line speed must co-operate with setting of PHY. 1 = 100M 0 = 10M
14	-	R/W	0	Reserved, this bit must set to 0 for normal operation
13	-	R/W	0	Reserved, this bit must set to 0 for normal operation.
12	RXFLOW	R/W	0	RX Flow Control If this bit and bit8 of RX_CFG are enabled, MAC will perform flow control and send pause on/off frame when the available space of receive buffer is less than the value of RXBTHD0. 1 = enable 0 = disable
11	-	R/W	0	Reserved, this bit must set to 0 for normal operation.
10:4	IPGT	R/W	0x15	Inter Packet Gap time: (IPG) This field defines the back-to-back transmit packet gap for 10/100M only.
3:0	-	R/W	0x7	Reserved, keep the default value for normal operation.

4.16 MAC_CFG1--MAC Configuration1 Register

Offset Address = 0xFC44 Default = 0x0000_6000

Field	Name	Type	Default	Description
31:15	-	R	All 0's	Reserved
14	PUSRULE	R/W	1	Pause Frame Check Rule When this bit is set, AX88780 accepts pause frame that DA can be any value. 1 = don't check DA field. 0 = check DA is equal to "01 80 C2 00 00 01"
13	CRCCHK	R/W	1	Check CRC of received Packet. When this bit is enabled, AX88780 will drop any CRC error packet. 1 = enable 0 = disable
12:7	-	R/W	All 0's	Reserved, keep all bits in '0' for normal operation.
6	DUPLEX	R/W	0	Duplex Mode. 1 = Full-Duplex mode 0 = Half-Duplex mode
5	TXFLW_EN	R/W	0	TX Flow Enable When this bit is enabled, MAC will block the transmitted operation when it captures pause frame from Ethernet. The re-transmission will be activated

				until the waiting time is expired. 1 = enable 0 = disable
4:1	-	R/W	0000	Reserved, must set to '0s' for normal operation
0	-	R/W	0	Reserved, must set to '0s' for normal operation

4.17 MAC_CFG2--MAC Configuration2 Register

Offset Address = 0xFC48 Default = 0x0000_0100

Field	Name	Type	Default	Description
15:8	-	R/W	0x01	Reserved, keep this field in default value for normal operation.
7:2	JamLT	R/W	000000	Define Jam Limit for backpressure collision account. Normally set this field at 0x19. It can avoid HUB port going to partition state due to too many collisions. AX88780 will skip one frame collision backpressure when collision counter equal to JamLT. The collision count will be reset to zero when every transmit frame with no collision or receive a frame with no backpressure collision.
1:0	-	R/W	00	Reserved, must set to '00' for normal operation

4.18 MAC_CFG3--MAC Configuration3 Register

Offset Address = 0xFC4C Default = 0x0000_060E

Field	Name	Type	Default	Description
15	NOABORT	R/W	0	No Abort When this bit is enabled, MAC will keep retry transmit current frame even excessive collision otherwise it will abort current transmission due to excessive collision. 1 = enable 0 = disable
13:7	IPGR1	R/W	0001100	Inter-Frame Gap segment1
6:0	IPGR2	R/W	0001110	Inter-Frame Gap segment2

4.19 TXPAUT--TX Pause Time Register

Offset Address= 0xFC54 Default = 0x001F_E000

Field	Name	Type	Default	Description
31:23	-	R		Reserved
22:0	TXPVAL	R/W	0x1F_E000	TX Pause Time out It is used to re-transmit a pause-on frame when pause timer expired and receive buffer still not enough. In 32-bit mode, this field should be set to 0x7F_8000. In 16-bit mode, this field should be set to 0xFFFF at 10/100Mbps modes. (Note: The bit 16 ~ 22 of this field are invalid in 16-bit mode.)

4.20 RXBTHD0--RX buffer Threshold0 Register

Offset Address= 0xFC58 Default = 0x0000_0300

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXLOWB	R/W	0x300	RX Remainder Capacity Low-Bound This field defines as the remainder capacity of RX buffer for pause operation. If the flow control (bit12 of MACCFG0) is enabled, MAC will send pause frame when the available space of receive buffer is less than this value. The unit is 16-byte.

4.21 RXBTHD1--RX Buffer Threshold1 Register

Offset Address= 0xFC5C Default = 0x0000_0600

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXHIGHB	R/W	0x600	RX Remainder Capacity Upper-Bound This field defines as upper bound of remainder size of RX buffer for pause operation. If the flow control is enabled, MAC will stop to send pause frame until the available space of receive buffer is more than this value. The unit is 16-byte.

4.22 RXFULTHD--RX Buffer Full Threshold Register

Offset Address= 0xFC60 Default = 0x0000_0100

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXFULB	R/W	0x100	RX Full Threshold This field defines the least capacity of RX buffer. AX88780 will cause RX full if it remains capacity less than this value. The unit is 16-byte.

4.23 MISC—Misc. Control Register

Offset Address= 0xFC68 Default = 0x0000_0013

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	WAKE_LNK	R/W	0	WAKE-UP by Link-Up Function If this bit is enabled, MAC will drive wakeup pin whenever there is link-up occurrence. The polarity of wakeup pin is according to bit0 of CMD register. 1= enable 0= disable
4	WAKE_MAG	R/W	1	WAKE-UP by Magic Packet If this bit is enabled, MAC will drive wakeup pin whenever there is magic packet detected by hardware. The polarity of wakeup pin is according to bit0 of CMD register. 1= enable wake-up by magic packet 0 = disable
3:2	-	R/W	00	Reserved
1	SRST_PHY	R/W	1	Software Reset Internal PHY Driver set this bit to '0' to reset internal PHY. The reset duration is depended on whenever this bit is de-asserted by deriver. 1 = in normal operation 0 = in reset status
0	SRST_MAC	R/W	1	Software Reset MAC Driver set this bit to '0' to reset MAC. The reset duration is depended on whenever this bit is de-asserted by deriver. After power-on, driver must activate software reset MAC once before initial other registers. 1 = in normal operation 0 = in reset status

4.24 MACID0--MAC ID0 Register

Offset Address = 0xFC70h Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID15_0	R/W	0x0000	MAC ID Address [15:0]. This field defines lower address bit15 to bit0 of MAC. The MACID0, MACID1 and MACID2 combine into 48-bit MAC address. The MAC address format is [47:0] = {MACID2[15:0], MACID1[15:0], MACID0[15:0]}. If the EEPROM is attached, this field will be auto-loaded from EEPROM after hardware reset.

4.25 MACID1--MAC ID1 Register

Offset Address = 0xFC74 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID31_16	R/W	0x0000	MAC ID Address [31:16].

4.26 MACID2--MAC ID2 Register

Offset Address = 0xFC78h Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved.
15:0	MID47_32	R/W	0x0000	MAC ID Address [47:32].

4.27 TXLEN--TX Length Register

Offset Address = 0xFC7C Default = 0x0000_05FC

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	MAXTXLEN	R/W	0x5FC	Max TX packet size This field defines the maximum raw packet size in transmittance. It is not included 4 bytes FCS.

4.28 RXFILTER--RX Packet Filter Register

Offset Address = 0xFC80 Default = 0x0000_0004

Field	Name	Type	Default	Description
31:6	-	R	All 0's	Reserved
5	GOODCRC	R/W	0	Good CRC enable When this bit is enabled, AX88780 will receive any packet of good CRC. 1 = enable 0 = disable
4	MULTI_HASH	R/W	0	Receive Multicast packet by lookup hash table. When this is enabled, AX88780 will receive multicast packet by the hash mapping function. It will refer to HASTAB0, HASHTAB1, HASHTAB2 and HASHTAB3 to look up the table. 1 = enable 0 = disable
3	BROADCAST	R/W	0	Receive Broadcast packet When this bit is enabled, AX88780 will receive the broadcast packet 1 = enable

				0 = disable
2	UNICAST	R/W	1	Receive Directed Packet. If this bit is enabled, AX88780 will compare the destination address field of received packet with the address of MAC (refer to MACID0, MACID1, MACID2). When it is matched and good CRC, the packet will be passed to driver. Otherwise it will be dropped. 1 = enable 0 = disable
1	MULTICAST	R/W	0	Receive all Multicast Packets. If this bit is enabled, any multicast packet (good CRC) will be received and passed to driver. 1 = enable 0 = disable
0	RXANY	R/W	0	Receive Anything. If this bit is enabled, any packet whether it is good or fail will be received and passed to driver. 1 = enable 0 = disable

4.29 MDIOCTRL--MDIO Control Register

Offset Address = 0xFC84 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	WTEN	R/W	0	Write Enable. Driver enables this bit to issue a write cycle to PHY, it will be cleared when finished the write cycle 1 = enable 0 = disable
14	RDEN	R/W	0	Read Enable. Driver enables this bit to issue a read cycle to PHY. This bit will be cleared when finished the read cycle 1 = enable 0 = disable
12:8	PHYCRIDX	R/W	00000	PHY Register Index If driver wants to access PHY, set this field to define the internal register index of PHY.
7:5	-	R	000	Reserved
4:0	PHYID	R/W	00000	PHY ID If driver wants to access PHY, set this field to define the address (ID) of PHY. The address of internal PHY is fixed to 0x10

4.30 MDIODP--MDIO Data Port Register

Offset Address = 0xFC88 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	MDPORT	R/W	All 0's	PHY Data Port To or from internal PHY data is put in this field.

4.31 GPIO_CTRL--GPIO Control Register

Offset Address = 0xFC8C Default = 0x0000_0003

Field	Name	Type	Default	Description
31:10	-	R	All 0's	Reserved
9	GPIO1S	R/W	0	GPIO1 Status This bit stands for the pin status of GPIO1 when it is set to input mode. 1 = high state 0 = low state
8	GPIO0S	R/W	0	GPIO0 Status This bit stands for the pin status of GPIO0 when it is set to input mode. 1 = high state 0 = low state
7:2	-	R	All 0's	Reserved
1	GPIO1DIR	R/W	1	GPIO1 Mode Direction This field defines the direction of GPIO1 pin. 1 = input mode 0 = output mode
0	GPIO0DIR	R/W	1	GPIO0 Mode Direction This field defines the direction of GPIO pin. 1 = input mode 0 = output mode

Note: For output mode, software must firstly set the bit0 or bit1 to output mode then set bit8 or bit9.

4.32 RXINDICATOR--Receive Indicator Register

Offset Address= 0xFC90 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:1	-	R	All 0's	Reserved
0	RXSTART	R/W	0	Receive Start Driver set this bit to start or end receive operation from RX buffer of MAC. 1= Start read RX buffer 0= End read RX buffer

4.33 TXST--TX Status Register

Offset Address = 0xFC94 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:4	-	R	All 0's	Reserved
3	TXD3FAIL	R	0	TX Descriptor3 Transmit Fail When this bit is set 1, it means MAC fails in transmission of descriptor 3. This bit will be self-cleared when driver reads TXST register.
2	TXD2FAIL	R	0	TX Descriptor2 Transmit Fail When this bit is set 1, it means MAC fails in transmission of descriptor 2. This bit will be self-cleared when driver reads TXST register.
1	TXD1FAIL	R	0	TX Descriptor1 Transmit Fail When this bit is set 1, it means MAC fails in transmission of descriptor 1. This bit will be self-cleared when driver reads TXST register.
0	TXD0FAIL	R	0	TX Descriptor0 Transmit Fail When this bit is set 1, it means MAC fails in transmission of descriptor 0. This bit will be self-cleared when driver reads TXST register.

4.34 MDCLKPAT--MDC Clock Pattern Register

Offset Address = 0xFCA0 Default = 0x0000_8040

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:8	-	R/W	0x80	Reserved, must set to 0x80 for normal operation
7:0	MDCPAT	R/W	0x40	MDC Clock Divide Factor This field defines the divide factor of host clock. AX88780 will refer to this field and generate a low speed clock to PHY.

4.35 RXCHKSUMCNT--RX IP/UDP/TCP Checksum Error Counter

Offset Address = 0xFCA4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	RXCHKERCNT	R/W	All 0's	RX Checksum Error Counter If the RXCHKSUM field of RX_CFG register is set to '1', MAC will check the checksum of IP, TCP or UDP packet. Whenever there is checksum error detected, this field will be added one. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.36 RXCRCNT--RX CRC Error Counter

Offset Address = 0xFCA8 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	RXCRCCNT	R/W	All 0's	RX CRC32 Error Counter MAC checks the received packet. If there is a CRC error detect, this field will be added one. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.37 TXFAILCNT--TX Fail Counter

Offset Address = 0xFCAC Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	TXFILCNT	R/W	All 0's	TX Fail Counter This field records the number of transmitted error for TX packet. The value will be rounded back to 0x0000 if it exceeds 0xFFFF.

4.38 PROMDPR--EEPROM Data Port Register

Offset Address = 0xFCB0h Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	PROMDP	R/W	All 0's	EEPROM Data Port The data to or from EEPROM is set in this field.

4.39 PROMCTRL--EEPROM Control Register

Offset Address= 0xFCB4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:15	-	R	All 0's	Reserved
14:12	ROM_CMD	R/W	000	EEPROM Command Code. Driver set this field to represent what type command will be send to EEPROM device. 110 = read command 111 = erase command 101 = write command
11	ROM_WT	R/W	0	Write EEPROM Set to '1' to write EEPROM, it will be cleared when MAC finished the write operation.
10	ROM_RD	R/W	0	Read EEPROM Set to '1' to read EEPROM, it will be cleared when MAC finished the read operation. Driver can read PROMDPR register to get the returned data.
9	ROM_RLD	R/W	0	Reload EEPROM Set to '1' to re-load EEPROM, this bit will be cleared when MAC finished loading operation.
8	-	R	0	Reserved
7:0	ROM_ADDR	R/W	0x00	EEPROM Address Set this field to define the address for serial EEPROM access. (only support 16-bit data access, 93C56 type)

4.40 MAXRXLEN--Max. RX Packet Length Register

Offset Address= 0xFCB8 Default = 0x0000_0600

Field	Name	Type	Default	Description
31:11	-	R	All 0's	Reserved
10:0	RXLEN	R/W	0x600	Max RX Packet length This field defines the max length of received packet. It doesn't include 4-byte CRC.

4.41 HASHTAB0--Hash Table0 Register

Offset Address = 0xFCC0 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB0	R/W	0x0000	Hash table: bit15~bit0 Driver sets HASHTAB0, HASHTAB1, HASHTAB2 and HASHTAB3 to define 64-bit hash table. AX88780 will refer this table to check multicast packet if multicast filter is enabled for RX. When AX88780 receives a packet then it extracts the destination address (DA). The DA is calculated by CRC32 algorithm. After the operation, AX88780 will grab the MSB[31:27] of result as hash table index. The range of index is from 0 to 63. For example, the hash table is composite as {HASHTAB3[15:0], HASHTAB2[15:0], HASHTAB1[15:0], HASHTAB0[15:0]}. If AX88780 detects the MSB[31:27] = 26 of CRC32 of DA for someone multicast packet, and driver set '1' to HASHTAB1[10], then the multicast packet will received by AX88780.

4.42 HASHTAB1--Hash Table1 Register

Offset Address = 0xFCC4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB1	R/W	0x0000	Hash table: bit31~bit16

4.43 HASHTAB2--Hash Table2 Register

Offset Address = 0xFCC8 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB2	R/W	0x0000	Hash table: bit47~bit32

4.44 HASHTAB3--Hash Table3 Register

Offset Address = 0xFCCC Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	HTAB3	R/W	0x0000	Hash table: bit63 ~ bit48

4.45 DOGTHD0—Watch Dog Timer Threshold0 Register

Offset Address = 0xFCE0 Default = 0x0000_FFFF

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15:0	DOGTH0	R/W	0xFFFF	Watch Dog Timer Low Word This register and DOGTHD1[11:0] are defined to an expired threshold for internal watchdog counter. The threshold {[DOGTHD1, DOGTHD0] is a 28-bit value. To multiply 28-bit value with one-cycle period of a host clock is the expired duration. If the DOGEN is set to '1' and WDTEI of ISR is set, then AX88780 will periodically generate interrupt whenever the counter reaches to the threshold.

4.46 DOGTHD1—Watch Dog timer Threshold1 Register

Offset Address = 0xFCE4 Default = 0x0000_0000

Field	Name	Type	Default	Description
31:16	-	R	All 0's	Reserved
15	DOGEN	R/W	0	Dog Timer Enable 1 = Enable internal dog timer
14:12	-	R/W	All 0s	Reserved
11:0	DOGTH1	R/W	0x000	Dog Timer High Byte. This filed and DOGTHD0[15:0] combine to a 28-bit register.

4.47 SOFTRST – Software reset Register

Offset Address = 0xFCEC Default = 0x0000_0003

Field	Name	Type	Default	Description
31:2	-	R	All 0's	Reserved
1	RST_PHY	R/W	1	Reset Internal PHY Driver set this bit to '0' to reset internal PHY. The reset duration is depended on whenever this bit is de-asserted by driver. All registers of PHY will be clean to default value. 1 = in normal operation 0 = in reset status
0	RST_MAC	R/W	1	Reset MAC Driver set this bit to '0' to reset MAC. The reset duration is depended on whenever this bit is de-asserted by driver. Most registers of MAC will be clear to default value. 1 = in normal operation 0 = in reset status

5.0 PHY Register

AX88780 is built a high performance 10/100M PHY for cost-effective. Driver can access these registers of PHY by in-directed mechanism. For write operation, software firstly sets data to MDIODP register, then sets index and write enable bit to MDIOCTRL register. AX88780 will access PHY by internal interface and clear the write enable bit whenever the operation finished. For read operation, driver sets the index and read enable bit to MDIOCTRL register, then polls the read-enable bit. The returned data will be put in MDIODP register whenever the read-enable bit is cleared.

Table 9 : PHY Register Mapping

Index	Name	Description
0x00	BMCR	Basic Mode Control Register
0x01	BMSR	Basic Mode Status Register
0x02	PHYIDR0	PHY Identifier 0 Register
0x03	PHYIDR1	PHY Identifier 1 Register
0x04	ANAR	Auto-negotiation Advertisement Register
0x05	ANLPAR	Auto-negotiation Link Partner Ability Register
0x06	ANER	Auto-negotiation Expansion Register

The following abbreviations apply to below sections for detained register description.

Access type
R = read only
RW= read/write

Attribute:
LL = latch low
LH = latch high
SC = Self-clearing
PS = Value is permanently set
X = don't care

5.1 BMCR--Basic Mode Control Register

Index = 0x00

Field	Name	Type	Default	Description
15	PHYRST	R/W	0, SC	Soft reset: 1 = software reset PHY, this bit will be cleared when reset finish. 0 = normal operation
14	LOOPBACK	R/W	0	Loop back operation: 1 = Loop back enable 0 = Loop back disable
13	SPDSEL	R/W	1	Speed selection: 1 = 100Mb/s 0 = 10Mb/s
12	AUTONEG_EN	RW	1	Auto-negotiation enable: 1 = enable, bit8 and bit13 will be ignored when this bit is enabled. 0 = disable, bit8 and bit13 of this register determine the link speed and mode.
11	PHYPWDN	R/W	0	Power down: 1 = power-down enable 0 = normal operation
10	-	R	0	Reserved
9	AUTONEG_RS	R/W	0	Auto-negotiation restart: 1=Restart auto-negotiation, this bit will be cleared when finish negotiation. 0=normal operation
8	DPLX	R/W	1	Duplex mode:

				1=Full-duplex operation 0= Normal operation
7	COLTST	R/W	0	Collision test: 1=Enable collision test 0= Normal operation
6:0	-	R	X	Reserved

5.2 BMSR--Basic Mode Status Register

Index = 0x01

Field	Name	Type	Default	Description
15	100BCAP	R	0, PS	100Base-T4 capability 0 = AX88780 is not able to execute 100 BASE-T4 mode.
14	100BFUL	R	1, PS	100BASE-TX full-duplex capability: 1= AX88780 is able to perform in 100BASE-TX full-duplex mode.
13	100BHAF	R	1, PS	100BASE-TX half-duplex capability: 1 = AX88780 is able to perform in 100BASE-TX half-duplex mode.
12	10BFUL	R	1, PS	10BASE-T full-duplex capability: 1 = AX88780 is able to perform in 10BASE-T full-duplex mode.
11	10BHAF	R	1, PS	10BASE-T half-duplex capability: 1 = AX88780 is able to perform in 10BASE-T half-duplex mode.
10:7	-	R	All 0's	Reserved, default 4'b0000
6	MFPS	R	0, PS	Management frame preamble suppression: 0 = AX88780 will not accept management frames with preamble suppressed.
5	AUTONEST	R	0	Auto negotiation completion: 1 = auto-negotiation process is complete. 0 = auto-negotiation process is not completed
4	RFST	RC	0, LH	Remote fault status: 1 = The link partner signals a far-end fault, read to clear. 0 = Remote fault condition is not detected
3	AUTOCFG	R	1, PS	Auto configuration ability: 1 = AX88780 is able to perform auto-negotiation
2	LNKST	R	0, LL	Link status: 1= Valid link is established, (100Mb/s or 10Mb/s operation) 0= Valid link is not established
1	JABDET	R	0, LH	Jabber detection: 1= Jabber condition is detected. 0 = Jabber condition is not detected
0	EXTCAP	R	1, PS	Extended capability: 1= Extended register capable 0= Basic register capability only.

5.3 PHYIDR0--PHY Identifier 0 Register

Index = 0x02

Field	Name	Type	Default	Description
15:0	OUIMSB	R	0x003B PS	OUI most significant bits. Bits 3 to 18 of the OUI are mapped to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored

5.4 PHYIDR1--PHY Identifier 1 Register

Index = 0x03

Field	Name	Type	Default	Description	Default
15:10	OUILSB	R	000110	OUI lease significant bits.	0x1833
9:4	MANMODE	R	000011	Manufacture's mode number	PS
3:0	RECNUM	R	0011	Revision number 0001 for version 2 0011 for version 3	

5.5 ANAR--Auto-negotiation Advertisement Register

Index = 0x04

Field	Name	Type	Default	Description
15	NXTP	R	0, PS	Next page indication: Not support
14	-	R	0	Reserved
13	-	R	0	Remote fault: Not support fault condition detected.
12:11	-	R	X	Reserved
10	PF	R/W	0	Pause function: AX88780 does not support this function in PHY layer. The pause function will support with MAC operation.
9	100BSUP	R	0, PS	100BASE-T4 support: Not support
8	100BFULSUP	R/W	1	100BASE-TX full-duplex support: 1=enable 100BASE-TX full duplex 0=disable 100BASE-TX full-duplex
7	100BHAFSUP	R/W	1	100BASE-TX half-duplex support: 1=enable 100BASE-TX half-duplex 0=disable 100BASE-TX half-duplex.
6	10BFULSUP	R/W	1	10BASE-T full-duplex support: 1=enable 10BASE-T full-duplex 0=disable 10BASE-T full duplex.
5	10BHAFSUP	R/W	1	10BASE-T half-duplex support: 1=enable 10BASE-T half-duplex 0=disable 10BASE-T half-duplex.
4:0	PROSEL	R/W	00001	Protocol selection bits: AX88780 support IEEE 802.3u CSMA/CD.

5.6 ANLPAR--Auto-negotiation Link Partner Ability Register

Index = 0x05

Field	Name	Type	Default	Description
15	PNRNXT	R	0	Next page indication: 1= Link partner is next page enabled. 0= Link partner is not next page enabled
14	PNRACK	R	0	Acknowledgement: 1= Link partner ability for reception of data word is acknowledged 0= Link partner ability for reception of data word is not acknowledged.
13	PNRRF	R	0	Remote fault: (from link partner view) 1= Remote fault is indicated by link partner. 0= Remote fault is not indicated by link partner.
12:11	-	R	00	Reserved
10	PNRPAUS	R	0	Pause: 1= Pause operation is supported by link partner.

				0= Pause operation is not support by link partner.
9	PNR100B	R	0	100Base-T4 support: 1 = 100Base-T4 is supported by link partner. 0 = 100Base-T4 is not supported by link partner.
8	PNR100BFUL	R	0	100BASE-TX full-duplex support: 1 = 100BASE-T full-duplex is supported by link partner. 0 = 100BASE-TX full-duplex is not supported by link partner.
7	PNR100BHAF	R	0	100BASE-TX half-duplex support: 1 = 100BASE-TX half-duplex is supported by link partner. 0 = 100BASE-TX half-duplex is not supported by link partner.
6	PNR10BFUL	R	0	10BASE-T full-duplex support: 1 = 10BASE-T full-duplex is supported by link partner. 0 = 10BASE-T full-duplex is not supported by link partner.
5	PNR10BHAF	R	0	10BASE-T half-duplex support: 1 = 10BASE-T half-duplex is supported by link partner. 0 = 10BASE-T half-duplex is not supported by link partner.
4:0	PNRPROSEL	R	00000	Protocol selection bits: Link partner's binary encoded protocol selector.

5.7 ANER--Auto-negotiation Expansion Register

Index = 0x06

Field	Name	Type	Default	Description
15:5	-	R	All 0's	Reserved,
4	PARDETF	R	0, LH	Parallel detection fault: 1 = Fault is detected via parallel detection function 0 = Fault is not detected
3	LNKPNRNXT	R	0	Link partner next page enable: 1 = Link partner is next page enabled 0 = Link partner is not next page enabled.
2	PHYNXTPG	R	0, PS	PHY next page enable: 1 = PHY is next page enabled 0 = PHY is not next page enabled.
1	NPREC	R	0, LH	New page reception: 1 = New page is received 0 = New page is not received.
0	LNKPNRAN	R	0	Link partner auto-negotiation enable: 1 = Auto-negotiation is supported by link partner, 0 = Auto-negotiation is not supported by link partner.

6.0 Electrical Specification and Timings

6.1 DC Characteristics

6.1.1 Absolute Maximum Ratings

Symbol	Description	Rating	Units
T_{STG}	Storage Temperature	-40 to 150	°C
VCC3	Power supply of 3.3V	-0.3 to VCC3 + 0.3	V
VCC2	Power supply of 2.5V	-0.3 to VCC2 + 0.3	V
V_{I3}	Input voltage of 3.3V IO with 5V tolerance	-0.3 to 5.5	V
V_{I2}	Input voltage of 2.5V IO with 3.3V tolerance	-0.3 to 3.9	V

Note: Stress above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to Absolute Maximum Ratings conditions for extended period, adversely affect device life and reliability.

6.1.2 General Operation Conditions

Symbol	Description	Min	Typ	Max	Units
Tj	Junction temperature	0	-	115	°C
VCC2	Supply Voltage of 2.5V	2.25	2.5	2.75	V
VCC3	Supply Voltage of 3.3V	3.0	3.3	3.6	V
V_{I3}	Input voltage of 3.3V IO with 5V tolerance	0	3.3	5.25	V
V_{I2}	Input voltage of 2.5V IO with 3.3V tolerance	0	2.5	3.6	V

6.1.3 Leakage Current and Capacitance

Symbol	Description	Min	Typ	Max	Units
I_{IN}	Input Leakage Current	-10	±1	+10	μA
I_{OZ}	Tri-state leakage current	-10	±1	+10	μA
C_{OUT}	Output capacitance	-	3.1	-	pF
C_{BID}	Bi-directional buffer capacitance	-	3.1	-	pF

6.1.4 DC Characteristics of 2.5V IO Pins

Symbol	Description	Min	Typ	Max	Units
VCC2	Power supply of 2.5V IO	2.25	2.5	2.75	V
Vil	Input low voltage	-	-	0.7	V
Vih	Input high voltage	1.7	-	-	V
Vol	Output low voltage	-	-	0.4	V
Voh	Output high voltage	1.85			V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ

6.1.5 DC Characteristics of 3.3V IO Pins

Symbol	Description	Min	Typ	Max	Units
VCC3	Power supply of 3.3V IO	3.0	3.3	3.6	V
Vil	Input low voltage	-	-	0.8	V
Vih	Input high voltage	2.0	-	-	V
Vol	Output low voltage	-	-	0.4	V
Voh	Output high voltage	2.4			V
Rpu	Input pull-up resistance	40	75	190	KΩ
Rpd	Input pull-down resistance	40	75	190	KΩ

6.1.6 Transmission Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
Vpp	Peak-to-Peak differential output voltage	10BASE-T mode	4.5	5	5.5	V
2xVtxa	Peak-to-Peak differential output voltage, 2xVtxa	100BASE-TX	1.9	2	2.1	V
T_r/T_f	Signal rising/falling time	100BASE-TX	3	4	5	ns
T_{jit}	Output jitter	100BASE-TX			1.4	ns
Vtxov	Overshoot	100BASE-TX			5	%

6.1.7 Reception Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Units
R_{imp}	Reception impedance		5			KΩ
Vsqu	Differential squelch voltage	10BASE-TX	300	400	500	mV
Vcom	Common mode input voltage		1.2	1.6	2	V
L_{free}	Max error-free cable length		100			Meter

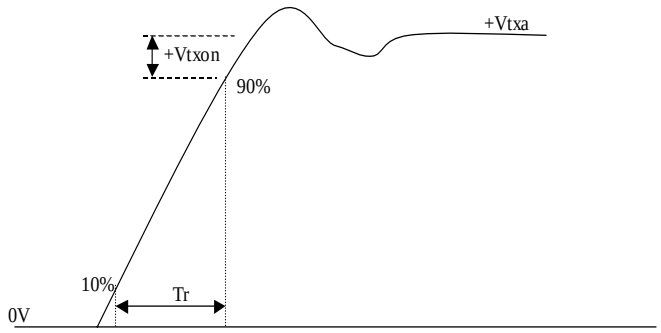


Figure 6: Transmit waveform specification

6.1.8 Power Consumption

Device Only

Measurement bases on 100MHz frequency of HCLK and turn on internal regulator at 25 °C temperature.

Item	Symbol	Power-On with cable removed	Operation at 10Base-T	Operation at 100Base-T	PHY power down	Stand-by current (HCLK is off)	Units
1	VCC3 (IO)	1.6	5.4	6.4	1.6	0.061	mA
2	VCC3R	103	86	97.5	64	1.5	mA

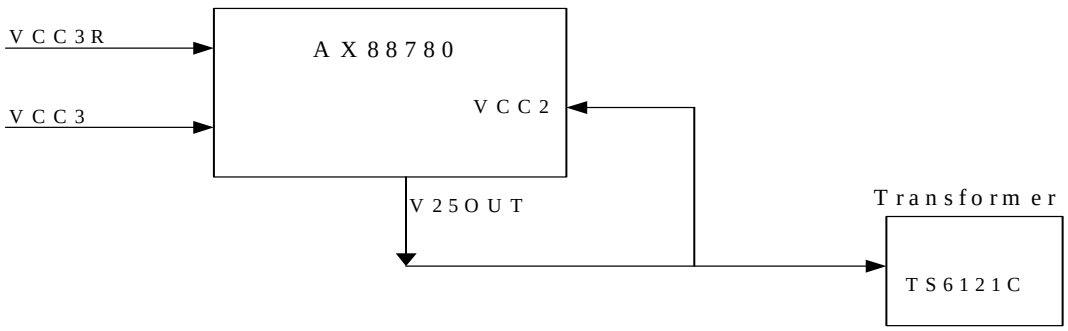
Note: The current of VCC3R includes VCC2 core current.

Device and system components

It is a total of Ethernet connectivity solution, which includes external component supporting the AX88780. The brief connection is shown as below.

Measurement bases on 100MHz frequency of HCLK and turn on internal regulator at 25 °C temperature.

Item	Test conditions	Total power	Units
1	10Base-T operation (**internal PHY sinks 140 mA)	619	mW
2	100Base-T operation (**internal PHY sinks 100 mA)	469	mW
3	Cable unplug	654	mW
4	PHY power down	315	mW



1. Enable regulator of AX88780
2. The 2.5V power of TS6121C is from AX88780

6.1.9 Thermal Characteristics

A. Junction to ambient thermal resistance, θ_{JA}

Symbol	Min	Typ	Max	Units
θ_{JA}	-	46.3	-	°C/W

B. Junction to case thermal resistance, θ_{JC}

Symbol	Min	Typ	Max	Units
θ_{JC}	-	16.2		°C/W

1: Note θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P}, \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature
T_A: ambient or environment temperature
T_C: the top center of compound surface temperature
P: input power (watts)

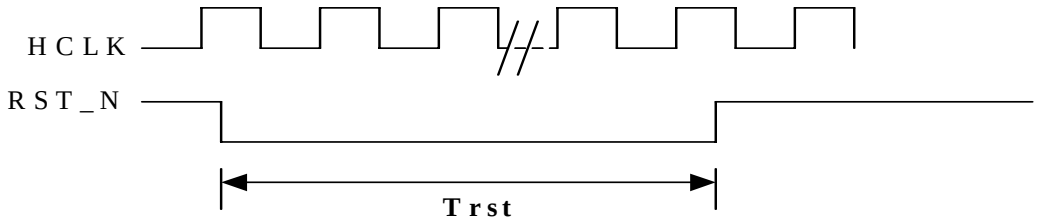
6.2 A.C. Timing Characteristics

6.2.1 Host Clock

Reference clock (HCLK)

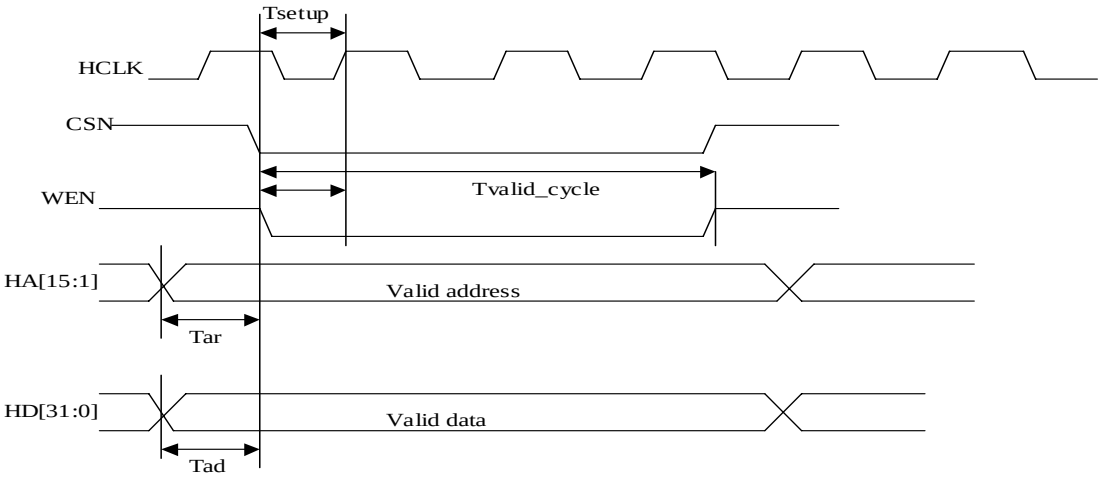
Description	Min	Typ.	Max	Units
Reference frequency	40	--	100	MHz
Reference clock duty cycle	40	50	60	%

6.2.2 Reset Timing



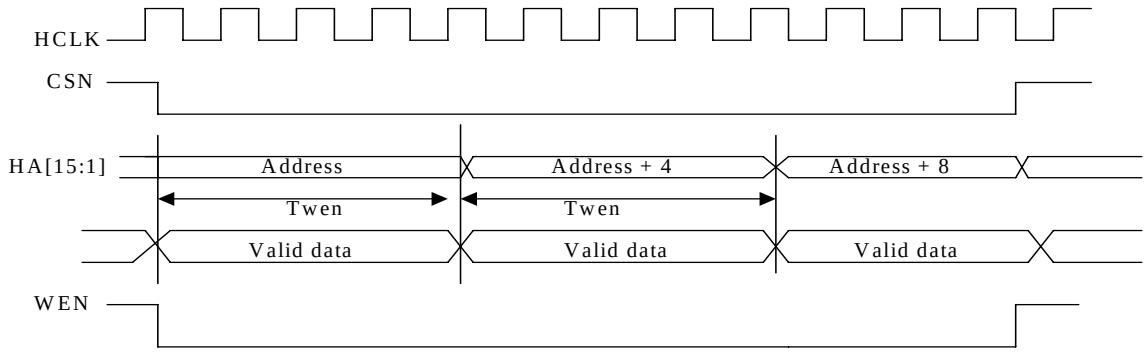
Symbol	Description	Min	Typ.	Max	Units
Trst	Reset pulse width	1	-	-	ms

6.2.3 Host Single Write Timing



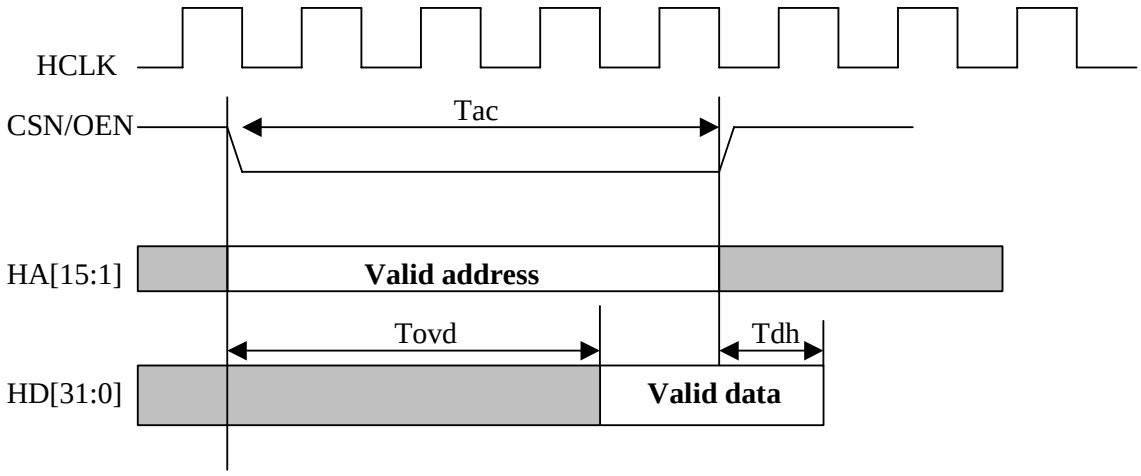
Symbol	Description	Min	Typ.	Max	Units
Tsetup	CSN, WEN to HCLK setup timing	2	-	-	ns
Tar	HA exceed to WEN timing	0			HCLK
Tad	HA exceed to WEN timing	0			HCLK
Tvalid_cycle	A Valid write cycle timing (synchronous to MCU)	4	-	-	HCLK
Tvalid_cycle	A Valid write cycle timing- (asynchronous to MCU)	6	-	-	HCLK

6.2.4 Host Burst Write Timing



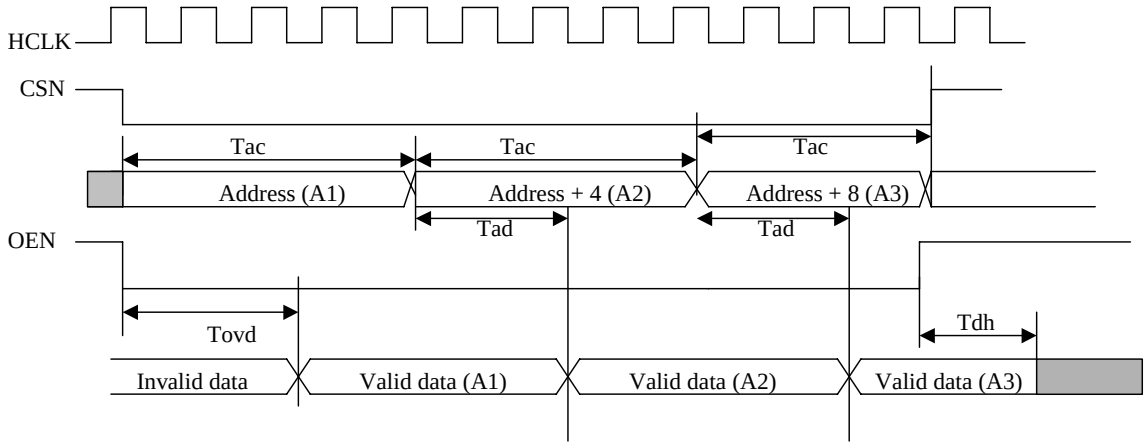
Symbol	Description	Min	Typ.	Max	Units
Twen	Valid write cycle timing	6	-	-	HCLK

6.2.5 Host Single Read Timing



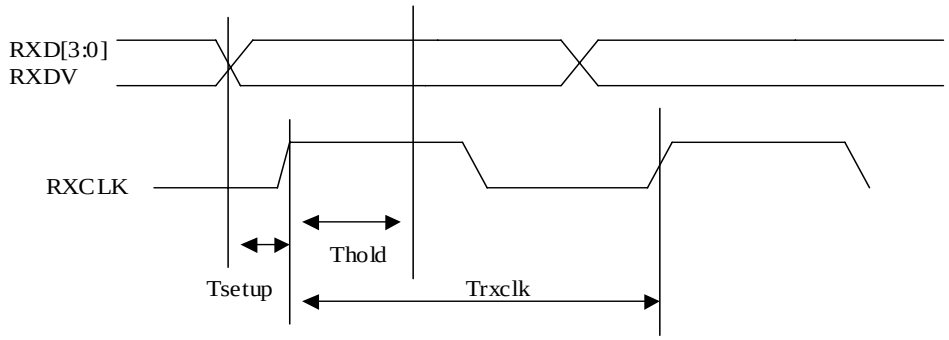
Symbol	Description	Min	Typ.	Max	Units
Tac	CSN/OEN access timing (synchronous to MCU)	5	-	-	HCLK
Tac	CSN/OEN access timing (asynchronous to MCU)	6			HCLK
Tovd	OEN assert to valid data timing	4	-	-	HCLK
Tdh	Valid data hold timing to OEN de-asserted	0			ns

6.2.6 Host Burst Read Timing



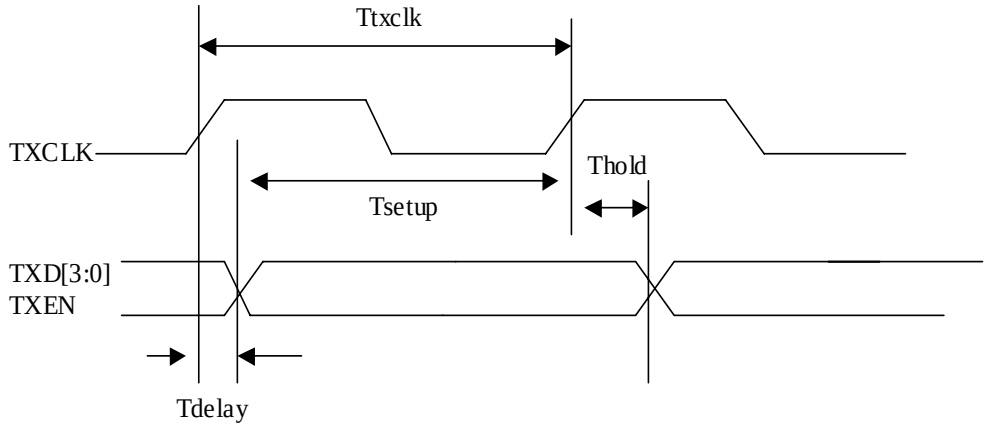
Symbol	Description	Min	Typ.	Max	Units
Tac	Valid address access timing	6			HCLK
Tovd	OEN assert to valid data timing	4	-	-	HCLK
Tad	Burst mode address to valid data	4			HCLK
Tdh	Valid data hold timing to OEN de-asserted	0			ns

6.2.7 MII Receive Timing (100Mb/s)



Symbol	Description	Min	Typ.	Max	Units
Trxclk	RXCLK clock cycle time*		40		ns
Tsetup	RXD[3:0] RXDV setup time for RXCLK	5	-	-	ns
Thold	RXD[3:0], RXDV hold timing for RXCLK	3	-	-	ns

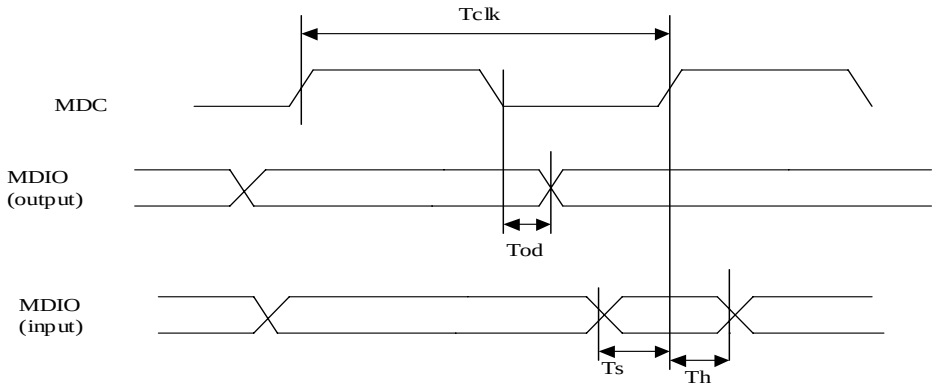
6.2.8 MII Transmit Timing (100Mbps)



Symbol	Description	Min	Typ.	Max	Units
Ttxclk	TXCLK reference clock*		40	-	ns
Tdelay	TXD[3:0], TXEN delay timing for TXCLK		-	10	ns
Tsetup	TXD[3:0], TXEN setup time	28			ns
Thold	TXD[3:0], TXEN hold time	5			ns

*Note: for 10Mbps, the typical value of Ttxclk shall scale to 400ns

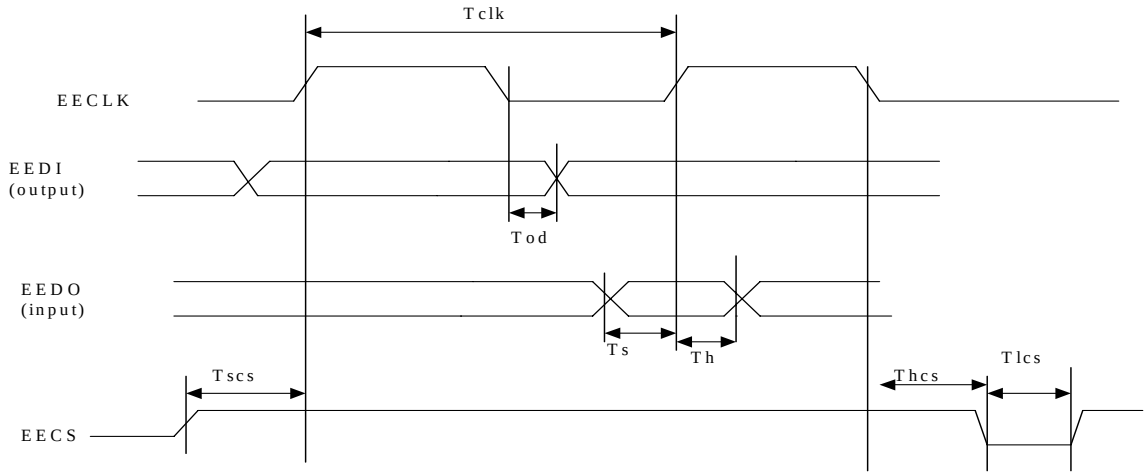
6.2.9 MDIO Timing



Symbol	Description	Min	Typ.	Max	Units
Tclk	MDC clock timing*		1340	-	ns
Tod	MDC falling edge to MDIO output delay		-	32	ns
Ts	MDIO data input setup timing	10	-	-	ns
Th	MDIO data input hold timing	4	-	-	ns

*Note: HCLK is 100MHz case.

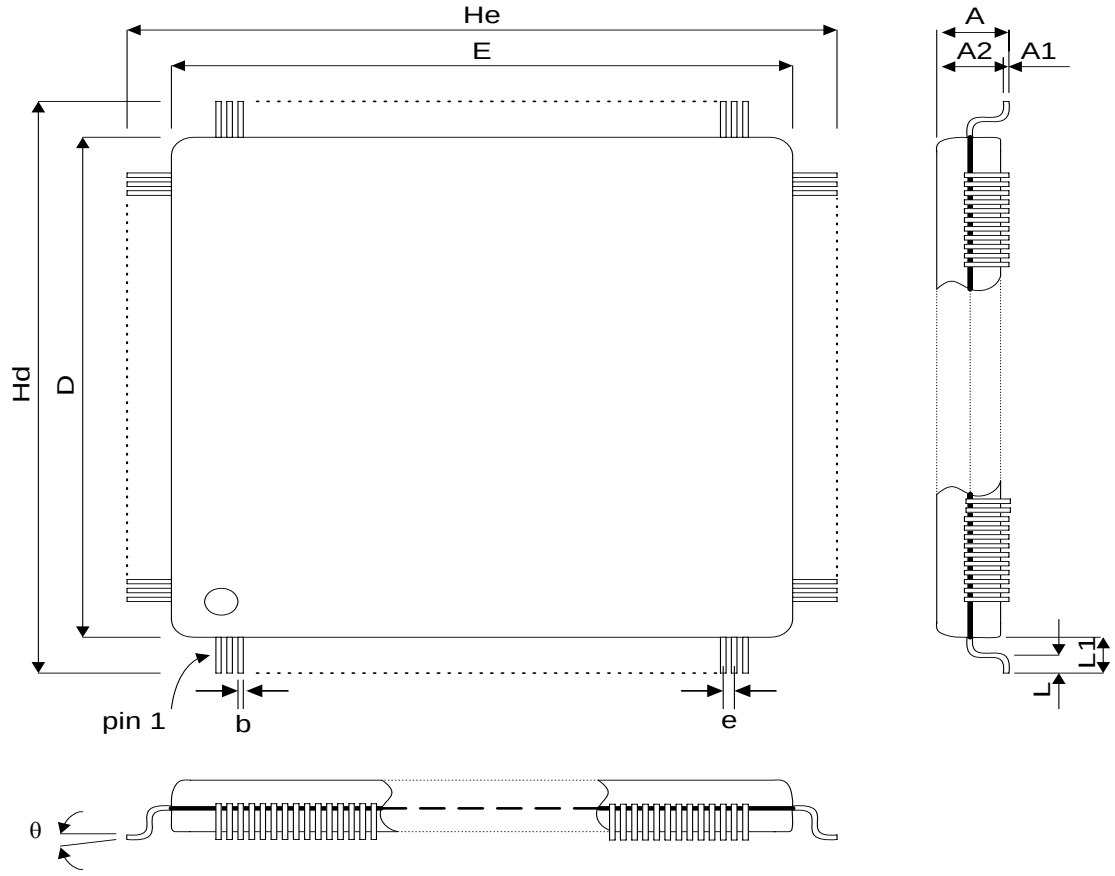
6.2.10 Serial EEPROM Timing



Symbol	Description	Min	Typ.	Max	Units
Tclk	EECLK clock timing*		1370	-	ns
Tod	EECLK falling edge to EEDI output delay		-	5	ns
Ts	EEDO data input setup timing	6	-	-	ns
Th	EEDO data input hold timing	6	-	-	ns
Tscs	EECS output valid to EECLK rising edge	650			ns
Thcs	EECLK falling edge to EECS invalid timing	0			ns
Tlcs	Minimum EECS low timing	-	560	-	ns

*Note: HCLK is 100MHz case.

7.0 Package Information



SYMBOL	MILIMETER		
	MIN.	NOM	MAX
A1	0.05	0.1	
A2	1.35	1.4	1.45
A			1.6
b	0.13	0.18	0.23
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e		0.40	
Hd	15.85	16.00	16.15
He	15.85	16.00	16.15
L	0.45	0.60	0.75
L1		1.00	
θ	0		7

8.0 Ordering Information

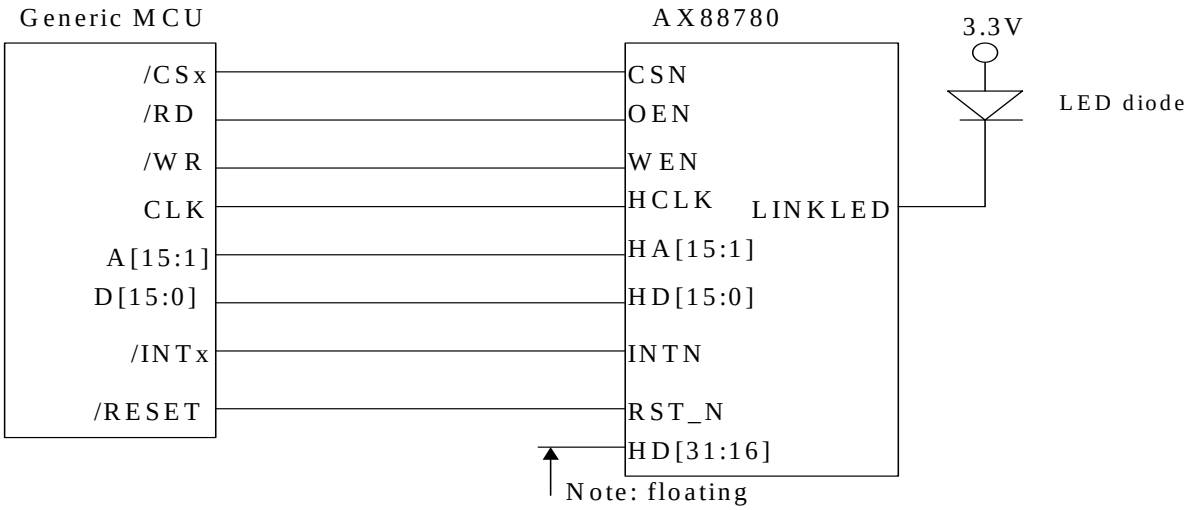
AX88780	L	F
Product name	Package LQFP	F: Lead Free

Appendix A1. 16-bit mode address and data bus

A1-1. 16-bit mode and separated address and data bus

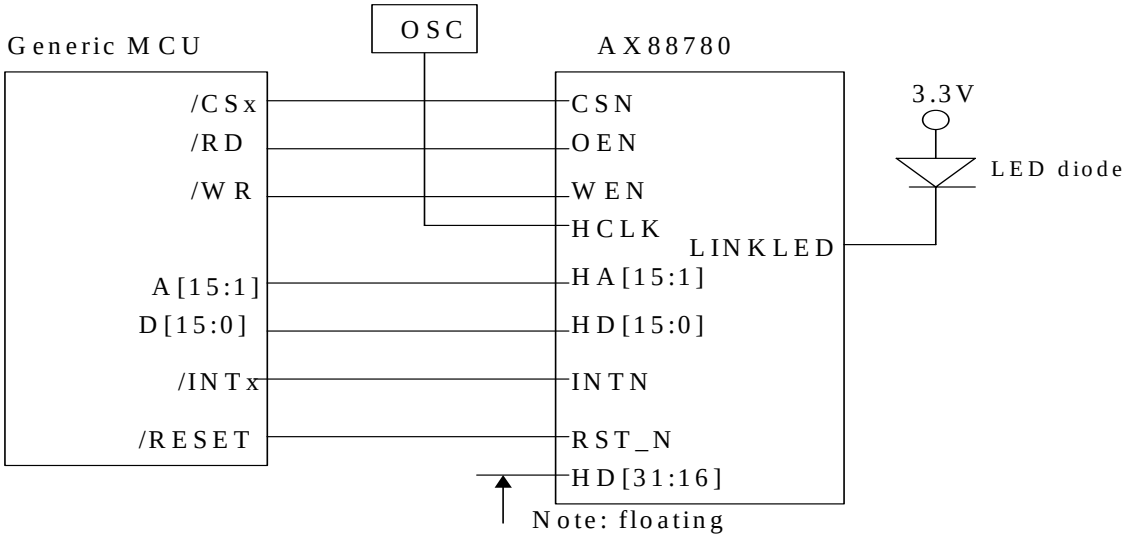
Note: The name of control signal for MCU is demonstrated only.

A1-1-1. AX88780 is synchronous to host MCU

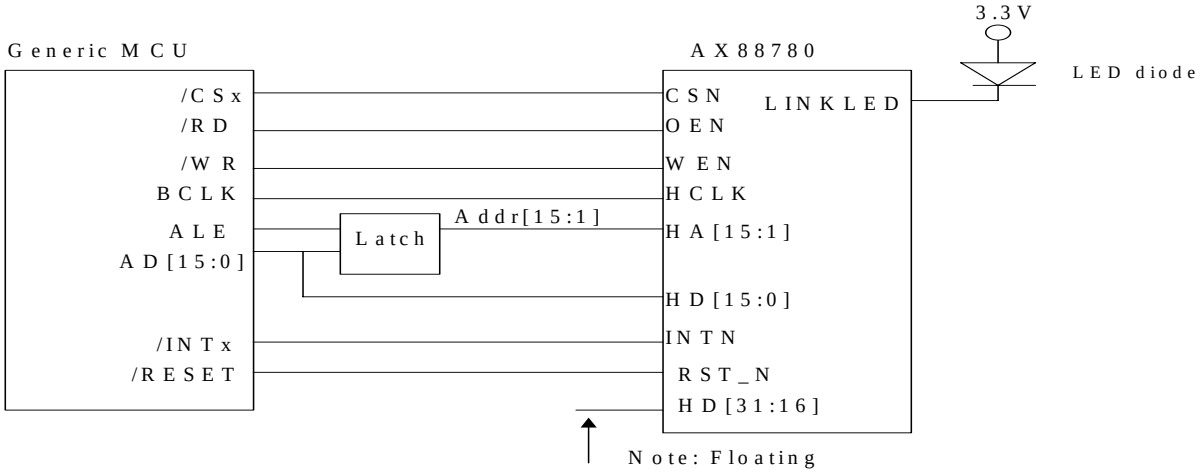


A1-1-2. AX88780 is asynchronous to host MCU

Note: For asynchronous mode, system must provide extra OSC to output clock to AX88780

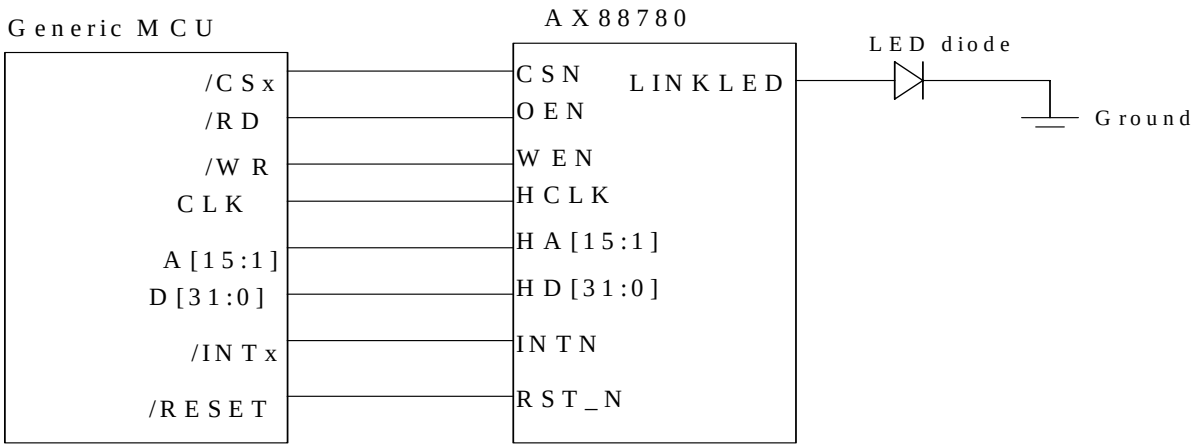


A1-2. 16-bit mode multiplexed address and data



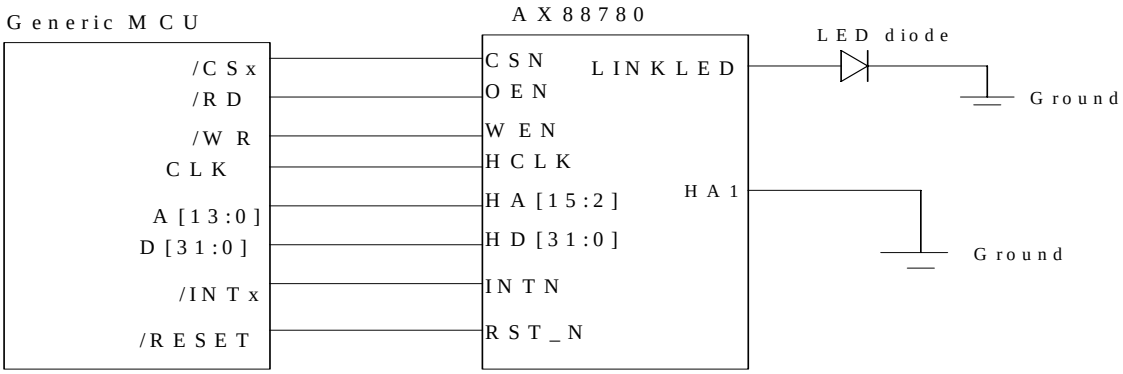
Appendix A2. 32-bit mode address and data bus

A2-1. Linear address mode and byte aligned (in synchronous mode)



Note: For asynchronous mode, system must provide extra OSC to output clock to AX88780. Please refer to Section A1-1-2 for details.

A2-2. MCU is double-word boundary and the addressing is DWORD unit



Appendix A3. Synchronous and asynchronous timing selection

AX88780 can support synchronous or asynchronous access from host MCU. Below information provides some references to select clock frequency of host MCU and AX88780.

A3-1. AX88780 is synchronous with host MCU.

The timing selection is suitable for both 32-bit and 16-bit mode.

Frequency	Access type	Valid access timing (OEN/WEN active timing)
Max 100MHz	Single or Burst	Min 5 clocks

A3-2. AX88780 is asynchronous to host MCU.

The timing selection is suitable for both 32-bit and 16-bit mode.

Frequency	Access type	Valid access timing (OEN/WEN active timing)
Max 100MHz	Single or Burst	Min 6 reference clocks (Note)

Note: The reference clock is from OSC, and it's not the output of host MCU. For instance, if AX88780 runs in asynchronous mode and refers a 100MHz clock from OSC, whereas MCU runs in 125Mhz environment. In such condition, MCU must at least offer 60ns (min 6 reference clock of 100Mhz) access timing to AX88780. The 60ns for MCU is almost reached to 8 clocks (125MHz). We recommend that it is needed to extend the access timing of MCU to AX88780.

Appendix A4. Wake On LAN (WOL) without driver via Magic Packet

A4-1. Wake On LAN (WOL) without driver

AX88780 can support WOL without driver exists. In such situations, system must offer 3.3V voltage, reference clock and rest signal to AX88780. Whenever AX88780 detects magic packet from cable, it will drive WAKEUP signal to host system. AX88780 defaults in MII mode (after reset before EEPROM auto-loaded) and uses external PHY. In order to use this function, user must set index 5 of EEPROM to 0x0002 to enable the internal PHY of AX88780.

A4-2. Magic packet

The magic packet received by AX88780 is shown as following;

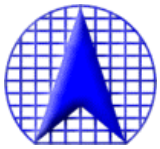
DA + SA + 0x0000 + 0xFFFFFFFFFFFF + (at least repeats 16 times) DA + CRC32

DA = MAC address of AX88780 (6 bytes)

SA = Source address (6 bytes)

Revision History

Revision	Date	Comment
V1.0	2005/10/4	First edition
V1.1	2006/7/28	1. Some typo errors corrected between Pin diagram and tables. 2. Host read/write timing revised in Section 5. 3. Some bits of registers are updated. 4. Add some connections between MCU and AX88780 in Appendix. 5. Add wake up LAN description in Appendix.
V1.2	2007/3/28	1. Correct some information in Section 3.9 for 16-bit mode operation. 2. Modify the data access timing information in Section 6.2.5, 6.2.6, 6.2.10 and Appendix A3. 3. Change the default value of PHYIDR1 register for version 3. 4. Add some information in Section 3.11. 5. Modify some descriptions in Section 1.1, 4.6, 4.17, 4.18, 4.19, 4.23, 4.35~37, 4.41. 6. Rearrange the content of Appendix into Appendix A1~A4. 7. Change the number format from 16h'XXXX to 0xXXXX for example.
V1.3	2007/5/4	1. Swap the XTLN and XTLP pin definitions in Section 2.7. 2. Correct some typo errors of pin type in Table 4 and Table 6.
V1.4	2007/5/18	1. Modify max operation frequency of HCLK from 125MHz to 100MHz. 2. Modify some thermal information in Section 6.1.9.



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