



AZ10EL16VO AZ100EL16VO

ECL/PECL Oscillator Gain Stage and Buffer with Enable

FEATURES

- Green and RoHS Compliant Available
- 250ps Propagation Delay on \bar{Q} Output
- High Voltage Gain vs. Standard EL16
- For Oscillator Applications
- Available in 2x2 or 3x3mm MLP Package
- 75k Ω Enable Pull-Down Resistor
- S-Parameter (.s2p) and IBIS Model Files Available on Arizona Microtek Website

DESCRIPTION

The AZ10/100EL16VO is an oscillator gain stage with a high gain output buffer including an enable. The Q_{HG}/\bar{Q}_{HG} outputs have a voltage gain several times greater than the Q/\bar{Q} outputs. An enable input (\bar{EN}) allows continuous oscillator operation. When \bar{EN} is LOW or floating (NC), input data is passed to both sets of outputs. When \bar{EN} is HIGH, the Q_{HG}/\bar{Q}_{HG} outputs will be forced LOW/HIGH respectively, while input data will continue to be passed to the Q/\bar{Q} outputs. The \bar{EN} input can be driven with an ECL/PECL signal or a CMOS logic signal.

The input impedance of the D/\bar{D} inputs remain constant for all operating modes since forcing the outputs via the \bar{EN} pin does not power-down the chip but only disables the high gain Q_{HG}/\bar{Q}_{HG} outputs.

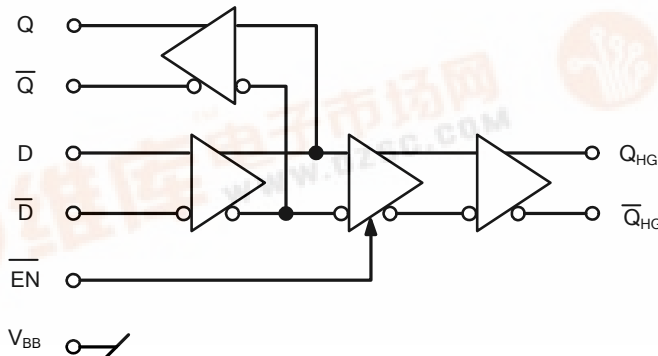
Input protection diodes are included on the D/\bar{D} inputs for enhanced ESD protection.

The EL16VO also provides a V_{BB} output that supports 1.5mA sink/source current. When used, the V_{BB} pin should be bypassed to ground or V_{CC} via a 0.01 μ F capacitor.

Any used output must have an external pull down resistor. For 3.3V operation, an 180 Ω resistor to V_{EE} is recommended if an AC coupled load is present. At 5.0V, a 330 Ω resistor is recommended for the AC load case. Alternately, a 50 Ω load terminated to $V_{CC} - 2V$ or the Thevenin equivalent may be driven directly. Unused outputs may be left floating (NC).

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

PIN/PAD DESCRIPTION



PIN	FUNCTION
D/\bar{D}	Data Inputs
Q/\bar{Q}	Data Outputs
Q_{HG}/\bar{Q}_{HG}	Data Outputs w/High Gain
V_{BB}	Reference Voltage Output
\bar{EN}	Enable Input
V_{CC}	Positive Supply
V_{EE}	Negative Supply



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PACKAGE AVAILABILITY

PACKAGE	PART NUMBER	MARKING	NOTES
MLP 8 (2x2) Green / RoHS Compliant / Lead (Pb) Free	AZ100EL16VONG	P0G <Date Code>	1,2
MLP 8 (2x2)	AZ100EL16VONB	P4 <Date Code>	1,2,3
MLP 8 (2x2) RoHS Compliant / Lead (Pb) Free	AZ100EL16VONB+	P4+ <Date Code>	1,2
MLP 8 (2x2x0.75) Green / RoHS Compliant / Lead (Pb) Free	AZ100EL16VONBG	P4G <Date Code>	1,2
MLP 16 (3x3)	AZ10/100EL16VOL	AZM 16J <Date Code>	1,2
MLP 16 (3x3) Green / RoHS Compliant / Lead (Pb) Free	AZ10/100EL16VOLG	AZMG 16J <Date Code>	1,2
SOIC 8	AZ10EL16VOD	AZM10 EL16VO	1,2,4
SOIC 8	AZ100EL16VOD	AZM100 EL16VO	1,2,4
TSSOP 8	AZ10EL16VOT	AZT 16VO	1,2,4
TSSOP 8 RoHS Compliant / Lead (Pb) Free	AZ10EL16VOT+	AZT+ 16VO	1,2,4
TSSOP 8	AZ100EL16VOT	AZH 16VO	1,2,4
TSSOP 8 RoHS Compliant / Lead (Pb) Free	AZ100EL16VOT+	AZH+ 16VO	1,2,4
TSSOP 10 RoHS Compliant / Lead (Pb) Free	AZ10EL16VOU+	AZT+ 16VOU	1,2,4
TSSOP 10 RoHS Compliant / Lead (Pb) Free	AZ100EL16VOU+	AZH+ 16VOU	1,2,4
DIE	AZ10/100EL16VOXP	N/A	5
DIE	AZ10/100EL16VOXR	N/A	6

- 1 Add R1 at end of part number for 7 inch (1K parts), R2 for 13 inch (2.5K parts) Tape & Reel.
- 2 Date code format: "Y" or "YY" for year followed by "WW" for week.
- 3 Parts marked JNB for date codes prior to 4WW (prior to 2004).
- 4 Date code "YWW" or "YYWW" on underside of part.
- 5 Waffle Pack. Die thickness 180 µm.
- 6 Die on 7 inch Tape & Reel, 3k parts per reel. Die thickness 180 µm.

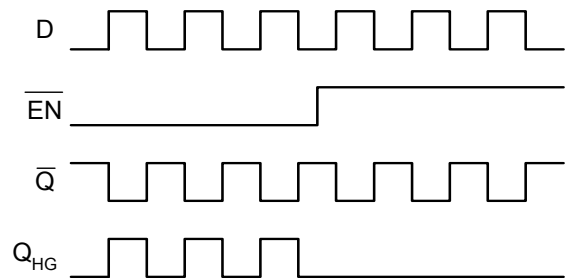
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TRUTH TABLE

EN	Q/Q	Q _{HG}	Q _{HG}
LOW or NC	Data	Data	Data
HIGH	Data	LOW	HIGH

NC = No Connect

TIMING DIAGRAM



Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V _{CC}	PECL Power Supply (V _{EE} = 0V)	0 to +6.0	Vdc
V _I	PECL Input Voltage (V _{EE} = 0V)	0 to +6.0	Vdc
V _{EE}	ECL Power Supply (V _{CC} = 0V)	-6.0 to 0	Vdc
V _I	ECL Input Voltage (V _{CC} = 0V)	-6.0 to 0	Vdc
V _{I DIFF}	Differential Input Voltage D/D	0 to ±1.6	Vpp ¹
I _{OUT}	Output Current — Continuous — Surge	50 100	mA
T _A	Operating Temperature Range	-40 to +85	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C

1. V_{I DIFF} is the voltage difference between D and D-bar

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10K ECL DC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$, $V_{CC} = GND$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{OH}	Output HIGH Voltage ¹	-1080		-890	-1020		-840	-980		-810	-910		-720	mV	
V_{OL}	Output LOW Voltage ¹	-1950		-1650	-1950		-1630	-1950		-1630	-1950		-1595	mV	
V_{IH}	Input HIGH Voltage	D/D	-1230		-430	-1170		-380	-1130		-360	-1060		-310	mV
		\overline{EN}	-1230		V_{CC}	-1170		V_{CC}	-1130		V_{CC}	-1060		V_{CC}	mV
V_{IL}	Input LOW Voltage	D/D	-2300		-1500	-2260		-1480	-2240		-1480	-2190		-1445	mV
		\overline{EN}	V_{EE}		-1500	V_{EE}		-1480	V_{EE}		-1480	V_{EE}		-1445	mV
V_{BB}	Reference Voltage	-1430		-1300	-1380		-1260	-1360		-1240	-1310		-1190	mV	
I_{IH}	Input HIGH Current	D/D			60			60			60			60	μA
		\overline{EN}			150			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA	
I_{EE}	Power Supply Current			40			40			40			40	mA	

1. Each output is terminated through a 50 Ω resistor to $V_{CC} - 2V$.

10K LVPECL DC Characteristics ($V_{EE} = GND$, $V_{CC} = +3.3V$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{OH}	Output HIGH Voltage ^{1,2}	2220		2410	2280		2460	2320		2490	2390		2580	mV	
V_{OL}	Output LOW Voltage ^{1,2}	1350		1650	1350		1670	1350		1670	1350		1705	mV	
V_{IH}	Input HIGH Voltage	D/D ¹	2070		2870	2130		2920	2170		2940	2240		2990	mV
		\overline{EN}	2070 ¹		V_{CC}	2130 ¹		V_{CC}	2170 ¹		V_{CC}	2240 ¹		V_{CC}	mV
V_{IL}	Input LOW Voltage	D/D ¹	1000		1800	1040		1820	1060		1820	1110		1855	mV
		\overline{EN}	V_{EE}		1800 ¹	V_{EE}		1820 ¹	V_{EE}		1820 ¹	V_{EE}		1855 ¹	mV
V_{BB}	Reference Voltage ¹	1870		2000	1920		2040	1940		2060	1990		2110	mV	
I_{IH}	Input HIGH Current	D/D			60			60			60			60	μA
		\overline{EN}			150			150			150			150	μA
I_{IL}	Input LOW Current	D/D	0.5		0.5			0.5			0.5			μA	
		\overline{EN} ³	-300		-300			-300			-300			μA	
I_{EE}	Power Supply Current			40			40			40			40	mA	

1. For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.

2. Each output is terminated through a 50 Ω resistor to $V_{CC} - 2V$.

3. Specified with \overline{EN} forced to V_{EE} .

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10K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3920		4110	3980		4160	4020		4190	4090		4280	mV
V_{OL}	Output LOW Voltage ^{1,2}	3050		3350	3050		3370	3050		3370	3050		3405	mV
V_{IH}	Input HIGH Voltage D/D ¹ EN	3770 3770 ¹		4570 V_{CC}	3830 3830 ¹		4620 V_{CC}	3870 3870 ¹		4640 V_{CC}	3940 3940 ¹		4690 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D ¹ EN	2700 V_{EE}		3500 3500 ¹	2740 V_{EE}		3520 3520 ¹	2760 V_{EE}		3520 3520 ¹	2810 V_{EE}		3555 3555 ¹	mV
V_{BB}	Reference Voltage ¹	3570		3700	3620		3740	3640		3760	3690		3810	mV
I_{IH}	Input HIGH Current D/D EN			60 150			60 150			60 150			60 150	μA
I_{IL}	Input LOW Current D/D EN ³	0.5 -1400			0.5 -1400			0.5 -1400			0.5 -1400			μA
I_{EE}	Power Supply Current			40			40			40			40	mA

1. For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
2. Each output is terminated through a 50 Ω resistor to $V_{CC} - 2\text{V}$.
3. Specified with EN forced to V_{EE} .

100K ECL DC Characteristics ($V_{EE} = -3.0\text{V}$ to -5.5V , $V_{CC} = \text{GND}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ¹	-1085		-880	-1025		-880	-1025		-880	-1025		-880	mV
V_{OL}	Output LOW Voltage ¹	-1900		-1555	-1900		-1620	-1900		-1620	-1900		-1620	mV
V_{IH}	Input HIGH Voltage D/D EN	-1165 -1165		-390 V_{CC}	-1165 -1165		-390 V_{CC}	-1165 -1165		-390 V_{CC}	-1165 -1165		-390 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D EN	-2250 V_{EE}		-1475 -1475	-2250 V_{EE}		-1475 -1475	-2250 V_{EE}		-1475 -1475	-2250 V_{EE}		-1475 -1475	mV
V_{BB}	Reference Voltage	-1390		-1250	-1390		-1250	-1390		-1250	-1390		-1250	mV
I_{IH}	Input HIGH Current D/D EN			60 150			60 150			60 150			60 150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			0.5			μA
I_{EE}	Power Supply Current			40			40			40			46	mA

1. Each output is terminated through a 50 Ω resistor to $V_{CC} - 2\text{V}$.

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100K LVPECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +3.3\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	2215		2420	2275		2420	2275		2420	2275		2420	mV
V_{OL}	Output LOW Voltage ^{1,2}	1400		1745	1400		1680	1400		1680	1400		1680	mV
V_{IH}	Input HIGH Voltage D/D ¹ EN	2135 2135 ¹		2910 V_{CC}	2135 2135 ¹		2910 V_{CC}	2135 2135 ¹		2910 V_{CC}	2135 2135 ¹		2910 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D ¹ EN	1050 V_{EE}		1825 1825 ¹	1050 V_{EE}		1825 1825 ¹	1050 V_{EE}		1825 1825 ¹	1050 V_{EE}		1825 1825 ¹	mV
V_{BB}	Reference Voltage ¹	1910		2050	1910		2050	1910		2050	1910		2050	mV
I_{IH}	Input HIGH Current D/D EN			60 150			60 150			60 150			60 150	μA
I_{IL}	Input LOW Current D/D EN ³	0.5 -300			0.5 -300			0.5 -300			0.5 -300			μA
I_{EE}	Power Supply Current			40			40			40			46	mA

- For supply voltages other than 3.3V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50 Ω resistor to $V_{CC} - 2\text{V}$.
- Specified with EN forced to V_{EE} .

100K PECL DC Characteristics ($V_{EE} = \text{GND}$, $V_{CC} = +5.0\text{V}$)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage ^{1,2}	3915		4120	3975		4120	3975		4120	3975		4120	mV
V_{OL}	Output LOW Voltage ^{1,2}	3100		3445	3100		3380	3100		3380	3100		3380	mV
V_{IH}	Input HIGH Voltage D/D ¹ EN	3835 3835 ¹		4610 V_{CC}	3835 3835 ¹		4610 V_{CC}	3835 3835 ¹		4610 V_{CC}	3835 3835 ¹		4610 V_{CC}	mV
V_{IL}	Input LOW Voltage D/D ¹ EN	2750 V_{EE}		3525 3525 ¹	2750 V_{EE}		3525 3525 ¹	2750 V_{EE}		3525 3525 ¹	2750 V_{EE}		3525 3525 ¹	mV
V_{BB}	Reference Voltage ¹	3610		3750	3610		3750	3610		3750	3610		3750	mV
I_{IH}	Input HIGH Current D/D EN			60 150			60 150			60 150			60 150	μA
I_{IL}	Input LOW Current D/D EN ³	0.5 -1400			0.5 -1400			0.5 -1400			0.5 -1400			μA
I_{EE}	Power Supply Current			40			40			40			46	mA

- For supply voltages other than 5.0V, use the ECL table values and ADD supply voltage value.
- Each output is terminated through a 50 Ω resistor to $V_{CC} - 2\text{V}$.
- Specified with EN forced to V_{EE} .

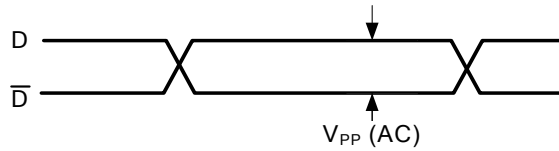
AZ10EL16VO AZ100EL16VO

AC Characteristics ($V_{EE} = -3.0V$ to $-5.5V$; $V_{CC} = GND$ or $V_{EE} = GND$, $V_{CC} = +3.0V$ to $+5.5V$)

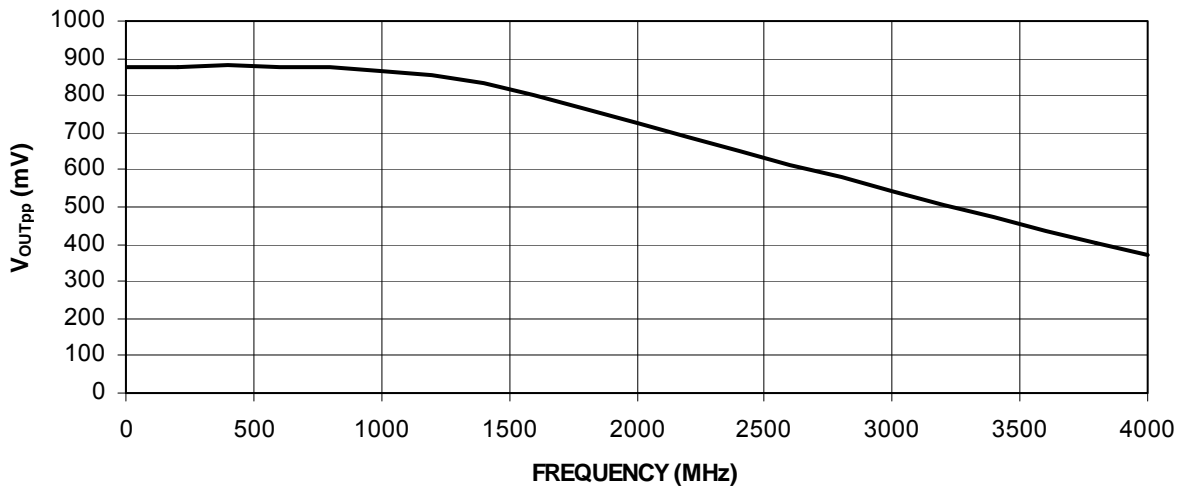
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH}/t_{PHL}	Propagation Delay D to Q/\bar{Q} Outputs (SE)	100		300	100		300	100	200	300	100		300	ps
	D to Q_{HG}/\bar{Q}_{HG} Outputs (SE)	150		450	150		450	150	290	450	150		450	
t_{SKEW}	Duty Cycle Skew ¹ (SE)		5	20		5	20		5	20		5	20	ps
$V_{PP}(AC)$	Input Swing ²	80		1000	80		1000	80		1000	80		1000	mV
t_r/t_f	Output Rise/Fall Times (20% – 80%)	80		240	80		240	80	135	240	80		240	ps

- Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.
- V_{PP} is the peak-to-peak differential input swing for which AC parameters are guaranteed. The device has a voltage gain of ≈ 20 to Q/\bar{Q} outputs and a voltage gain of ≈ 100 to Q_{HG}/\bar{Q}_{HG} outputs.

AC PP INPUT



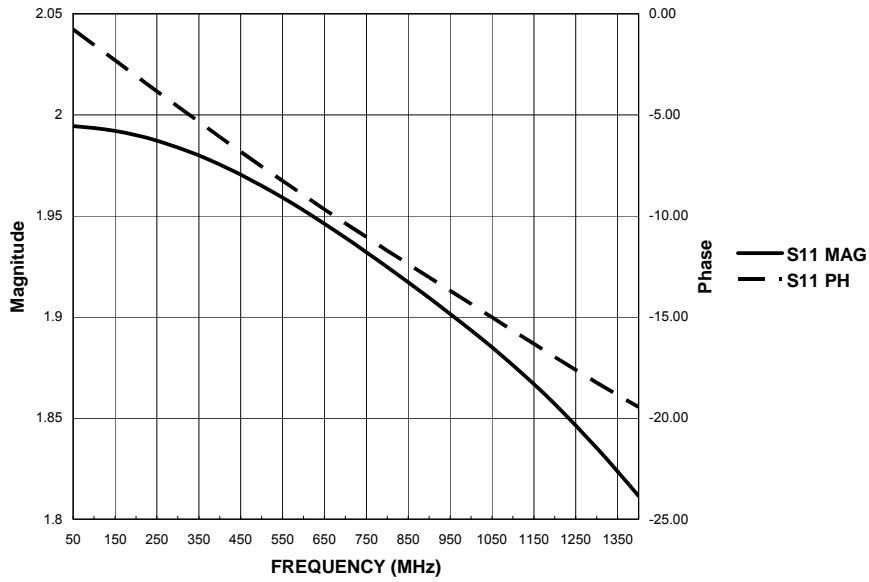
Typical Large Signal Outputs, Q_{HG}/\bar{Q}_{HG}



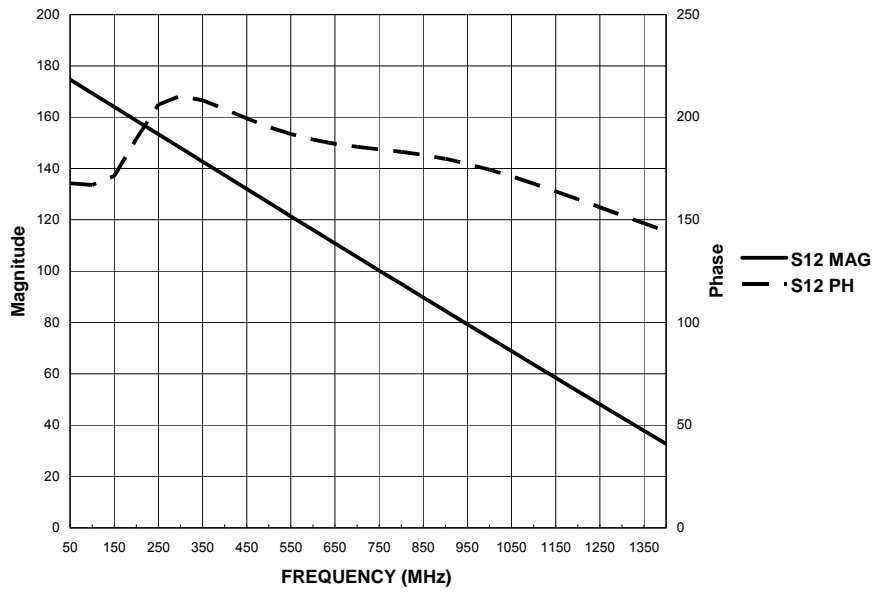
Measured with 750mV differential input, V_{EEP} NC, Q_{HG}/\bar{Q}_{HG} each terminated to $V_{CC}-2V$ via 50Ω resistors.



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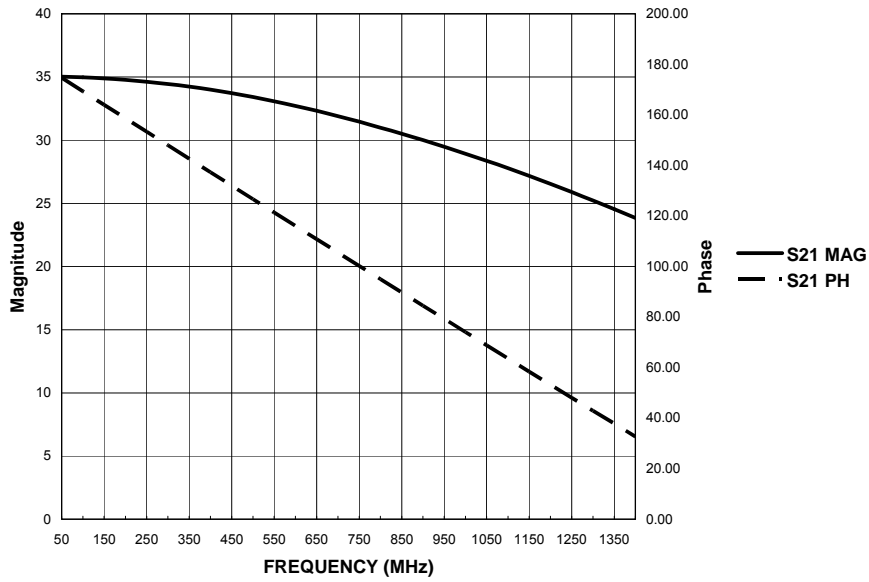


S11, D to Q, 50 Ω load to V_{CC} – 2V

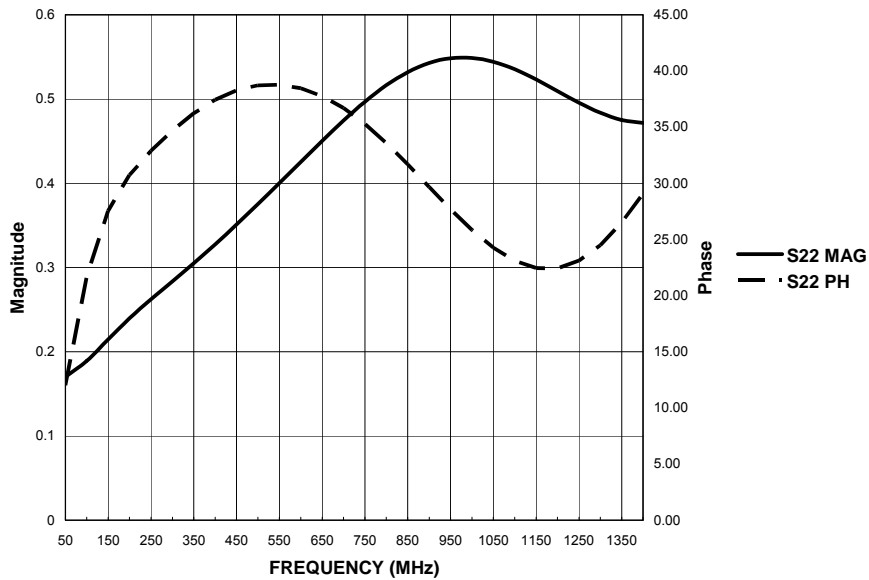


S12, D to Q, 50 Ω load to V_{CC} – 2V

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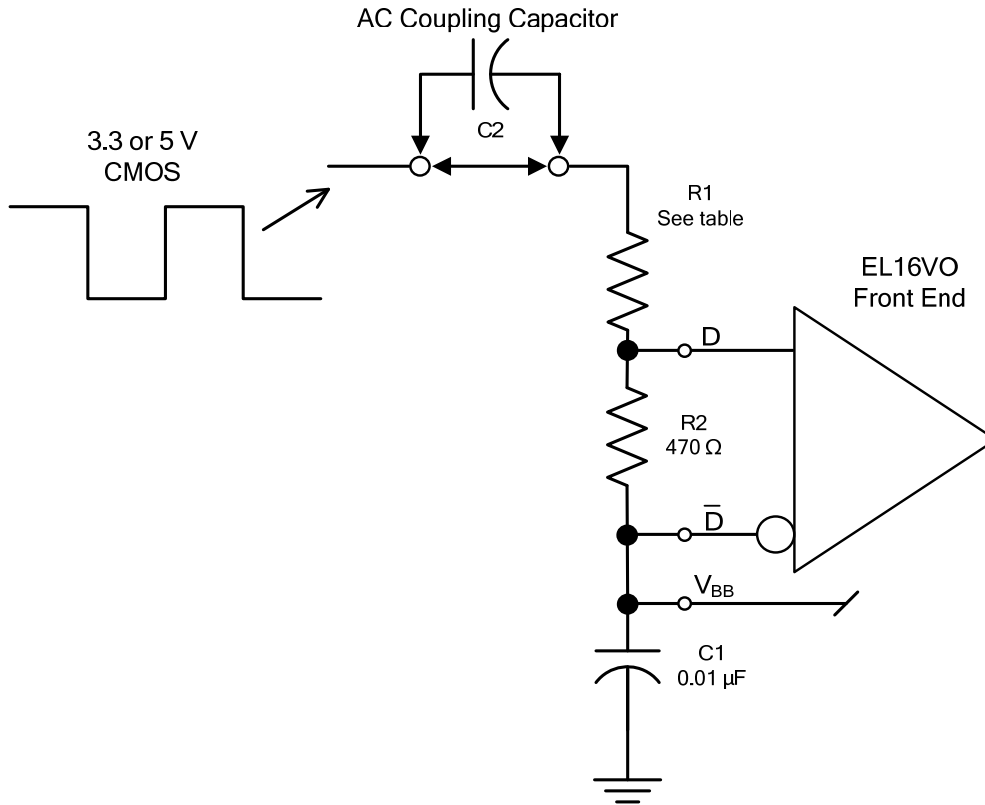


S21, D to Q, 50 Ω load to $V_{CC} - 2V$



S22, D to Q, 50 Ω load to $V_{CC} - 2V$

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Application Circuit for CMOS Inputs

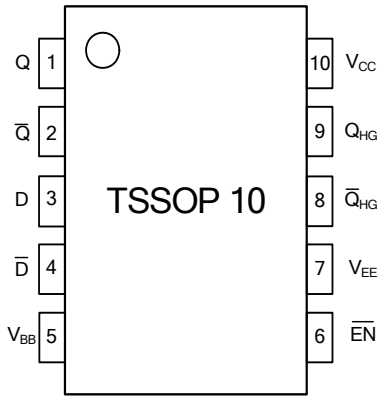
Input Type	R1 ¹	
	AC Coupled (C2 in circuit)	DC Coupled (C2 shorted)
3.3 V CMOS	430 Ω	750 Ω
5 V CMOS	910 Ω	1.8K Ω

¹ R1 should be chosen so that the input swing on the D input with respect to \bar{D} is in the range of ± 80 to ± 1000 mV, per the AC Characteristics table.

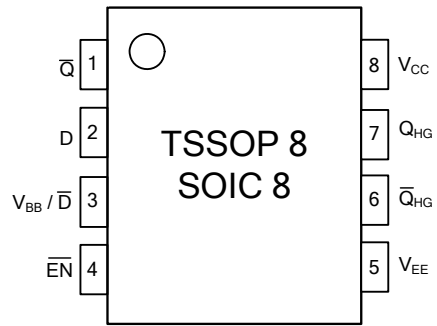
Recommended Component Values for CMOS Single Ended Inputs

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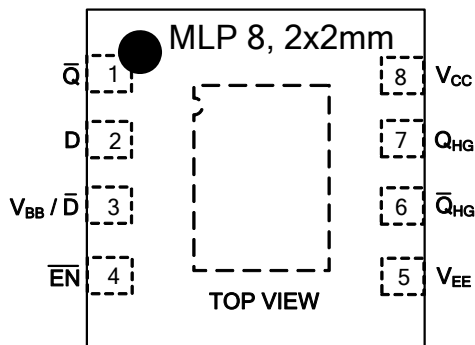
AZ10EL16VOU
AZ100EL16VOU



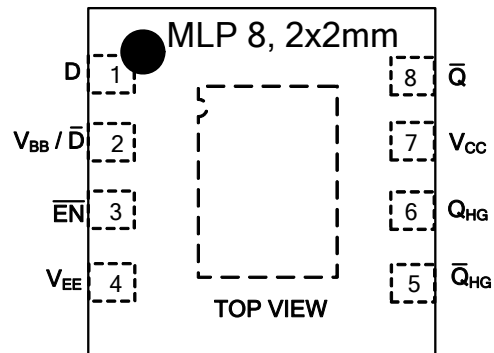
AZ10EL16VOD
AZ100EL16VOD
AZ10EL16VOT
AZ100EL16VOT



AZ100EL16VON

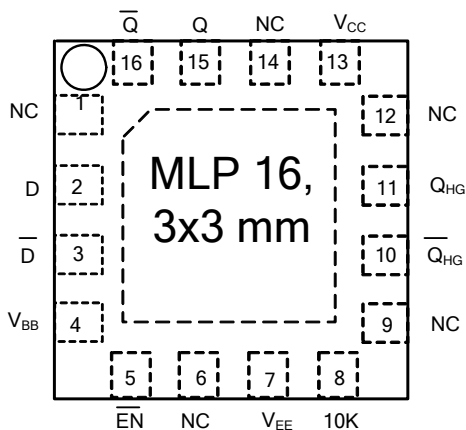


AZ100EL16VONB



MLP 8: Bottom Center Pad may be left open or tied to V_{EE}. Pin 4 is the V_{EE} return.

AZ10/100EL16VOL



MLP 16 (L) Package and DIE:
10K/100K Selection

Connect pin/pad 10K to V_{EE} to select 10K operation. Float (NC) pin/pad 10K to select 100K operation. V_{EE} connection must be less than 1Ω.

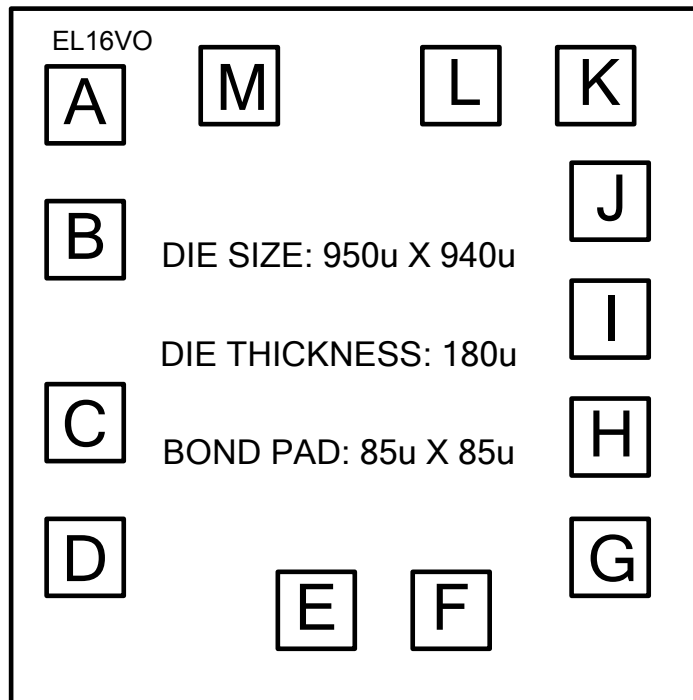
Pin 6 of the MLP 16 package may be connected to pin 7 (V_{EE}) with no effect on the circuit.

MPL 16: Bottom Center Pad may be left open or tied to V_{EE}. Pin 7 is the V_{EE} return.

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DIE PAD COORDINATES

AZ10/100EL16VO DIE:



Note: Other die thicknesses available. Contact factory for further information.

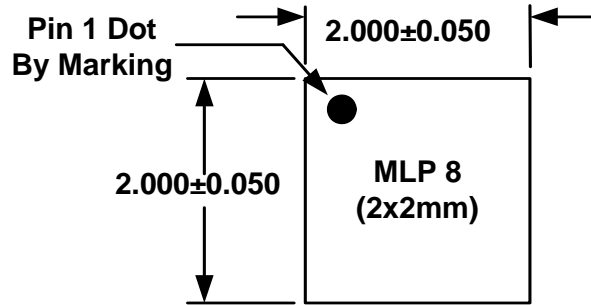
PAD CENTER COORDINATES

NAME	PAD DESIGNATION	X(Microns)	Y(Microns)
A	D	-342.5	312.5
B	\bar{D}	-342.5	144.5
C	V_{BB}	-342.5	-87.0
D	\bar{EN}	-342.5	-255.0
E	V_{EE}	-33.5	-312.5
F	10K	126.5	-312.5
G	\bar{Q}_{HG}	312.5	-248.5
H	Q_{HG}	312.5	-98.5
I	NC	312.5	51.5
J	V_{CC}	312.5	201.5
K	V_{CC}	302.5	342.5
L	Q	142.5	342.5
M	\bar{Q}	-140.5	342.5

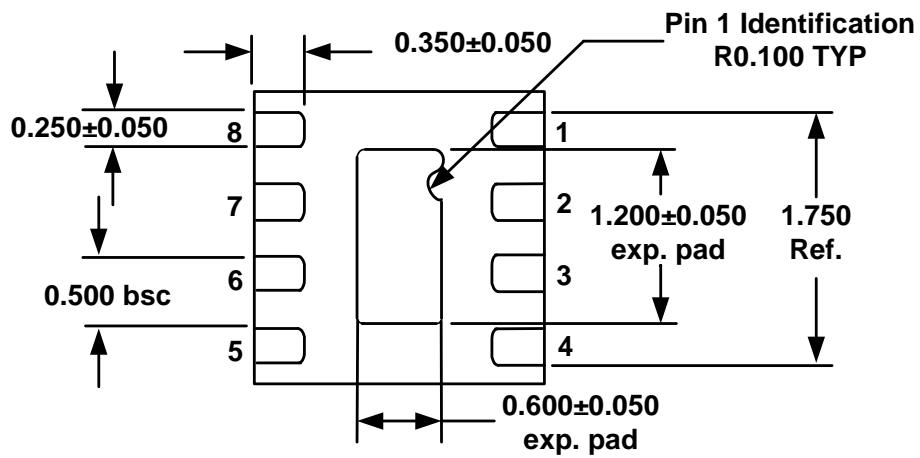
NC = No connect, leave open.

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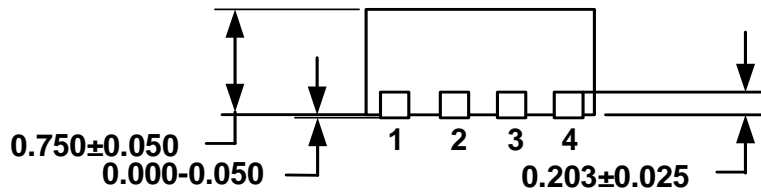
PACKAGE DIAGRAM
MLP 8 2x2mm



TOP VIEW



BOTTOM VIEW

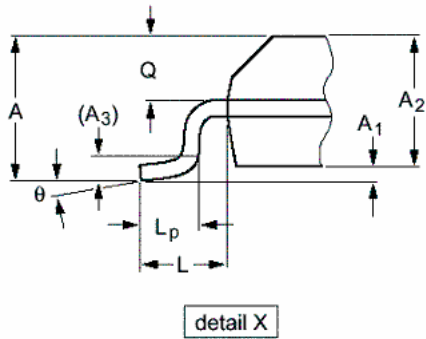
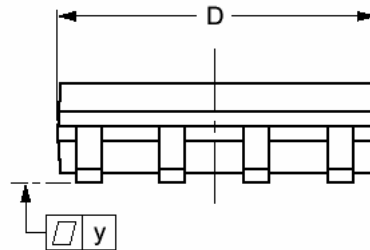
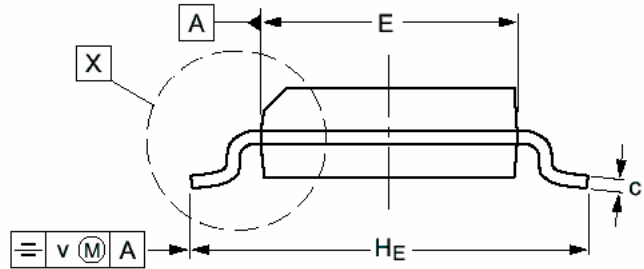
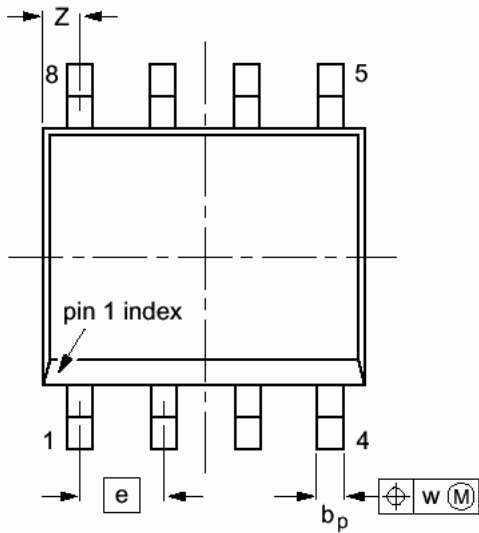


SIDE VIEW

Note: All dimensions are in mm

AZ10EL16VO
AZ100EL16VO

PACKAGE DIAGRAM
SOIC 8



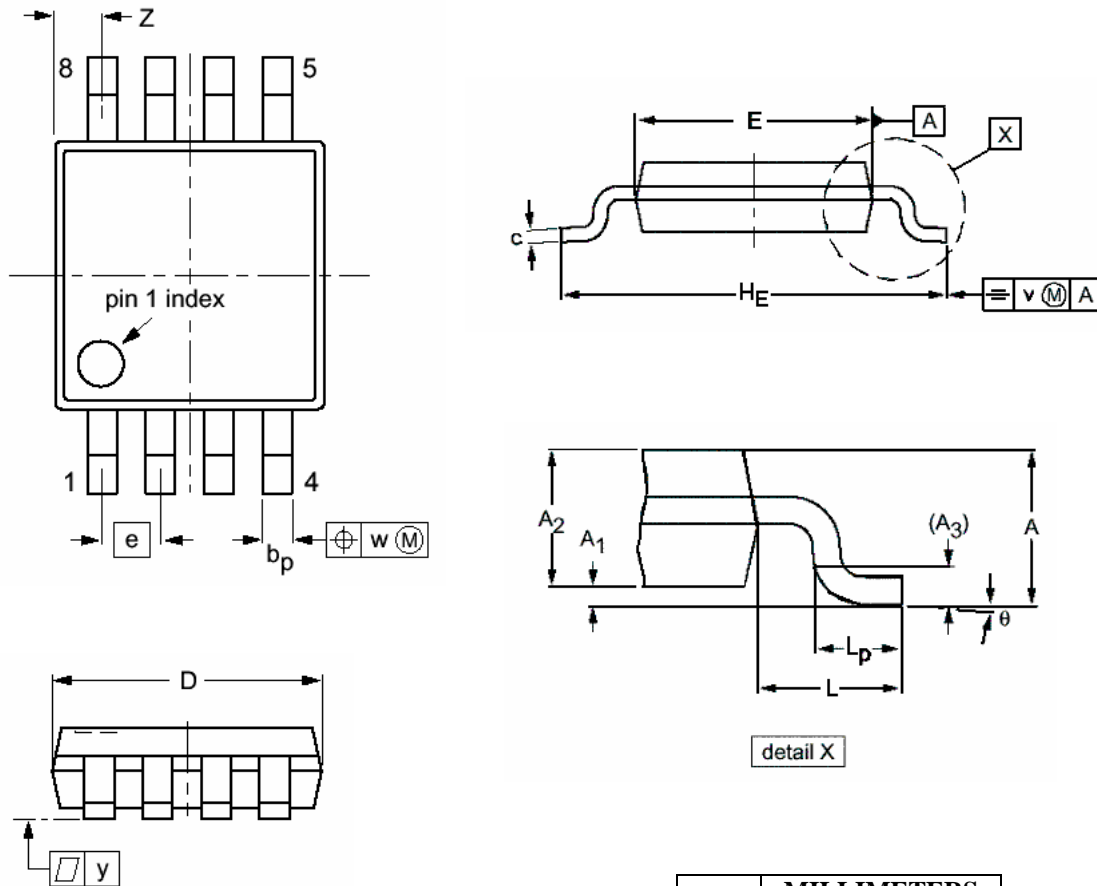
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		0.75		0.069
A ₁	0.10	0.25	0.004	0.010
A ₂	1.25	1.45	0.049	0.057
A ₃	0.25		0.01	
b _p	0.36	0.49	0.014	0.019
c	0.19	0.25	0.0075	0.0100
D	4.8	5.0	0.19	0.20
E	3.8	4.0	0.15	0.16
e	1.27		0.050	
H _E	5.80	6.20	0.228	0.244
L	1.05		0.041	
L _p	0.40	1.00	0.016	0.039
Q	0.60	0.70	0.024	0.028
v	0.25		0.01	
w	0.25		0.01	
y	0.10		0.004	
Z	0.30	0.70	0.012	0.028
θ	0°	8°	0°	8°

NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

AZ10EL16VO
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PACKAGE DIAGRAM
TSSOP 8



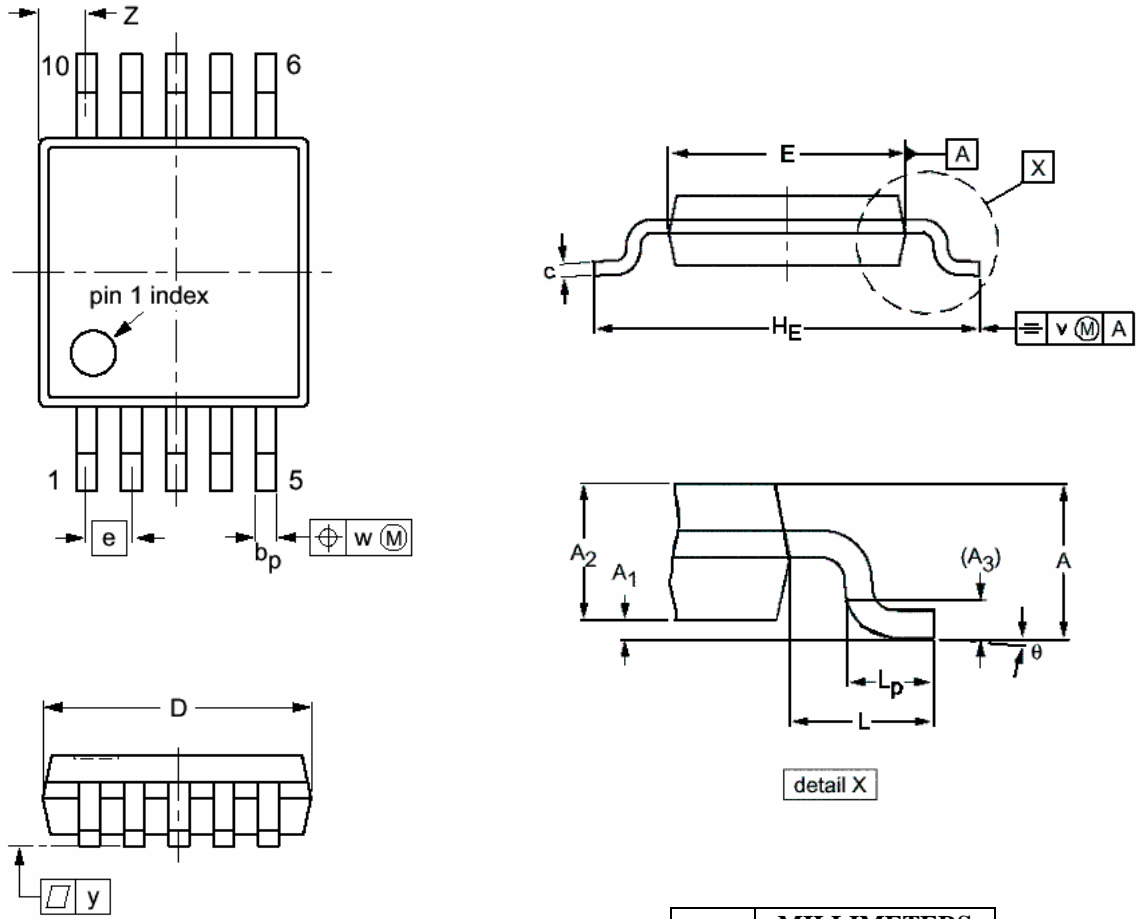
NOTES:

1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

DIM	MILLIMETERS	
	MIN	MAX
A		1.10
A ₁	0.05	0.15
A ₂	0.80	0.95
A ₃	0.25	
b _p	0.25	0.45
c	0.15	0.28
D	2.90	3.10
E	2.90	3.10
e	0.65	
H _E	4.70	5.10
L	0.94	
L _p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.35	0.70
θ	0°	6°

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**PACKAGE DIAGRAM
TSSOP 10**



- NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 2. MAXIMUM MOLD PROTRUSION FOR D IS 0.15mm.
 3. MAXIMUM MOLD PROTRUSION FOR E IS 0.25mm.

	MILLIMETERS	
	MIN	MAX
A		1.10
A₁	0.05	0.15
A₂	0.80	0.95
A₃	0.25	
b_p	0.15	0.30
c	0.15	0.23
D¹	2.90	3.10
E²	2.90	3.10
e	0.50	
H_E	4.80	5.00
L	0.95	
L_p	0.40	0.70
v	0.10	
w	0.10	
y	0.10	
Z	0.34	0.67
θ	0°	6°

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