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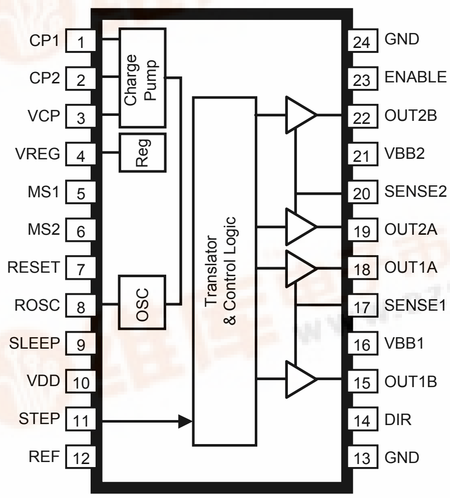
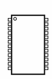
A3984

DMOS Microstepping Driver with Translator

Package LP





Approximate Scale 1:1

ABSOLUTE MAXIMUM RATINGS

Load Supply Voltage, V_{BB} .... **35 V**
Output Current, I_{OUT} .... **±2 A***
Logic Input Voltage, V_{IN} .... **–0.3 V to 7 V**
Sense Voltage, V_{SENSE} .... **0.5 V**
Reference Voltage, V_{REF} ……….. .... **4 V**
Operating Temperature Range
  Ambient, T_A .... **–20°C to 85°C**
  Junction Temperature, $T_{J(MAX)}$..................... **150°C**
Storage Temperature, T_S .... **–55°C to 150°C**

*Output current rating may be limited by duty cycle, ambient temperature, and heat sinking. Under any set of conditions, do not exceed the specified current rating or a junction temperature of 150°C.

The A3984 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes, with an output drive capacity of up to 35 V and ±2 A. The A3984 includes a fixed off-time current regulator which has the ability to operate in Slow or Mixed decay modes.

The translator is the key to the easy implementation of the A3984. Simply inputting one pulse on the STEP input drives the motor one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The A3984 interface is an ideal fit for applications where a complex microprocessor is unavailable or is overburdened.

The chopping control in the A3984 automatically selects the current decay mode (Slow or Mixed). When a signal occurs at the STEP input pin, the A3984 determines if that step results in a higher or lower current in each of the motor phases. If the change is to a higher current, then the decay mode is set to Slow decay. If the change is to a lower current, then the current decay is set to Mixed (set initially to a fast decay for a period amounting to 31.25% of the fixed off-time, then to a slow decay for the remainder of the off-time). This current decay control scheme results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes: thermal shutdown with hysteresis, undervoltage lockout (UVLO), and crossover-current protection. Special power-on sequencing is not required.

The A3984 is supplied in a low-profile (1.2 mm maximum), 24-pin TSSOP with exposed thermal pad (package *LP*). It is also available in a lead (Pb) free version (suffix *–T*), with 100% matte tin plated leadframes.

FEATURES

- Low $R_{DS(ON)}$ outputs
- Automatic current decay mode detection/selection
- Mixed and Slow current decay modes
- Synchronous rectification for low power dissipation
- Internal UVLO and thermal shutdown circuitry
- Crossover-current protection

Selection Guide

Part Number	Pb-free*	Package	Packing
A3984SLP-T	Yes	24-pin TSSOP	62 per tube
A3984SLPTR-T	Yes	24-pin TSSOP	4000 per reel

*Pb-based variants are being phased out of the product line. The variants cited in this footnote are in production but have been determined to be LAST TIME BUY. This classification indicates that sale of this device is currently restricted to existing customer applications. The variants should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: October 31, 2006. Deadline for receipt of LAST TIME BUY orders: April 27, 2007. These variants include: A3984SLP and A3984SLPTR.

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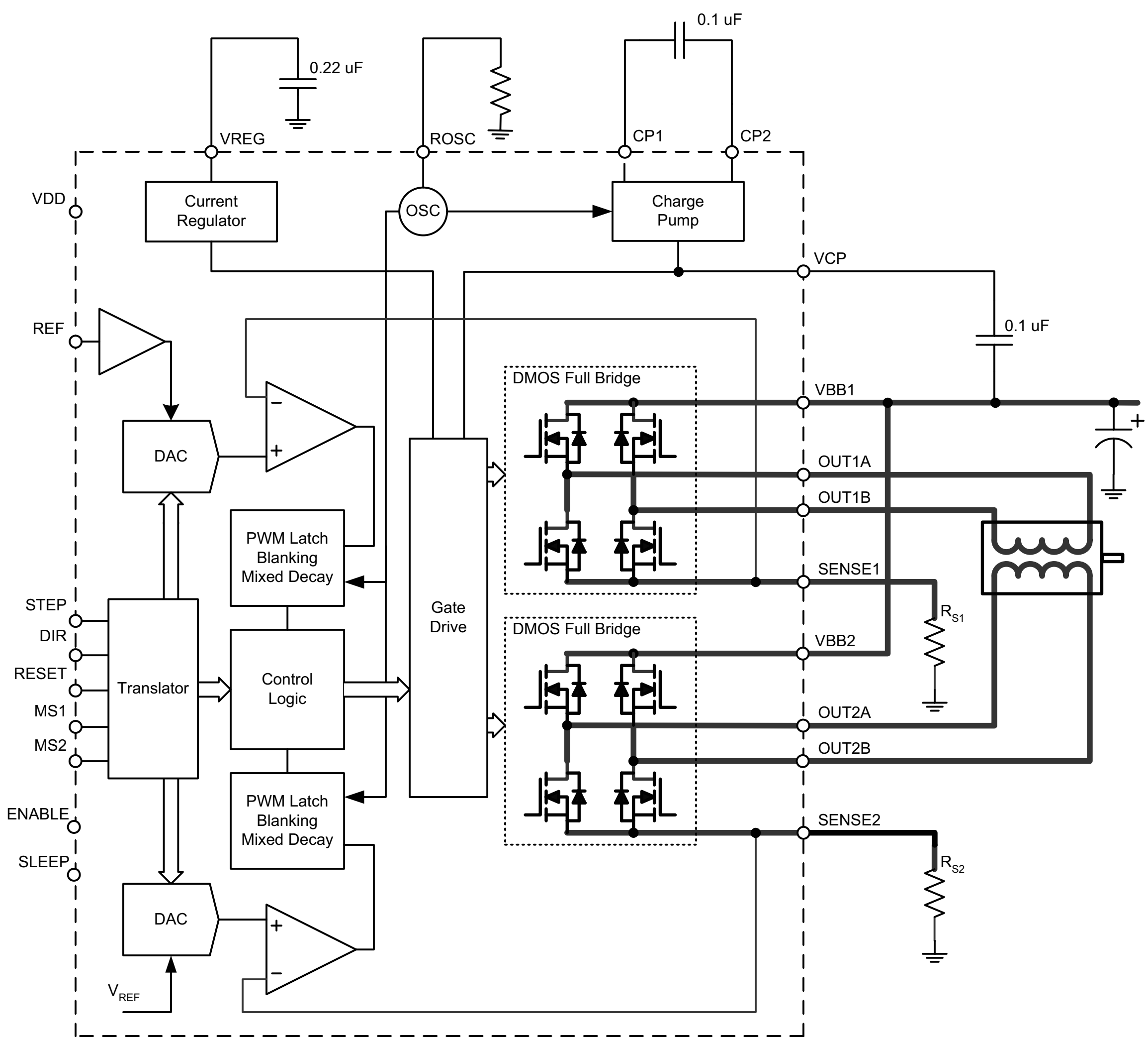
Functional Block Diagram



ELECTRICAL CHARACTERISTICS[1] at T_A = 25°C, V_{BB} = 35 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[2]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Operating	8	–	35	V
		During Sleep Mode	0	–	35	V
Logic Supply Voltage Range	V_{DD}	Operating	3.0	–	5.5	V
Output On Resistance	R_{DSON}	Source Driver, I_{OUT} = –1.5 A	–	0.350	0.450	Ω
		Sink Driver, I_{OUT} = 1.5 A	–	0.300	0.370	Ω
Body Diode Forward Voltage	V_F	Source Diode, I_F = –1.5 A	–	–	1.2	V
		Sink Diode, I_F = 1.5 A	–	–	1.2	V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz	–	–	4	mA
		Operating, outputs disabled	–	–	2	mA
		Sleep Mode	–	–	10	μA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz	–	–	8	mA
		Outputs off	–	–	5	mA
		Sleep Mode	–	–	10	μA
Control Logic						
Logic Input Voltage	$V_{IN(1)}$		$V_{DD}\times0.7$	–	–	V
	$V_{IN(0)}$		–	–	$V_{DD}\times0.3$	V
Logic Input Current	$I_{IN(1)}$	$V_{IN} = V_{DD}\times0.7$	–20	<1.0	20	μA
	$I_{IN(0)}$	$V_{IN} = V_{DD}\times0.3$	–20	<1.0	20	μA
Microstep Select 2	MS2		–	50	–	kΩ
Input Hysteresis	$V_{HYS(IN)}$		150	300	500	mV
Blank Time	t_{BLANK}		0.7	1	1.3	μs
Fixed Off-Time	t_{OFF}	OSC > 3 V	20	30	40	μs
		R_{OSC} = 25 kΩ	23	30	37	μs
Reference Input Voltage Range	V_{REF}		0	–	4	V
Reference Input Current	I_{REF}		–3	0	3	μA
Current Trip-Level Error[3]	err_I	V_{REF} = 2 V, $\%I_{TripMAX}$ = 38.27%	–	–	±15	%
		V_{REF} = 2 V, $\%I_{TripMAX}$ = 70.71%	–	–	±5	%
		V_{REF} = 2 V, $\%I_{TripMAX}$ = 100.00%	–	–	±5	%
Crossover Dead Time	t_{DT}		100	475	800	ns
Protection						
Thermal Shutdown Temperature	T_J		–	165	–	°C
Thermal Shutdown Hysteresis	T_{JHYS}		–	15	–	°C
UVLO Enable Threshold	UV_{LO}	V_{DD} rising	2.35	2.7	3	V
UVLO Hysteresis	UV_{HYS}		0.05	0.10	–	V

[1]Negative current is defined as coming out of (sourcing from) the specified device pin.
[2]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.
[3]$err_I = (I_{Trip} - I_{Prog}) / I_{Prog}$, where $I_{Prog} = \%I_{TripMAX} \times I_{TripMAX}$.

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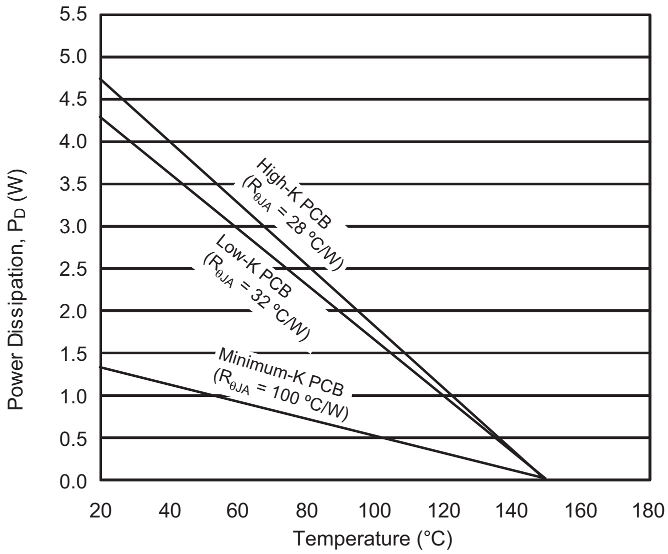
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	One-layer PCB, one-sided with copper limited to solder pads	100	ºC/W
		One layer PCB, two-sided with copper limited to solder pads and 3.8 in.^{2} of copper area on each side, connected to GND pins	32	ºC/W
		High-K PCB (multilayer with significant copper areas, based on JEDEC standard)	28	ºC/W

*In still air. Additional thermal information available on Allegro Web site.

Maximum Power Dissipation, $P_{D(max)}$



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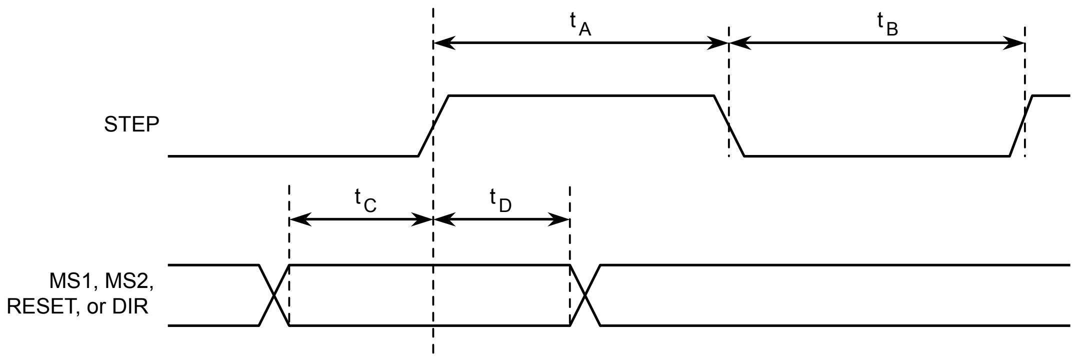

Time Duration	Symbol	Typ.	Unit
STEP minimum, HIGH pulse width	t_A	1	μs
STEP minimum, LOW pulse width	t_B	1	μs
Setup time, input change to STEP	t_C	200	ns
Hold time, input change to STEP	t_D	200	ns

Figure 1. Logic Interface Timing Diagram

Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution	Excitation Mode
L	L	Full Step	2 Phase
H	L	Half Step	1-2 Phase
L	H	Quarter Step	W1-2 Phase
H	H	Sixteenth Step	4W1-2 Phase

Functional Description

Device Operation. The A3984 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, quarter-, and sixteenth-step modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PMW (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (R_{S1} or R_{S2}), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-on or reset, the translator sets the DACs and the phase current polarity to the initial Home state (shown in figures 2 through 5), and the current regulator to Mixed Decay Mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See table 2 for the current-level sequence.) The microstep resolution is set by the combined effect of inputs MS1 and MS2, as shown in table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode for the active full-bridge is set to Mixed. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to Slow. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

RESET Input (RESET). The RESET input sets the translator to a predefined Home state (shown in figures 2 through 5), and turns off all of the DMOS outputs. All STEP inputs are ignored until the RESET input is set to high.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of inputs MS1 and MS2.

Microstep Select (MS1 and MS2). Selects the microstepping format, as shown in table 1. MS2 has a 50 kΩ pulldown resistance. Any changes made to these inputs do not take effect until the next STEP rising edge.

Direction Input (DIR). This determines the direction of rotation of the motor. When low, the direction will be clockwise and when high, counterclockwise. Changes to this input do not take effect until the next STEP rising edge.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and the current sense resistor, R_{Sx}. When the voltage across R_{Sx} equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off either the source DMOS FETs (when in Slow Decay Mode) or the sink and source DMOS FETs (when in Mixed Decay Mode).

The maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF pin. The transconductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

where R_S is the resistance of the sense resistor (Ω) and V_{REF} is the input voltage on the REF pin (V).

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

(See table 2 for $\%I_{TripMAX}$ at each step.)

It is critical that the maximum rating (0.5 V) on the SENSE1 and SENSE2 pins is not exceeded.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The one shot off-time, t_{OFF}, is determined by the selection of an external resistor connected from the ROSC timing pin to ground. If the ROSC pin is tied to an external voltage > 3 V, then t_{OFF} defaults to 30 µs. The ROSC pin can be safely connected to the VDD pin for this purpose. The value of t_{OFF} (µs) is approximately

$$t_{OFF} \approx (R_{OSC} / 880) + 1.6$$

Blanking. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (µs), is approximately

$$t_{BLANK} \approx 1\ \mu s$$

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side DMOS gates. A 0.1 µF ceramic capacitor, should be connected between CP1 and CP2. In addition, a 0.1 µF ceramic capacitor is required between VCP and VBB, to act as a reservoir for operating the high-side DMOS gates.

VREG (VREG). This internally-generated voltage is used to operate the sink-side DMOS outputs. The VREG pin must be decoupled with a 0.22 µF capacitor to ground. VREG is internally monitored. In the case of a fault condition, the DMOS outputs of the A3984 are disabled.

Enable Input (ENABLE). This input turns on or off all of the DMOS outputs. When set to a logic high, the outputs are disabled. When set to a logic low, the internal control enables the outputs as required. The translator inputs STEP, DIR, MS1, and MS2, as well as the internal sequencing logic, all remain active, independent of the ENABLE input state.

Shutdown. In the event of a fault, overtemperature (excess T_J) or an undervoltage (on VCP), the DMOS outputs of the A3984 are disabled until the fault condition is removed. At power-on, the UVLO (undervoltage lockout) circuit disables the DMOS outputs and resets the translator to the Home state.

Sleep Mode (SLEEP). To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output DMOS FETs, current regulator, and charge pump. A logic low on the SLEEP pin puts the A3984 into Sleep mode. A logic high allows normal operation, as well as start-up (at which time the A3984 drives the motor to the Home microstep position). When emerging from Sleep mode, in order to allow the charge pump to stabilize, provide a delay of 1 ms before issuing a Step command.

Mixed Decay Operation. The bridge can operate in Mixed Decay mode, depending on the step sequence, as shown in figures 3 thru 5. As the trip point is reached, the A3984 initially goes into a fast decay mode for 31.25% of the off-time. t_{OFF}. After that, it switches to Slow Decay mode for the remainder of t_{OFF}.

Synchronous Rectification. When a PWM-off cycle is triggered by an internal fixed–off-time cycle, load current recirculates according to the decay mode selected by the control logic. This synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low DMOS R_{DSON}. This reduces power dissipation significantly, and can eliminate the need for external Schottky diodes in many applications. Turning off synchronous rectification prevents the reversal of the load current when a zero-current level is detected.

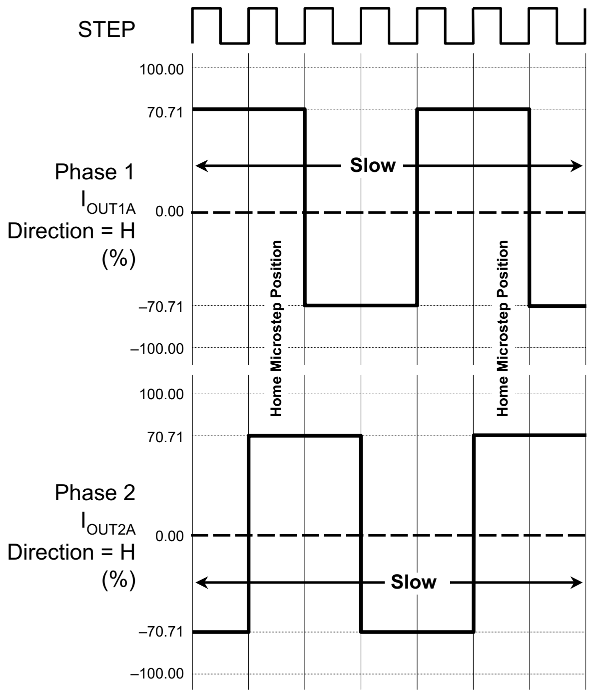

Figure 2. Decay Mode for Full-Step Increments

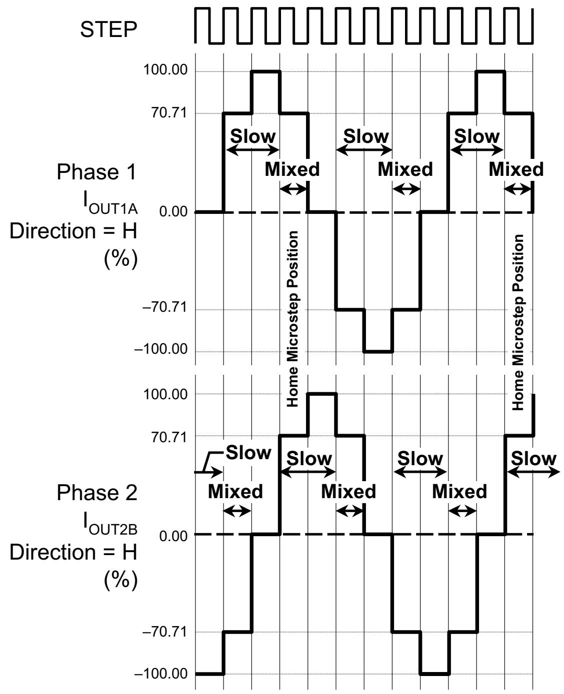

Figure 3. Decay Modes for Half-Step Increments

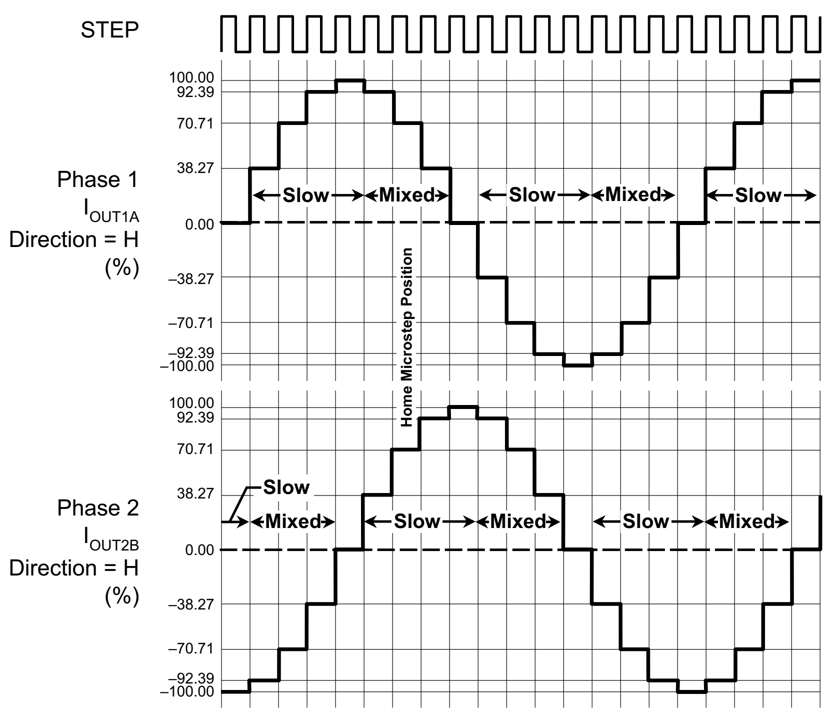

Figure 4. Decay Modes for Quarter-Step Increments

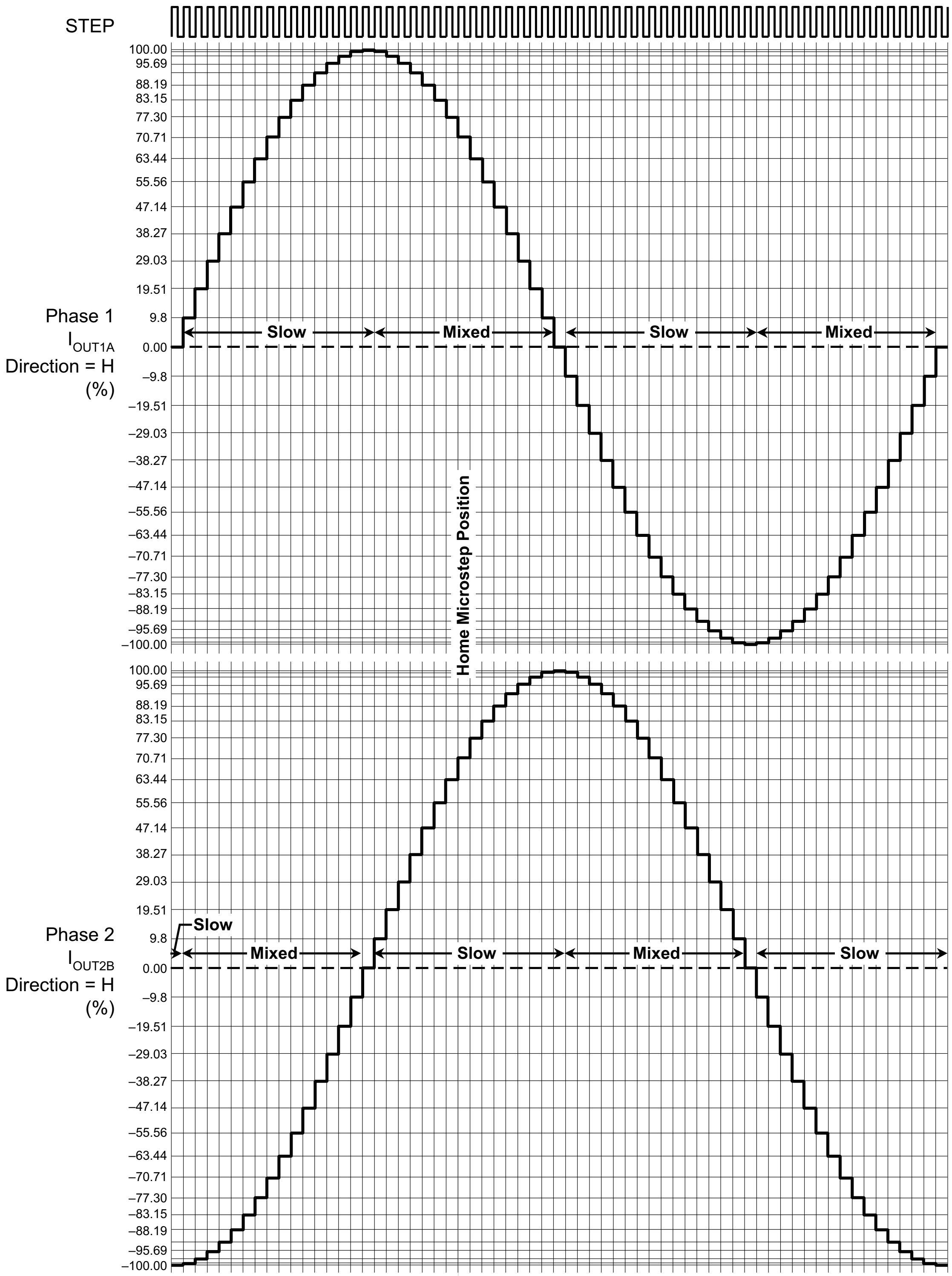

Figure 5. Decay Modes for Sixteenth-Step Increments

Table 2. Step Sequencing Settings

Home microstep position at Step Angle 45º; DIR = H

Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (º)	Full Step #	Half Step #	1/4 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (º)
	1	1	1	100.00	0.00	0.0		5	9	33	–100.00	0.00	180.0
			2	99.52	9.80	5.6				34	–99.52	–9.80	185.6
			3	98.08	19.51	11.3				35	–98.08	–19.51	191.3
			4	95.69	29.03	16.9				36	–95.69	–29.03	196.9
		2	5	92.39	38.27	22.5			10	37	–92.39	–38.27	202.5
			6	88.19	47.14	28.1				38	–88.19	–47.14	208.1
			7	83.15	55.56	33.8				39	–83.15	–55.56	213.8
			8	77.30	63.44	39.4				40	–77.30	–63.44	219.4
1	2	3	9	70.71	70.71	45.0	3	6	11	41	–70.71	–70.71	225.0
			10	63.44	77.30	50.6				42	–63.44	–77.30	230.6
			11	55.56	83.15	56.3				43	–55.56	–83.15	236.3
			12	47.14	88.19	61.9				44	–47.14	–88.19	241.9
		4	13	38.27	92.39	67.5			12	45	–38.27	–92.39	247.5
			14	29.03	95.69	73.1				46	–29.03	–95.69	253.1
			15	19.51	98.08	78.8				47	–19.51	–98.08	258.8
			16	9.80	99.52	84.4				48	–9.80	–99.52	264.4
	3	5	17	0.00	100.00	90.0		7	13	49	0.00	–100.00	270.0
			18	–9.80	99.52	95.6				50	9.80	–99.52	275.6
			19	–19.51	98.08	101.3				51	19.51	–98.08	281.3
			20	–29.03	95.69	106.9				52	29.03	–95.69	286.9
		6	21	–38.27	92.39	112.5			14	53	38.27	–92.39	292.5
			22	–47.14	88.19	118.1				54	47.14	–88.19	298.1
			23	–55.56	83.15	123.8				55	55.56	–83.15	303.8
			24	–63.44	77.30	129.4				56	63.44	–77.30	309.4
2	4	7	25	–70.71	70.71	135.0	4	8	15	57	70.71	–70.71	315.0
			26	–77.30	63.44	140.6				58	77.30	–63.44	320.6
			27	–83.15	55.56	146.3				59	83.15	–55.56	326.3
			28	–88.19	47.14	151.9				60	88.19	–47.14	331.9
		8	29	–92.39	38.27	157.5			16	61	92.39	–38.27	337.5
			30	–95.69	29.03	163.1				62	95.69	–29.03	343.1
			31	–98.08	19.51	168.8				63	98.08	–19.51	348.8
			32	–99.52	9.80	174.4				64	99.52	–9.80	354.4

Pin List Table

Name	Description	Number
CP1	Charge pump capacitor 1	1
CP2	Charge pump capacitor 2	2
VCP	Reservoir capacitor	3
VREG	Regulator decoupling	4
MS1	Logic input	5
MS2	Logic input	6
RESET	Logic input	7
ROSC	Timing set	8
SLEEP	Logic input	9
VDD	Logic supply	10
STEP	Logic input	11
REF	Current trip reference voltage input	12
GND	Ground*	13
DIR	Logic input	14
OUT1B	DMOS Full Bridge 1 Output B	15
VBB1	Load supply	16
SENSE1	Sense resistor for Bridge 1	17
OUT1A	DMOS Full Bridge 1 Output A	18
OUT2A	DMOS Full Bridge 2 Output A	19
SENSE2	Sense resistor for Bridge 2	20
VBB2	Load supply	21
OUT2B	DMOS Full Bridge 2 Output B	22
ENABLE	Logic input	23
GND	Ground*	24

*The two GND pins must be tied together externally by connecting to the exposed pad ground plane under the device.

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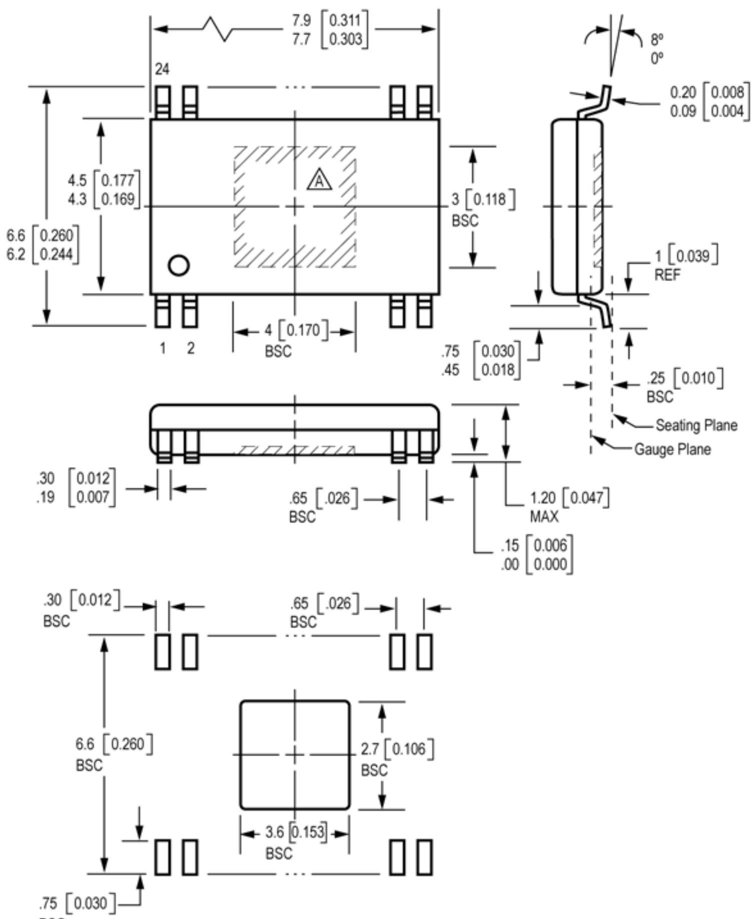
LP Package, 24-Pin TSSOP with Exposed Thermal Pad



Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
A Exposed thermal pad (bottom surface)
Dimensions preliminary

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