



BB502M

Built in Biasing Circuit MOS FET IC
UHF RF Amplifier

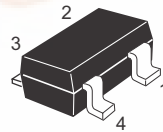
REJ03G0833-0500
(Previous ADE-208-809C)
Rev.5.00
Aug.10.2005

Features

- Built in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise; NF = 1.6 dB typ. at f = 900 MHz
- High gain; PG = 22 dB typ. at f = 900 MHz
- Withstanding to ESD;
Built in ESD absorbing diode. Withstand up to 200V at C=200pF, Rs=0 conditions.
- Provide mini mold packages; MPAK-4(SOT-143Rmod)

Outline

RENESAS Package code: PLSP0004ZA-A
(Package name: MPAK-4)



1. Source
2. Gate1
3. Gate2
4. Drain

- Notes:
1. Marking is "BS-".
 2. BB502M is individual type number of RENESAS BBFET.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate1 to source voltage	V_{G1S}	+6 -0	V
Gate2 to source voltage	V_{G2S}	+6 -0	V
Drain current	I_D	20	mA
Channel power dissipation	Pch	150	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

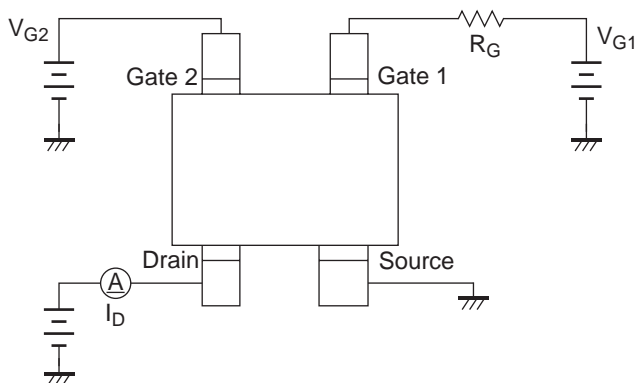
Electrical Characteristics

(Ta = 25°C)

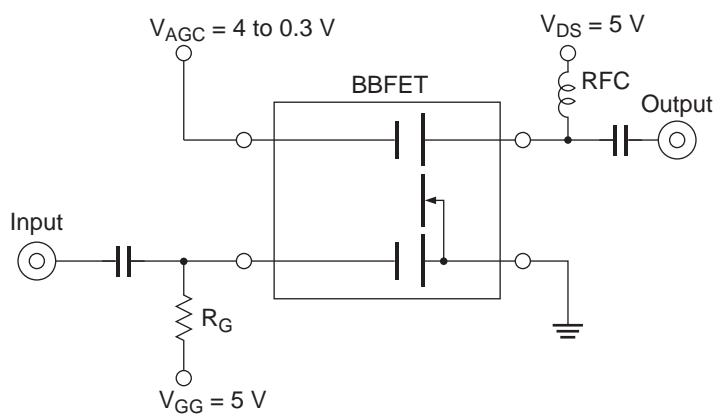
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	$I_D = 200 \mu A$, $V_{G1S} = V_{G2S} = 0$
Gate1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	$I_{G1} = +10 \mu A$, $V_{G2S} = V_{DS} = 0$
Gate2 to source breakdown voltage	$V_{(BR)G2SS}$	+6	—	—	V	$I_{G2} = +10 \mu A$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff current	I_{G1SS}	—	—	+100	nA	$V_{G1S} = +5 V$, $V_{G2S} = V_{DS} = 0$
Gate2 to source cutoff current	I_{G2SS}	—	—	+100	nA	$V_{G2S} = +5 V$, $V_{G1S} = V_{DS} = 0$
Gate1 to source cutoff voltage	$V_{G1S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5 V$, $V_{G2S} = 4 V$ $I_D = 100 \mu A$
Gate2 to source cutoff voltage	$V_{G2S(off)}$	0.5	0.7	1.0	V	$V_{DS} = 5 V$, $V_{G1S} = 5 V$ $I_D = 100 \mu A$
Drain current	$I_{D(op)}$	8	11	14	mA	$V_{DS} = 5 V$, $V_{G1} = 5 V$ $V_{G2S} = 4 V$, $R_G = 180 k\Omega$
Forward transfer admittance	$ y_{fs} $	20	25	30	mS	$V_{DS} = 5 V$, $V_{G1} = 5 V$, $V_{G2S} = 4 V$ $R_G = 180 k\Omega$, $f = 1 kHz$
Input capacitance	Ciss	1.4	1.7	2.0	pF	$V_{DS} = 5 V$, $V_{G1} = 5 V$ $V_{G2S} = 4 V$, $R_G = 180 k\Omega$ $f = 1 MHz$
Output capacitance	Coss	0.7	1.1	1.5	pF	
Reverse transfer capacitance	Crss	—	0.02	0.05	pF	
Power gain	PG	17	22	—	dB	$V_{DS} = 5 V$, $V_{G1} = 5 V$ $V_{G2S} = 4 V$, $R_G = 180 k\Omega$ $f = 900 MHz$
Noise figure	NF	—	1.6	2.2	dB	

Main Characteristics

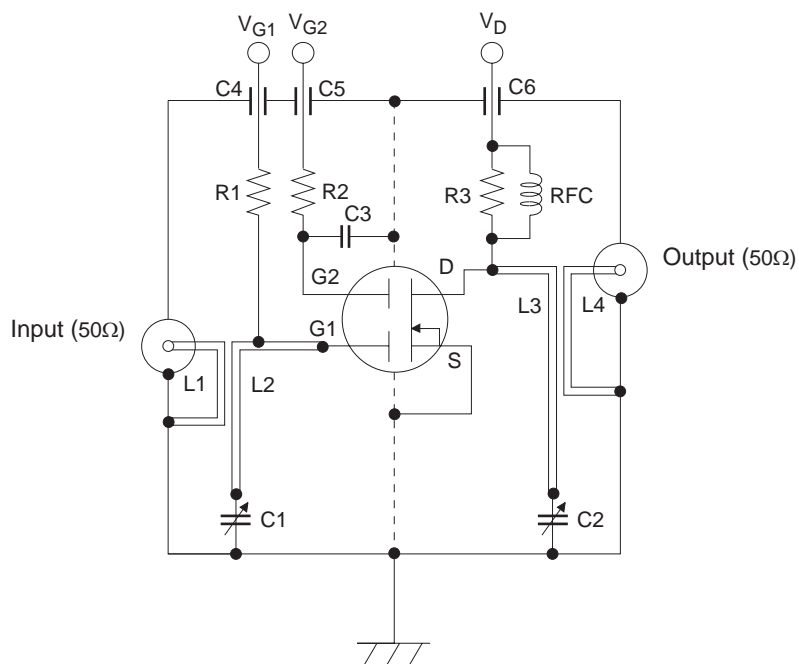
Test Circuit for Operating Items ($I_{D(op)}$, $|y_{fs}|$, C_{iss} , C_{oss} , C_{rss} , NF, PG)



Application Circuit

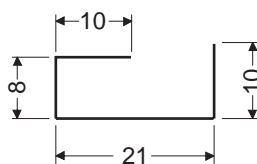


900MHz Power Gain, Noise Figure Test Circuit

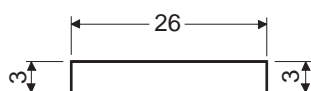


- C1, C2: Variable Capacitor (10pF MAX)
 C3: Disk Capacitor (1000pF)
 C4 to C6: Air Capacitor (1000pF)
 R1: 180 k Ω
 R2: 47 k Ω
 R3: 4.7 k Ω

L1:

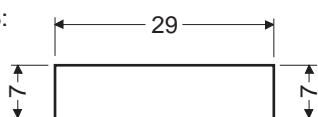


L2:

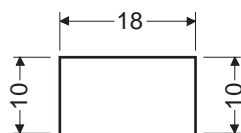


(ϕ 1mm Copper wire)
 Unit: mm

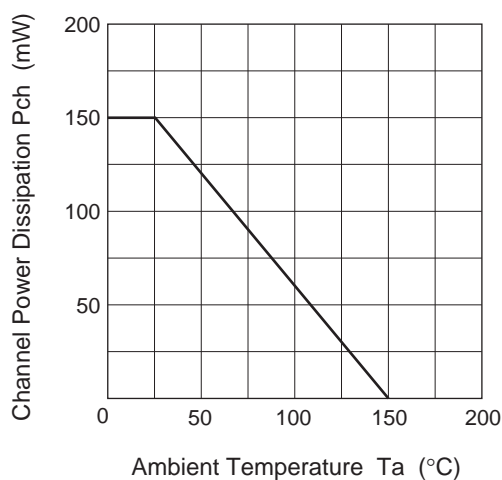
L3:



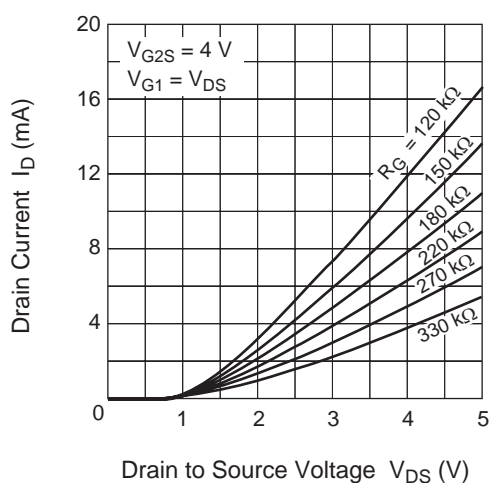
L4:



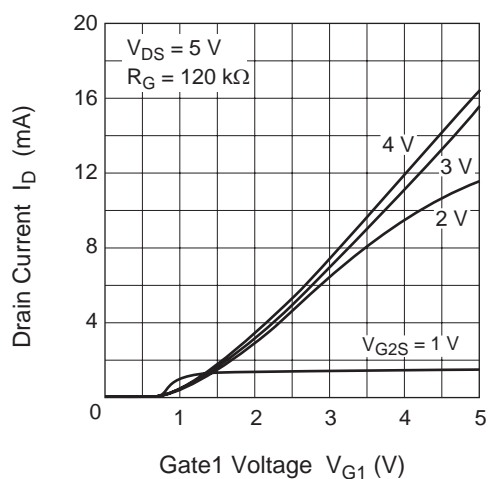
RFC: ϕ 1mm Copper wire with enamel 4turns inside dia 6mm

Maximum Channel Power
Dissipation Curve

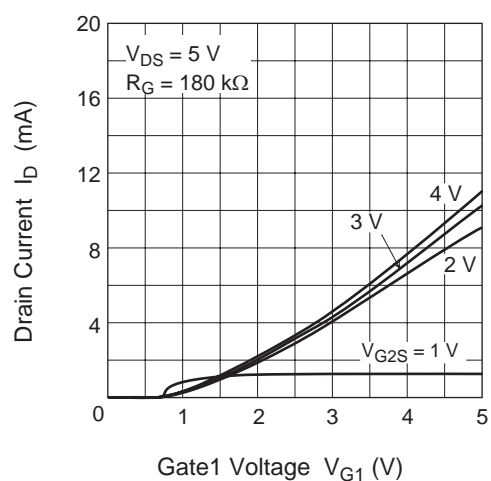
Typical Output Characteristics



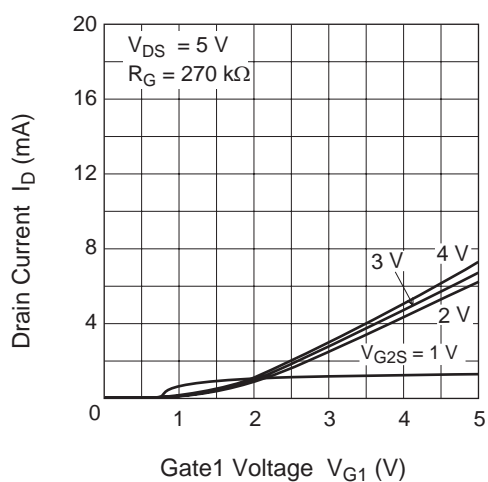
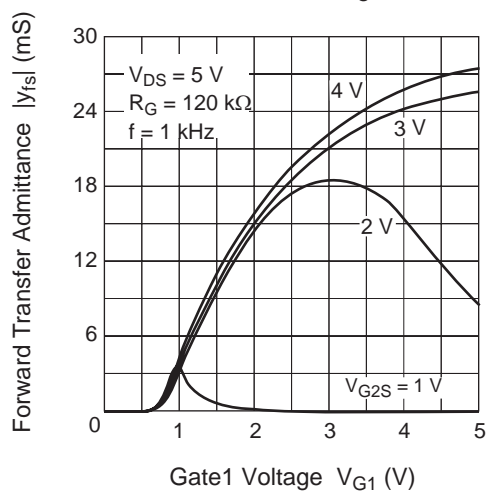
Drain Current vs. Gate1 Voltage

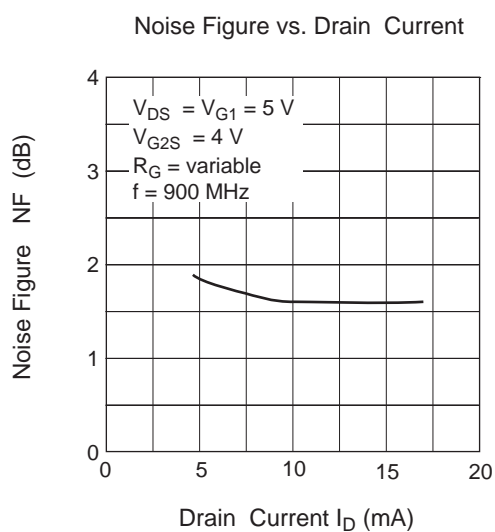
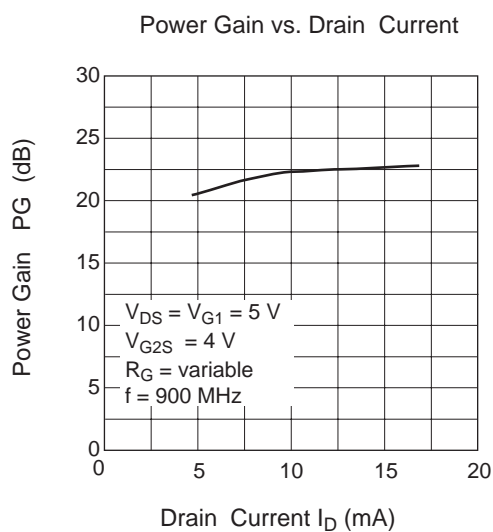
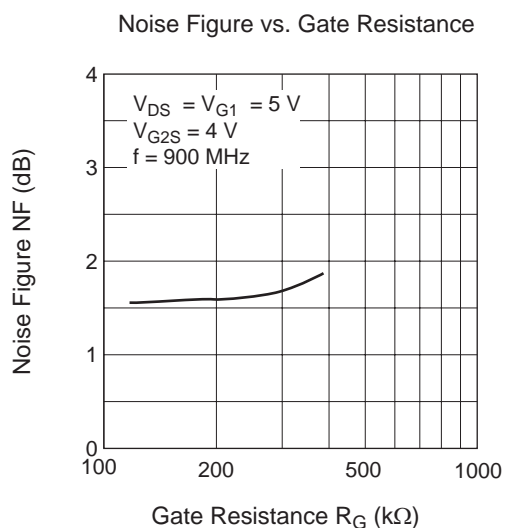
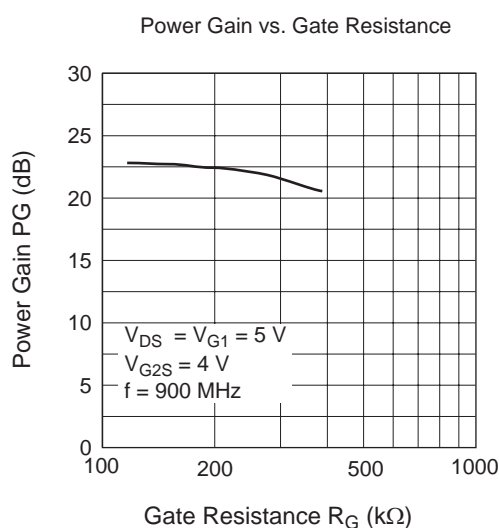
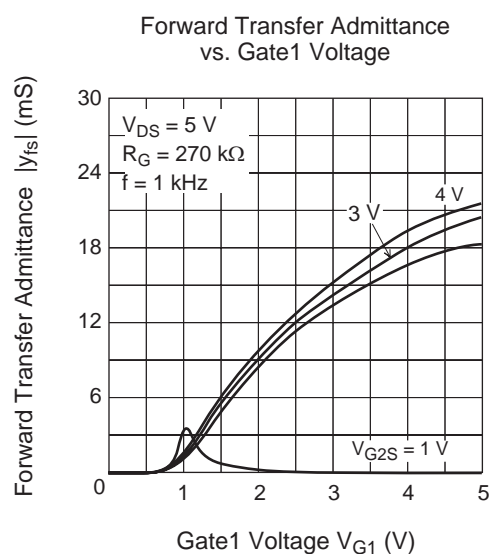
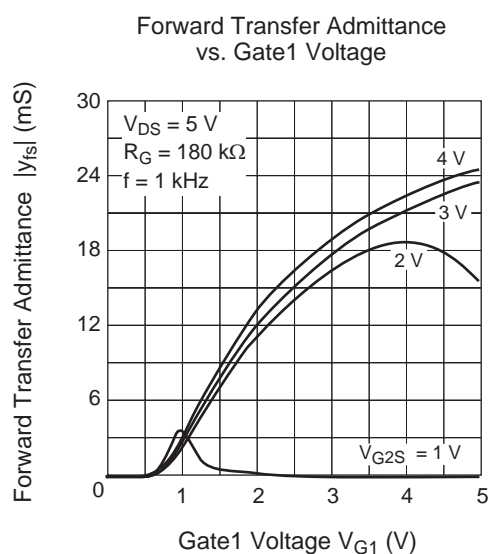


Drain Current vs. Gate1 Voltage

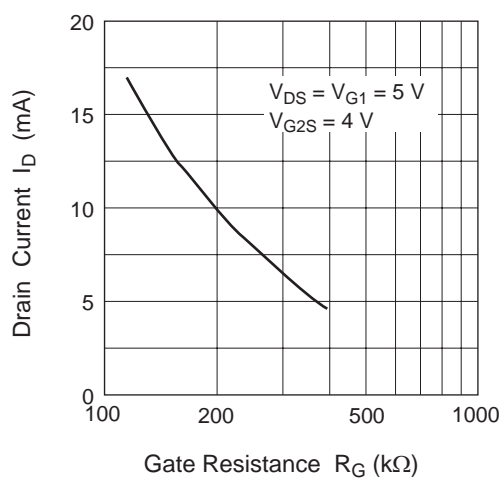


Drain Current vs. Gate1 Voltage

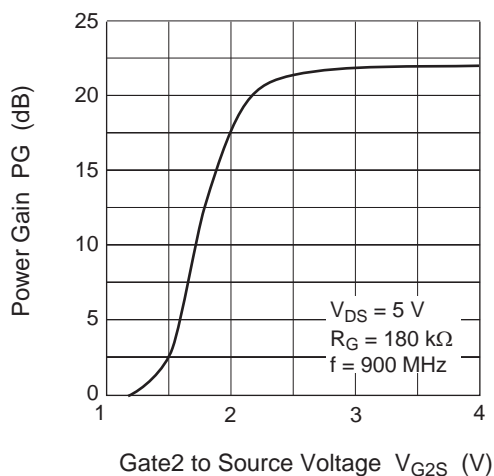
Forward Transfer Admittance
vs. Gate1 Voltage



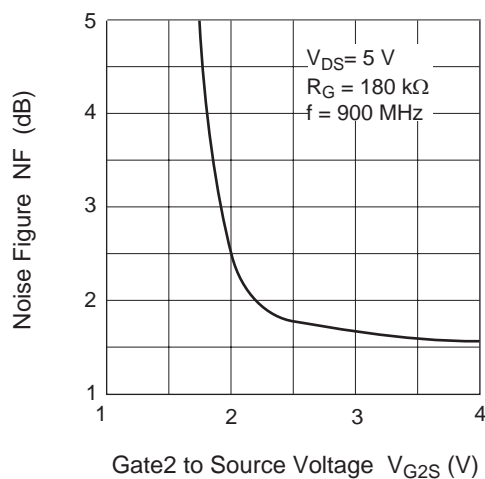
Drain Current vs. Gate Resistance



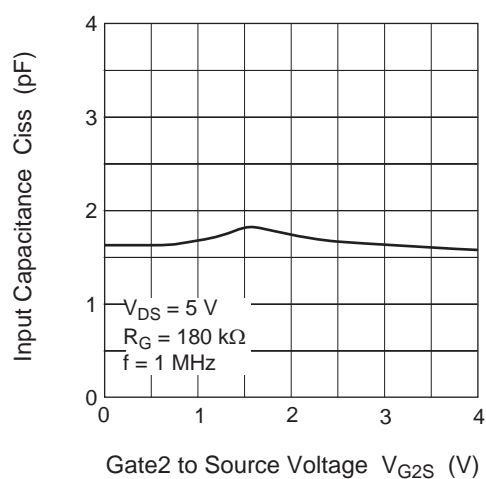
Power Gain vs. Gate2 to Source Voltage



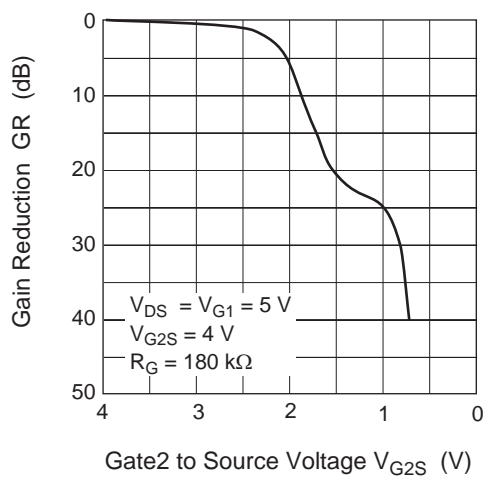
Noise Figure vs. Gate2 to Source Voltage



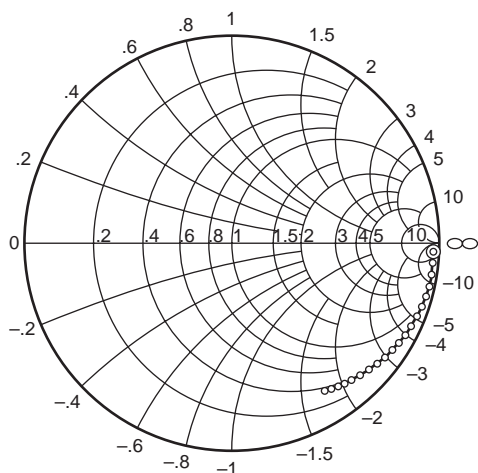
Input Capacitance vs. Gate2 to Source Voltage



Gain Reduction vs. Gate2 to Source Voltage



S11 Parameter vs. Frequency

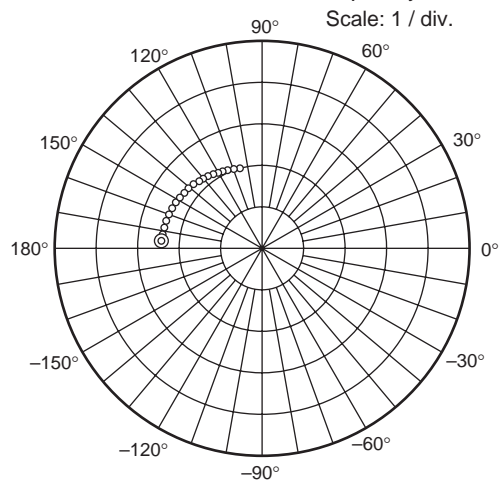


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 180\text{ k}\Omega$,
 $Z_0 = 50\Omega$

50 to 1000 MHz (50 MHz step)



S21 Parameter vs. Frequency

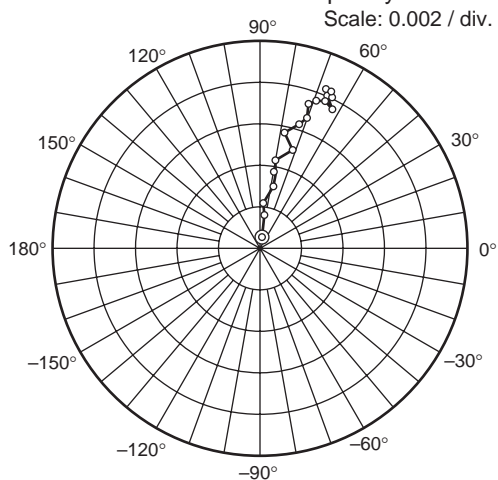


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 180\text{ k}\Omega$,
 $Z_0 = 50\Omega$

50 to 1000 MHz (50 MHz step)



S12 Parameter vs. Frequency

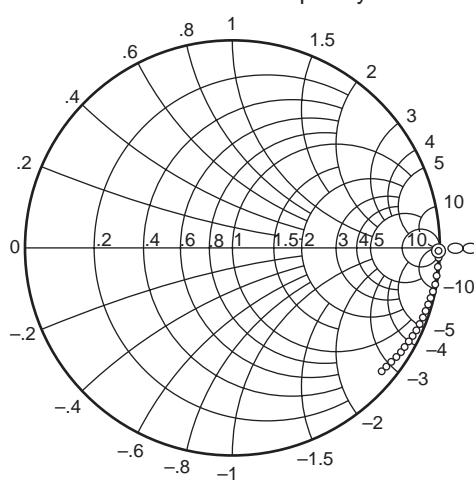


Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 180\text{ k}\Omega$,
 $Z_0 = 50\Omega$

50 to 1000 MHz (50 MHz step)



S22 Parameter vs. Frequency



Test Condition: $V_{DS} = 5\text{ V}$, $V_{G1} = 5\text{ V}$
 $V_{G2S} = 4\text{ V}$, $R_G = 180\text{ k}\Omega$,
 $Z_0 = 50\Omega$

50 to 1000 MHz (50 MHz step)

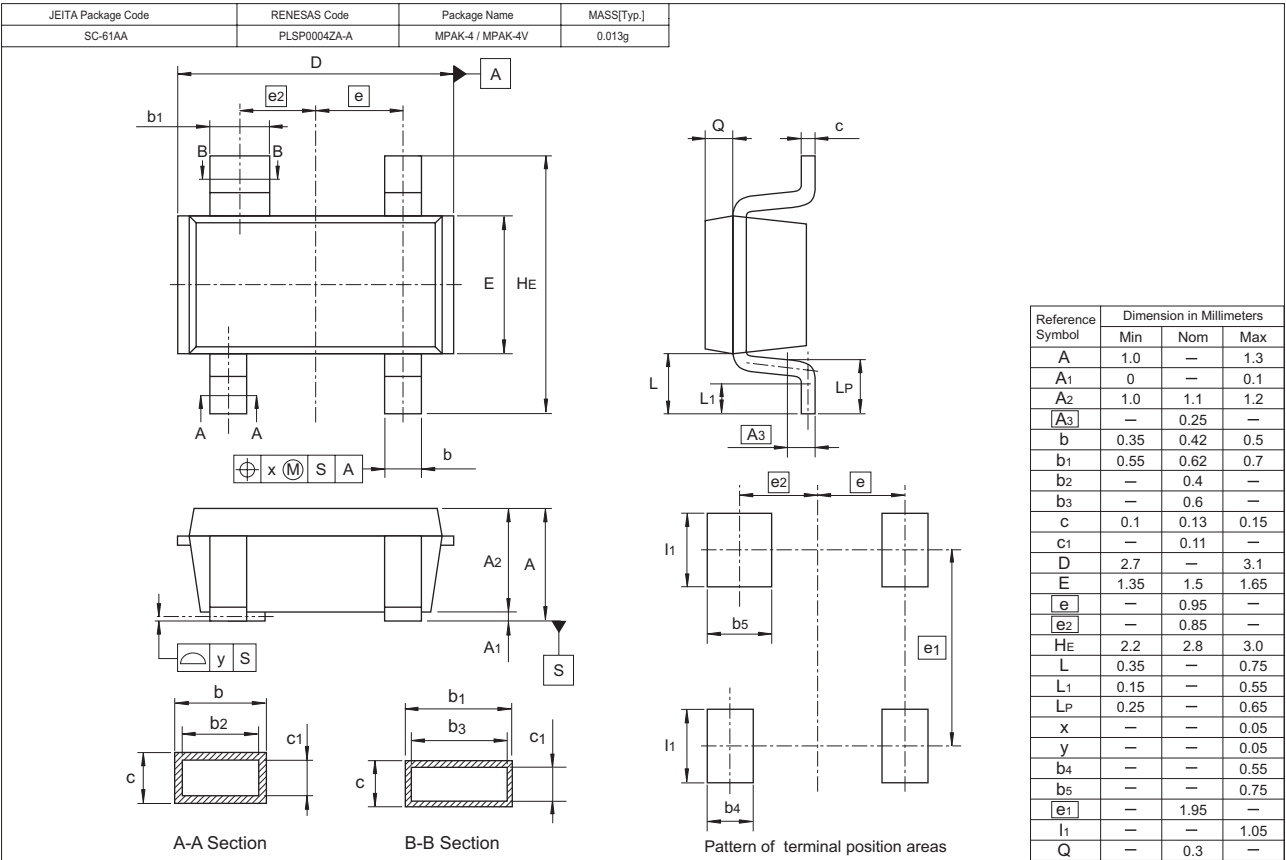


S Parameter

(V_{DS} = V_{G1} = 5V, V_{G2S} = 4V, R_G = 180kΩ, Z₀ = 50Ω)

f(MHz)	S11		S21		S12		S22	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
50	0.994	-2.8	2.52	176.2	0.00072	88.6	0.995	-2.2
100	0.994	-5.7	2.51	172.4	0.00161	80.9	0.998	-4.0
150	0.991	-9.2	2.50	168.1	0.00230	86.6	0.997	-6.2
200	0.985	-12.5	2.47	164.1	0.00297	78.0	0.996	-8.2
250	0.985	-15.5	2.46	160.0	0.00374	78.9	0.994	-10.2
300	0.975	-18.7	2.43	156.4	0.00436	80.6	0.992	-12.2
350	0.969	-22.0	2.40	152.3	0.00507	70.9	0.990	-14.2
400	0.962	-24.9	2.38	148.6	0.00557	77.3	0.989	-16.3
450	0.954	-27.7	2.35	144.6	0.00625	72.4	0.987	-18.5
500	0.945	-30.8	2.31	141.0	0.00663	70.0	0.984	-20.4
550	0.935	-33.8	2.28	136.7	0.00721	70.5	0.981	-22.4
600	0.925	-36.6	2.25	133.4	0.00747	68.4	0.978	-24.3
650	0.918	-39.5	2.21	130.3	0.00761	65.6	0.975	-26.4
700	0.909	-42.5	2.18	126.1	0.00807	65.6	0.972	-28.3
750	0.898	-45.0	2.14	122.9	0.00828	67.6	0.969	-30.2
800	0.887	-47.8	2.09	119.5	0.00801	65.1	0.965	-32.2
850	0.874	-50.6	2.07	116.0	0.00815	63.6	0.961	-34.2
900	0.862	-53.0	2.03	112.7	0.00832	65.1	0.958	-36.1
950	0.855	-55.5	1.99	109.4	0.00738	61.8	0.954	-37.9
1000	0.845	-58.1	1.95	106.1	0.00802	65.8	0.951	-39.8

Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
BB502MBS-TL-E	3000	φ 178 mm Reel, 8 mm Emboss Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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