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BCM5770/BCM5770R PRODUCT Brief

HIGH-PERFORMANCE 8/4-PORT SATA-I ← → PCI-X® CONTROLLERS

BCM5770/BCM5770R FEATURES

- **Industry's first 0.13µ CMOS SATA-I Controllers**
- **8 (BCM5770) and 4 (BCM5770R) ports**
- **Integrated high-performance 1.5G SATA PHY**
  - Enhanced support for driving backplanes
- **Host interfaces**
  - PCI-X 1.0 66, 100, and 133 MHz
  - PCI 2.3 32-bit and 64-bit interfaces
- **High-performance QDMA™ engine lowers CPU utilization, increases IOPS and throughput**
  - Ultra-deep command queues for command queuing
  - 256 independent command queue entries per port
  - Independent scatter gather DMA engines
  - Advanced interrupt coalescing algorithms
- **Automatic status block update**
  - Decrease CPU utilization associated with READ wait time
  - Increase efficiency of PCI-X host interface
- **Integrated PRBS generator and monitor**
- **Hot-plug support**

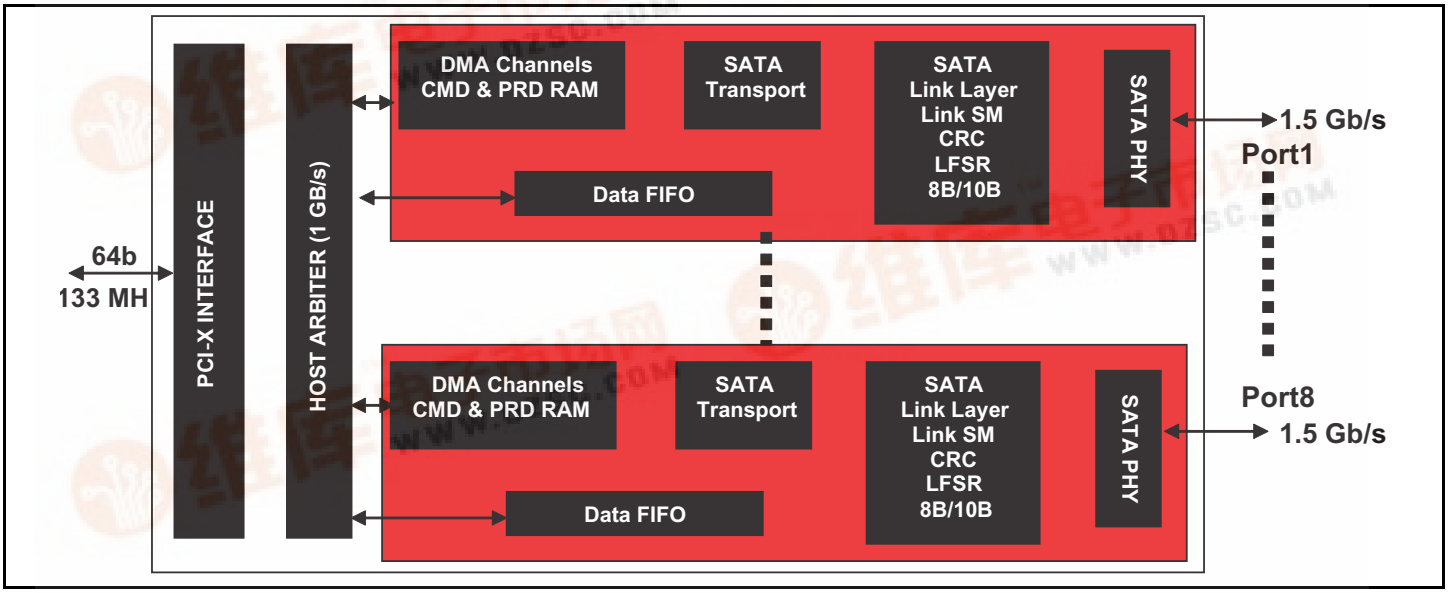
FEATURES (CONTINUED)

- **Enclosure management support**
- **8-port and 4-port versions are pin-compatible**
- **324 P-BGA packages**
- **1.68W max (BCM5770)**
- **1.36W max (BCM5770R)**
- **Driver support**
  - Windows®
  - Linux®

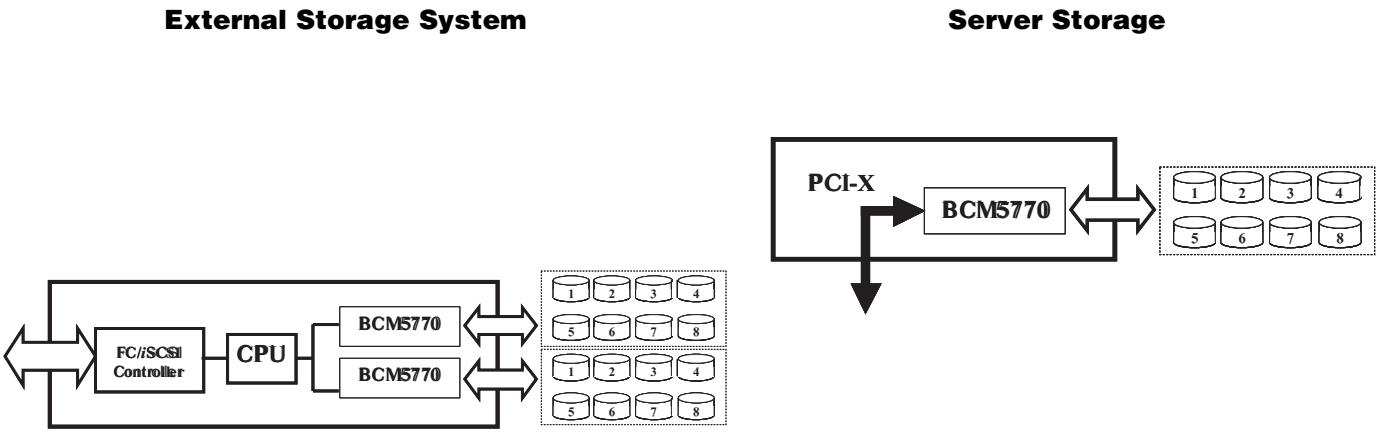
APPLICATIONS

- **Embedded on a motherboard**
- **DAS RAID HBA**
- **External RAID storage**

BCM5770/BCM5770R Block Diagram



OVERVIEW



BCM5770/BCM5770R Applications

The BCM5770/BCM5770R is a highly integrated, multiport SATA-I controller that has been designed for high performance storage applications requiring low host CPU utilization and maximum I/O performance.

The device communicates with the host via a 64-bit, 133-MHz PCI-X1.0 bus interface. It attaches directly to a maximum of eight SATA-I disk drives or to backplanes on the target side via a high-performance, integrated SATA PHY that is capable of driving long-length backplanes. Additionally, the BCM5770/BCM5770R supports hot-plug capability, enabling SATA disk drives to be inserted and removed from a storage rack or server without affecting system operation.

A high-bandwidth host arbiter (1 GB/s) decouples the PCI-X host interface from the SATA ports, enabling maximum throughput for workloads demanding sequential I/O performance.

Data from/to the drives are broken into 8-KB data FISes on the SATA links. The PCIX interface is arbitrated based on a round robin or LRU algorithm. Data is transferred in 512-byte blocks on the PCIX, thereby allowing fairness among the data channels.

The BCM5770/BCM5770R provides an interrupt coalescing mechanism to pace the host interrupts it generates. This allows host software to batch-process interrupts efficiently. In addition, the BCM5770/BCM5770R incorporates a mechanism to reduce IO reads by periodically DMAing the BCM5770/BCM5770R status block into host memory. Both of these mechanisms vastly reduce the host CPU utilization by limiting the amount of adaptor accesses that must be performed.

A Low Pin Count (LPC) Interface Specification 1.0 compliant interface is available to connect the BCM5770/BCM5770R to an external flash/ROM up to 128 KB. Three general-purpose I/O pins with tri-state capability are available and can be specially configured to drive LEDs. An I^2C master interface is also available to communicate with an external enclosure management device or with a serial EEPROM.

On-board power supply regulators are available that generate local 2.5V and 1.2V rails, allowing the entire chip to run from a single external 3.3V power source.

Built-in PRBS or pseudo-random bit sequence test generators/checkers are available per port for PHY testing without the use of additional hardware or drives. These are programmed from the in-band PCI interface.

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