

**ROHM**

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STRUCTURE Silicon Monolithic Integrated Circuit  
 TYPE System Regulator (RESET, Vcc-Detection Circuit and 150mA LDO)

PRODUCT SERIES **BD3951F**

FEATURES With low ESR capacitor for output

○ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Vcc Input Voltage	Vcc	-0.3~+36	V
OUT Terminal Voltage	Vout	-0.3~+7	V
RES Terminal Voltage	Vres	-0.3~+7	V
SOUT Terminal Voltage	Vsout	-0.3~+7	V
RES Output Current	Ires	0.2	mA
SOUT Output Current	Isout	2.5	mA
SIN Input Voltage	Vsin	-0.3~+36(3)	V
Power Dissipation	Pd	687(2)	mW
Operating Temperature Range	Topr	-40~+125	°C
Storage Temperature Range	Tstg	-55~+150	°C
Vcc Peak Input Voltage	Vccpeak	50(1)	V

- (1) tr(rising time) is over 1msec, applied voltage is less than 400msec
- (2) Pd is derated at 5.5mW/°C for temperature above Ta=25°C, mounted on 70mm×70mm×1.6mm PCB.
- (3) Input current from Vcc to SIN PIN has to be equal and less than 5mA when Vcc voltage is less than SIN PIN voltage.

○OPERATING CONDITIONS (Ta=-40~125°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	Unit
Recommended Supply Voltage *	Vcc	6.0	13.5	20	V
Function Available Supply Voltage **	Vcc	5.5	13.5	36	V
Reset Adjustable Range	Vdet	4	-	4.7	V
Reset Delay Time Controllable Range	Cct	-	-	10	μF
Vcc Detection Adjustable Range	Vcc	5	-	-	V

\*NOTE: The above conditions may not meet electrical characteristic.

\*\*Basic Function Available range, for example the Regulation etc.

\*This Product is not designed for protection against radio active rays.

\*This product described in this specification isn't judged whether it applies to COCOM regulations,  
 Please confirm in case of export.



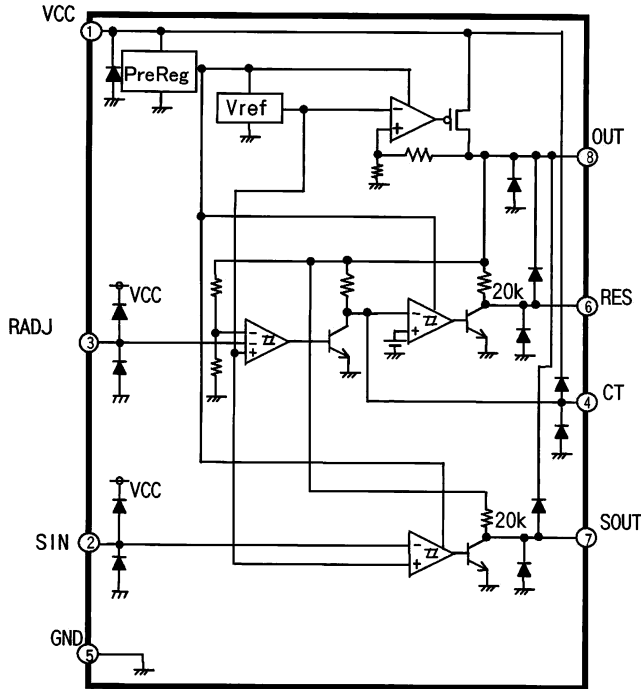
○ELECTRICAL CHARACTERISTIC (Ta=-40°C~125°C, Vcc=13.5V unless otherwise specified)

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITIONS
		MIN.	TYP.	MAX.		
[Whole Devices]						
Input Current	Icc	-	135	210	μA	Iout=0.3mA
[Regulator Block]						
Output Voltage	Vout	4.90	5.00	5.10	V	Vcc=6~20V, Iout=1~100mA
Line Regulation	Lin.Reg	-	10	20	mV	Vcc=6~20V
Load Regulation	Load.Reg	-	15	30	mV	Iout=1~100mA
Dropout Voltage	ΔVd	-	0.31	0.50	V	Vcc=4.75V, Io=100mA
Output Peak Current	Iomax	150	-	-	mA	(Current Limit)
[Reset Block]						
Threshold Voltage	Vdet	Vout ×0.92	Vout ×0.94	Vout ×0.96	V	
Hysteresis Voltage	Vhys	50	100	150	mV	
Reset Delay Time L→H	TdLH	17	30	-	mS	CT=0.1 μF (3)
Reset Delay Time H→L	TdHL	-	4	-	μS	CT=0.1 μF
RES Pull Up Resistor	Rrst	10	20	40	kΩ	
RES Low Output Voltage	VrL	-	0.08	0.40	V	4V<Vout<Vdet, INPUT CURRENT is 0.2mA
Reset Adjust Voltage	Vradj	1.18	1.26	1.34	V	
[Vcc DETECTION BLOCK]						
Threshold Voltage	Vsdet	1.19	1.26	1.33	V	
Hysteresis Voltage	Vsdet off	1.240	1.335	1.430	V	
SOUT Pull Up Resistor	Rso	10	20	40	kΩ	
SOUT Low Output Voltage	VsL	-	0.06	0.40	V	Vout>4V, VSIN<Vsdet, INPUT CURRENT is 1.5mA
SIN Input Current	I <sub>sin</sub>	-1	0	1	μA	V <sub>sin</sub> =2V

NOTE: (3) TdLH set by Cct terminal capacitor.

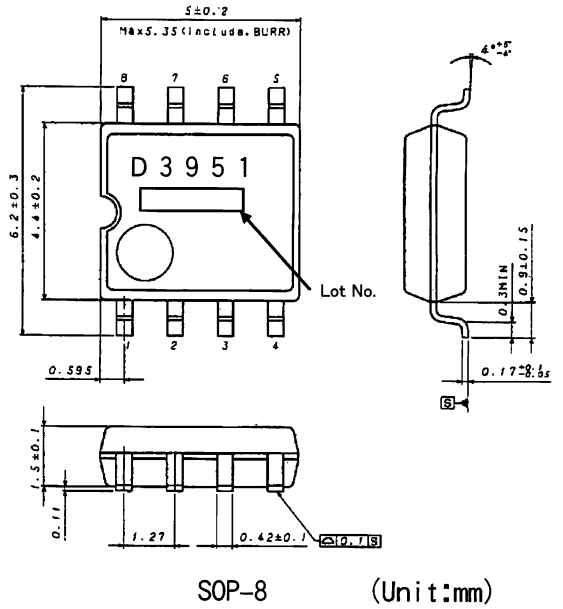
$$TdLH \approx 300k \times Cct$$

○BLOCK DIAGRAM, APPLICATION CIRCUIT



※Refer to the Technical Note about the details of the application.

○PHYSICAL DIMENSION



○PIN No. PIN name

PIN No.	PIN name
1	VCC
2	SIN
3	RADJ
4	CT
5	GND
6	RES
7	SOUT
8	OUT

## ○ NOTES FOR USE

1. Absolute maximum range  
This product are produced with strict quality control, but might be destroyed in using beyond absolute maximum ratings. The destroyed IC failure mode cannot be defined (like Short mode, or Open mode).  
Therefore physical security countermeasure, like fuse, is to be used when a specified mode is beyond absolute maximum ratings.
2. Operating supply voltage range  
BD3951F can operate within the operating supply voltage range and operating temperature range.  
Limits in the electrical characteristic table are not warranted. There is a little difference between the limits and electrical values.
3. GND terminal voltage must be always forced with the lowest voltage among the terminals.
4. Power GND pattern and Small signal GND pattern should be separated each other and supplied one point GND on the board to eliminate the surge current influences.
5. Power dissipation  
For power dissipation, refer to the thermal reducing characteristics and the approximation of IC internal power consumption shown in the attached sheet as guideline. Be sure to use this IC within the power dissipation range, allowing enough of margin.
6. Shorted terminals and Mounting Error  
Short circuits among the output terminals and short circuits between output terminals and VCC/GND terminal due to metallic foreign particles would result in permanent damage to the device. And this IC Pin Assignment is 1pin=Vcc, 5pin=GND. So if this IC is mounted upside down, it would be destroyed by the huge current from GND to Vcc. Please be careful to the mount destination.
7. The extent electromagnetic condition might cause wrong operation of BD3951F.
8. Note that running set testing procedure using capacitors connected to low-impedence terminals may produce stress on the IC. Therefore, be certain to use proper discharge procedure before each process of the Testing. To prevent electrostatic stress in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to any component to the test system, make certain that the power supply is OFF. Likewise, be sure to turn the power supply OFF before removing any component connected to the test system.
9. This IC is a Monolithic IC which has P+ isolation in the P substrate and between the various pins. A P-N junction is formed from this P layer and the N layer of each pin.  
Parasitic diodes can occur inevitably in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits as well as operation faults and physical damage.  
Accordingly, you must not use methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin.
10. About oscillation stopper of output and bypass capacitor  
Please use this to stop oscillation between OUT pin and GND. Ceramic Capacitor  $3.3\ \mu\text{F}\sim 2200\ \mu\text{F}$  can be used for this. When selecting the value of the output capacitor, please make sure that the operation on the actual application takes these conditions into account: rapid input or load transient response.
11. BD3951F might be damaged from the exceed inflow current from the terminals to VCC (for instance, VCC is short to GND while the output capacitor is charging.). In those cases, VCC series diode (to prevent inflow current) or bypass diode (connected from terminals to VCC) should be used externally in an application.
12. Over current protection circuit  
The over-current protection circuits are built in at the output, according to their respective current outputs. This prevents the IC from being damaged when the load is short-circuited or over-current. This protection circuit is designed not to occur latch-up against the unexpected huge current
13. BD3951F has thermal Shut Down protection (TSD) which performs Power Tr OFF in high Tj condition. Since TSD setting is higher temperature than absolute maximum ratings, thermal design must has done not to use this function.
14. We recommend to put a bypass capacitor  $0.33\ \mu\text{F}\sim 10\text{mF}$  into the nearest position between VCC pin and GND
15. Please insert power zenner diode between VCC terminal and GND terminal, if more than 50V surge voltage would be supplied to VCC terminals.
16. The SOUT terminal is only activated ( "H" / "L" ) while the RESET is "H" . While the RESET terminal is "L" , the SOUT terminal is always "L" .

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