STRUCTURE	Silicon Monolithic Integrated Circuit
TYPE	Power switch for ExpressCard™
PRODUCT SERIES	**BD4155FV**
FEATURE	・High Side switch for ExpressCard™
	・Soft Start Circuit
	・Meets the ExpressCard™ Standard

○ ABSOLUTE MAXIMUM RATINGS（Ta=100℃）

Parameter	Symbol	Limit	Unit
Input Voltage	V3AUX_IN, V3_IN, V15_IN	-0.3～+5.0 *1	V
Logic Input Voltage	CPPE#,CPUSB#,SYSR,EC_CLKREQ#, EC_CLKEN#,EC_RST#,PLT_RST#	-0.3～V3AUX_IN+0.3 *1	V
Logic Output Voltage	PERST#	-0.3～V3AUX_IN+0.3	V
Logic Output applied Voltage	PLL_CLKREQ#	-0.3～+5.0	V
Output Voltage	V3AUX,V3, V15	-0.3～+5.0 *1	V
Output current 1	IOV3AUX	1.0	A
Output current 2	IOV3	2.0	A
Output current 3	IOV15	2.0	A
Power Dissipation 1	Pd1	500 *2	mW
Power Dissipation 2	Pd2	812.5 *3	mW
Operating Temperature Range	Topr	-40～+100	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

*1 Not to exceed Pd.
*2 Reduced by 4.0mW for each increase in Ta of 1℃ over 25℃
*3 Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃(When mounted on a board 70mm×70mm×1.6mm Glass-epoxy PCB).

○ RECOMMENDED OPERATING CONDITIONS（Ta=25℃）

Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	V3AUX_IN	3.0	3.6	V
Input Voltage 2	V3_IN	3.0	3.6	V
Input Voltage 3	V15_IN	1.35	1.65	V
Logic Input Voltage	CPPE#,CPUSB#,SYSR,EC_CLKREQ#, EC_CLKEN#,EC_RST#,PLT_RST#	0	V3AUX_IN	V
Logic Output Voltage 1	PERST#	0	V3AUX_IN	V
Logic Output Voltage 2	PLL_CLKREQ#	0	3.6	V
Output current 1	IOV3AUX	0	275	mA
Output current 2	IOV3	0	1.3	A
Output current 3	IOV15	0	650	mA

★ This product is designed for protection against radioactive rays.

Status of this document
The English version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

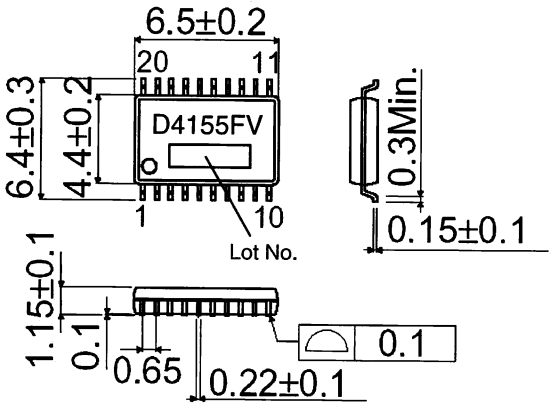
"ExpressCard™" is a trademark registered by PCMCIA(Personal Computer Memory Card International Association).

○ELECTRICAL CHARACTERISTICS (unless otherwise noted, Ta=25℃ V3AUX_IN =V3_IN=3.3V,V15_IN=1.5V)

Parameter	Symbol	Standard Value			Unit	Condition
		MIN	TYP	MAX		
Standby current	Icc1	-	120	250	uA	VSYSR=0V
Bias current	Icc2	-	250	500	uA	VSYSR=3.3V
[Logic]						
High Level Enable Input Voltage	VL_{HI}	2.0	-	-	V	
Low Level Enable Input Voltage	VL_{LOW}	-	-	0.8	V	
Input current	ICPPE#	-	0	1	uA	CPPE#=3.6V
		10	-	30	uA	CPPE#=0V
	ICPUSB#	-	0	1	uA	CPUSB#=3.6V
		10	-	30	uA	CPUSB#=0V
	ISYSR	-1	0	1	uA	SYSR=3.6V
	IEC_CLKEN#	5	0	20	uA	EC_CLKEN#=3.6V
	IEC_CLKREQ#	-1	0	1	uA	EC_CLKREQ#=3.6V
	IEC_RST#	-1	0	1	uA	EC_RST#=3.6V
	IPLT_RST#	-1	0	1	uA	PLT_RST#=3.6V
[Switch V3AUX]						
On Resistance	R_{V3AUX}	-	120	220	mΩ	Tj=-10~100℃ *
Discharge On Resistance	R_{V3AUX}Dis	-	60	150	Ω	
[Switch V3]						
On Resistance	R_{V3}	-	42	90	mΩ	Tj=-10~100℃ *
Discharge On Resistance	R_{V3}Dis	-	60	150	Ω	
[Switch V15]						
On Resistance	R_{V15}	-	45	90	mΩ	Tj=-10~100℃ *
Discharge On Resistance	R_{V15}Dis	-	60	150	Ω	
[Over Current Protection]						
V3 Over current	OCP_{V3}	1.6	-	-	A	
V3AUX Over current	$OCPV_{3AUX}$	0.35	-	-	A	
V15 Over current	OCP_{V15}	0.8	-	-	A	
[Low input miss operation prevent Block]						
V3_IN threshold voltage	$VUVLO_{V3\_IN}$	2.70	2.80	2.90	V	sweep up
V3_IN hysteresis Voltage	$\Delta VUVLO_{V3\_IN}$	50	100	150	mV	sweep down
V3AUX_IN threshold voltage	$VUVLO_{V3AUX\_IN}$	2.70	2.80	2.90	V	sweep up
V3AUX_IN hysteresis Voltage	$\Delta VUVLO_{V3AUX\_IN}$	50	100	150	mV	sweep down
V15_IN threshold voltage	$VUVLO_{V15\_IN}$	1.15	1.20	1.25	V	sweep up
V15_IN hysteresis Voltage	$\Delta VUVLO_{V15\_IN}$	50	100	150	mV	sweep down
[POWER GOOD]						
V3 POWER GOOD Voltage	PG_{V3}	2.700	2.850	3.000	V	
V3AUX POWER GOOD Voltage	PG_{V3AUX}	2.700	2.850	3.000	V	
V15 POWER GOOD Voltage	PG_{V15}	1.200	1.275	1.350	V	
PERST# LOW Voltage	$VPERST\#_{Low}$	-	0.1	0.3	V	I_{PERST}=0.5mA
PERST# HIGH Voltage	$VPERST\#_{HIGH}$	3.0	-	-	V	
PERST Delay	$T_{PERST\#}$	4	10	20	ms	
PLL_CLKREQ# Low Voltage	V_{PLL}	-	0.1	0.2	V	$I_{PLL\_CLKREQ\#}$=0.5mA
PLL_CLKREQ# Leak Current	I_{PLL}	-	-	1	uA	$V_{PLL\_CLKREQ\#}$=3.6V
[WAKE UP TIME]						
V3_IN to V3	T_{V3}	0.1	-	3	ms	
V3AUX_IN to V3AUX	T_{V3AUX}	0.1	-	3	ms	
V15_IN to V15	T_{V15}	0.1	-	3	ms	

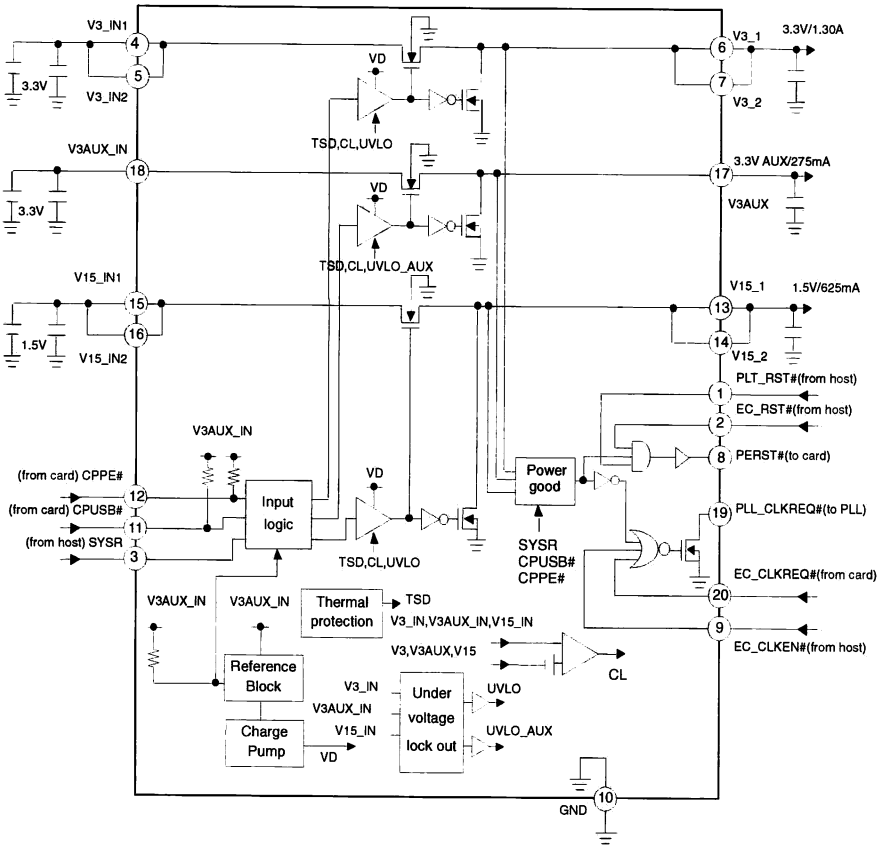
* Design Guarantee

O PHYSICAL DIMENSION



SSOP-B20 (UNIT:mm)

O BLOCK DIAGRAM



O PIN DESCRIPTION

PIN No.	Pin name
1	PLT_RST#
2	EC_RST#
3	SYSR
4	V3_IN1
5	V3_IN2
6	V3_1
7	V3_2
8	PERST#
9	EC_CLKEN#
10	GND
11	CPUSB#
12	CPPE#
13	V15_1
14	V15_2
15	V15_IN1
16	V15_IN2
17	V3AUX
18	V3AUX_IN
19	PLL_CLKREQ#
20	EC_CLKREQ#

ONOTES FOR USE

(1) Absolute maximum range
Although the quality of this product is rigorously controlled, and circuit operation is guaranteed within the operation ambient temperature range, the device may be destroyed when applied voltage or operating temperature exceeds its absolute maximum rating. Because the failure mode (such as short mode or open mode) cannot be identified in this instance, it is important to take physical safety measures such as fusing if a specific mode in excess of absolute rating limits is considered for implementation.

(2) Ground potential
Make sure the potential for the GND pin is always kept lower than the potentials of all other pins, regardless of the operating mode, including transient conditions.

(3) Thermal Design
In order to build sufficient margin into the thermal design, give proper consideration to the allowable loss (Power Dissipation) in actual operation.

(4) Using in the strong electromagnetic field
Use in strong electromagnetic fields may cause malfunctions.

(5) ASO
Be sure that the output transistor for this IC does not exceed the absolute maximum ratings or ASO value.

(6) Thermal shutdown circuit
The IC is provided with a built-in thermal shutdown (TSD) circuit. When chip temperature reaches the threshold temperature shown below, output goes to a cut-off (open) state. Note that the TSD circuit is designed exclusively to shut down the IC in abnormal thermal conditions. It is not intended to protect the IC per se or guarantee performance when extreme heat occurs. Therefore, the TSD circuit should not be employed with the expectation of continued use or subsequent operation once TSD is operated.

TSD ON temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
175	15

(7) GND pattern
When both a small-signal GND and high current GND are present, single-point grounding (at the set standard point) is recommended, in order to separate the small-signal and high current patterns, and to be sure the voltage change stemming from the wiring resistance and high current does not cause any voltage change in the small-signal GND. In the same way, care must be taken to avoid wiring pattern fluctuations in any connected external component GND.

(8) Electrical Characteristics
Be sure to check the electrical characteristics, such as transient characteristics in the present specification, since these can be changed by temperature, supply voltage, and external circuits.

(9) Input Capacitor
The input capacitor reduces the output impedence of the voltage supply source. If the output impedence of this power supply increases, the input voltage (V3_IN,V3AUX_IN,V15_IN) may become unstable. A 0.1uF capacitor for the V3AUX_IN pin, and a 1uF capacitor for V3_IN and V15_IN pin are recommended. A low ESR capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

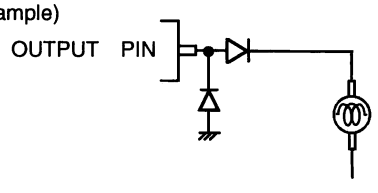
(10) Output Capacitor
Mount an output capacitor between output pin (V3,V3AUX,V15)and GND for stability purposes. A 10uF capacitor for the V3 and V15 pin, and a 1uF capacitor for the V3AUX pin are recommended. A low ESR capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.

(11) Short-circuits between pins and and mounting errors
When mounting the IC onto a set substrate or circuit board, be careful to avoid incorrect orientation or mis-positioning of the IC, as such mounting errors may cause device malfunctions. Similar damage may occur when the power supply connection is reversed. Also, note that the introduction of foreign material between pins and the GND, or between the pins themselves may cause shorts and destroy the IC.

(12) Power dissipation
When exercising modes that exceed Pd, there is a risk that IC characteristics, such as current capability, may be negatively impacted by the rise in chip temperature. Provide sufficient margin in the thermal design to account for the allowable power dissipation (Pd) expected in actual use.

(13) Please add a protection diode when a large inductance
component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.

(Example)



(14) Operating Conditions
The circuit functionality is guaranteed within the operating ambient temperature range. The standard electrical characteristics cannot be guaranteed, except at Ta=25°C. However, any variation will be small.

(15) Operating stability depends on the layout pattern. Make sure the wiring pattern for the input (V3_IN, V3AUX_IN, V15_IN) and the output (V3, V3AUX, V15) on the application board is designed wide and short , in order to minimize layout impedance.

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