



Structure Silicon monolithic integrated circuit
 Product High Side Switch
 Type **BD6519FJ**
 Features 100mΩ (V_{DD}=5V, Typ) High Side Switch
 Over current detector, Thermal shutdown, UVLO
 Control Logic : Active Low

◇Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V _{DD}	-0.3 ~ 6.0	V
Control input voltage	V _{CTRL}	-0.3 ~ V _{DD} + 0.3	V
Flag voltage	V _{FLAG}	-0.3 ~ 6.0	V
Flag Current	I _{FLAG}	10	mA
Output voltage	V _{OUT}	-0.3 ~ 6.0	V
Storage temperature	T _{STG}	-55 ~ 150	°C
Power dissipation *1	P _d	560	mW

*1 Derating : 4.48mW/°C for operation above Ta = 25°C

- * This product is not designed for protection against radioactive rays.
- * Operation is not guaranteed

◇Operating conditions

Parameter	Symbol	MIN	TYP	MAX	Unit
Supply voltage	V _{DD}	3.0	5.0	5.5	V
Operating temperature	T _{OPR}	-40	25	85	°C

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document, formal version takes priority.

Application example

- ROHM cannot provide adequate confirmation of patents.
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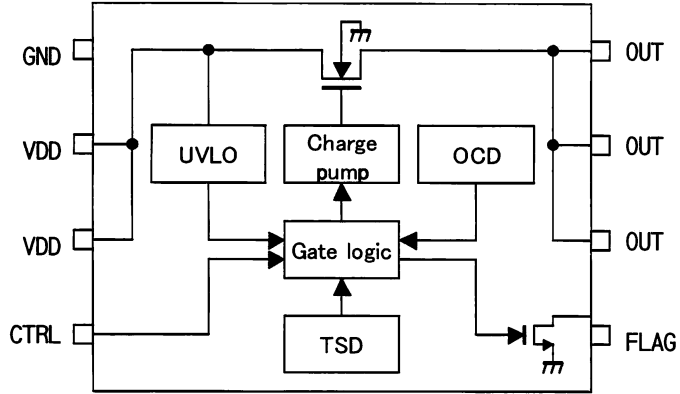


◇Electrical characteristics (Unless otherwise noted, $V_{DD} = 5V$, $T_a = 25^\circ C$)

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
Current consumption						
Supply current	I_{DD}	-	90	140	μA	$V_{CTRL} = 0V$, $OUT = OPEN$
		-	0.01	2	μA	$V_{CTRL} = 5V$, $OUT = OPEN$
I/O						
CTRL input voltage	V_{CTRL}	2.5	-	-	V	High level input voltage
		-	-	0.7	V	Low level input voltage
CTRL input current	I_{CTRL}	-1	0.01	1	μA	$V_{CTRL} = 0V$ or $5V$
Flag output resistance	R_{FLAG}	-	180	450	Ω	$I_{FLAG} = 1mA$
Flag output leak current	I_{LFLAG}	-	0.01	1	μA	$V_{FLAG} = 5V$
Flag output delay	T_{DFLAG}	-	2.5	8	ms	
Power switch						
ON resistance	R_{ON}	-	100	140	$m\Omega$	$V_{DD} = 5V$, $I_{OUT} = 500mA$
		-	140	180	$m\Omega$	$V_{DD} = 3.3V$, $I_{OUT} = 500mA$
Short circuit output current	I_{SC}	0.6	-	1.6	A	$V_{OUT} = 0V$
Output leak current	I_{LEAK}	-	-	10	μA	$V_{CTRL} = 5V$
Output rise time	T_{ON1}	-	1	4	ms	$R_L = 10\Omega$
Output turn on delay time	T_{ON2}	-	1.3	6	ms	$R_L = 10\Omega$
Output fall time	T_{OFF1}	-	1	20	μs	$R_L = 10\Omega$
Output turn off delay time	T_{OFF2}	-	3	20	μs	$R_L = 10\Omega$
Thermal shutdown threshold	T_{TS}	-	135	-	$^\circ C$	At T_j increase
UVLO						
UVLO threshold	V_{TUVH}	2.3	2.5	2.7	V	V_{DD} increasing
	V_{TUVL}	2.1	2.3	2.5	V	V_{DD} decreasing



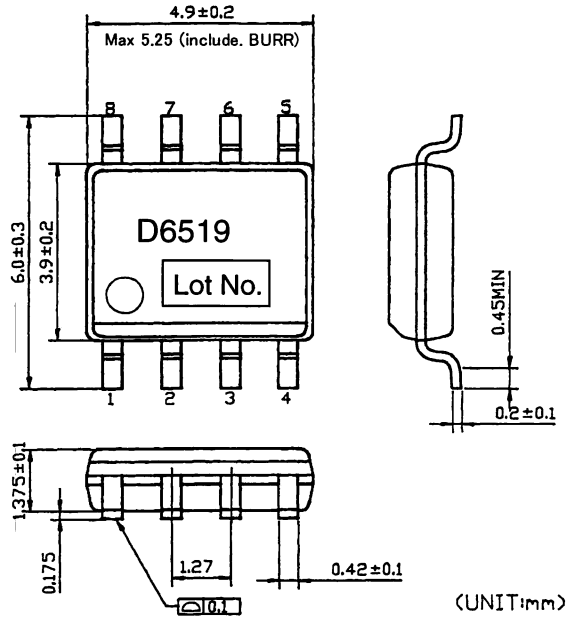
◇Block diagram



◇Pin description

Pin Number	Pin name	Pin Function
1	GND	Ground
2, 3	VDD	Supply Input Switch Input
4	CTRL	Enable Input
5	FLAG	Fault Flag Output
6, 7, 8	OUT	Switch Output

◇Package outline



(UNIT:mm)

図番: B1168

SOP-J8 (Unit : mm)

Rev. A



○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and GND line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and GND lines. Especially, when there are GND pattern for small signal and GND pattern for large current included the external circuits, separate each GND pattern. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(4) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(5) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)

When junction temperatures become 135°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design

Perform thermal design in which there are adequate margins by taking into account the power dissipation (Pd) in actual states of use.

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