



STRUCTURE Silicon Monolithic Integrated Circuit  
 PRODUCT NAME Driver For 3Phase Blushless Motor  
 TYPE **BD6922FV**  
 FEATURES •120° phase Direct PWM input  
 •Motor Lock Protection

○ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power Supply Voltage	VCC	36	V
Output Current	I <sub>OMAX</sub>	1300 *	mA
Input voltage	V <sub>IN</sub>	0~VCC	V
AL terminal voltage	V <sub>AL</sub>	36	V
AL output current	I <sub>ALMAX</sub>	5	mA
FG, FG3 terminal voltage	V <sub>FGMAX</sub>	36	V
FG, FG3 output current	I <sub>FGMAX</sub>	5	mA
Power dissipation	Pd	1025 **	mW
Operating temperature range	T <sub>opr</sub>	-40~+85	°C
Storage temperature range	T <sub>stg</sub>	-55~+150	°C
Junction temperature	T <sub>jmax</sub>	150	°C

\*1 Must not exceed Pd, ASO or T<sub>jmax</sub>=150°C.

\*2 Reduce by 8.2mW/°C over 25°C, when mounted on a glass epoxy board (70mm×70mm×1.6mm).

○Operating Conditions (Ta=-40~+85°C)

Power Supply voltage	VCC	8~28	V
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\*This product is not designed for normal operation within a radio active environment.

\*Status of this document

The Japanese version of this document is the formal specification.

A customer may use this translation version only for a reference to help reading the formal version.

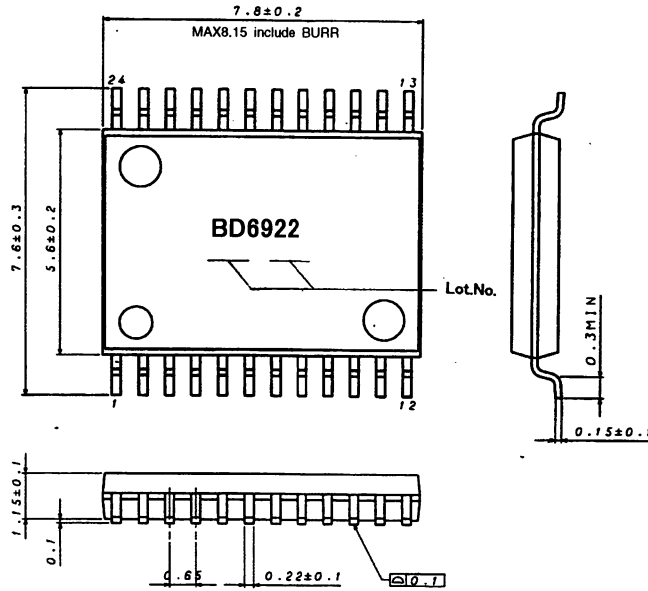
If there are any differences in translation version of this document, formal version takes priority.



**○Electrical Characteristics (Unless otherwise specified, Ta=25°C, VCC=12V)**

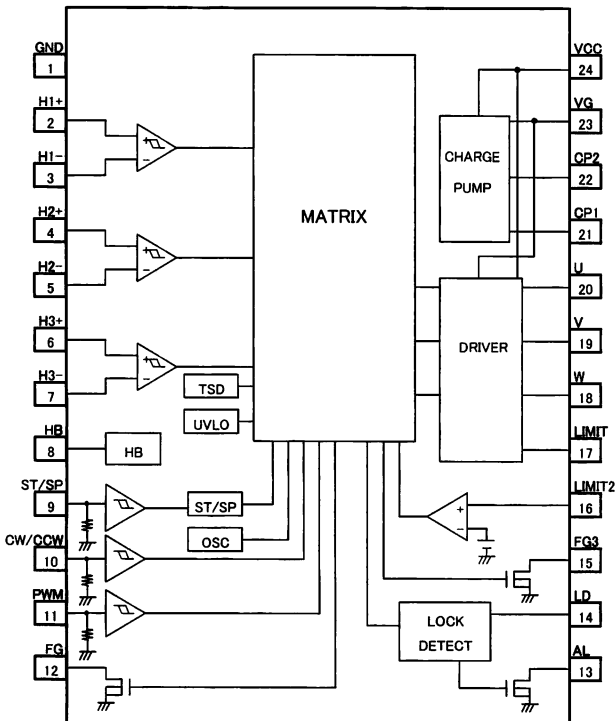
Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<Overall>						
Circuit Current 1	ICC1	4.3	10.5	14.9	mA	ST/SP=H
Circuit Current 2	ICC2	3.3	5.5	7.8	mA	ST/SP=L
<UVLO>						
UVLO detect voltage	VUVON	5.5	6.0	6.5	V	
UVLO off voltage	VUVOFF	6.0	6.5	7.0	V	
<ST/SP>						
ST voltage	VST	2.5	—	—	V	Start
SP voltage	VSP	—	—	1.0	V	Stop
Input current	IST	70	100	130	μA	VST=5V
<Hall Comparator>						
Input Bias current	IHA	-3.0	-0.7	-	μA	
Common phase input voltage range	VHAR	1.0	—	3.5	V	
Input level	VINH	60	—	—	mVpp	
hysteresis voltage H	VHYSH	7	14	21	mV	
hysteresis voltage L	VHYSL	-21	-14	-7	mV	
<Output>						
Upper side output on resister	RONH	0.3	0.5	0.7	Ω	I=-1.0A
Lower side output on resister	RONL	0.3	0.5	0.7	Ω	I=1.0A
Upper side output diode voltage	VDH	0.6	1.0	1.4	V	I=1.0A
Lower side output diode voltage	VDL	0.6	1.0	1.4	V	I=-1.0A
<Over current detection>						
Detection voltage	VTH	0.06	0.10	0.14	V	
Input Bias current	IIB	-5.0	-0.9	-	μA	
<Frequency for lock protection>						
frequency	FLOSC	9.6	13.7	17.8	Hz	C=0.47 μF
Triangle wave peak	VLDCL	1.96	2.8	3.64	V	
Triangle wave bottom	VLDCP	0.7	1.0	1.3	V	
Charge current	ILDC	-19.2	-13.5	-8.1	μA	VLD=1.2V
Lock detection output voltage	VALL	0.1	0.3	0.5	V	I <sub>AL</sub> =5mA
Lock detection output leak current	IALL	—	0	10	μA	
<PWM input>						
ON voltage	VPWMON	2.5	—	—	V	
OFF voltage	VPWMOF	—	—	1.0	V	
Input current	IPWMON	70	100	130	μA	VPWMON=5V
<FG(3) output>						
Output voltage	VFGL	0.1	0.3	0.5	V	I <sub>FG</sub> =5mA
Output leak current	I <sub>LEAKFG</sub>	—	—	10	μA	
<Hall Bias>						
Output voltage	VHB	0.60	0.92	1.24	V	I <sub>HB</sub> =10mA
Output leak current	I <sub>LEAKHB</sub>	—	—	10	μA	
<CW/CCW>						
CW voltage	VF	2.5	—	—	V	
CCW voltage	VR	—	—	1.0	V	
Input current	IVF	70	100	130	μA	VF=5V
<Booster>						
boost voltage	VG	12.3	18.3	23.8	V	C=0.1μF
boost frequency	f <sub>VG</sub>	15	25	35	kHz	

PHYSICAL DIMENSIONS • MARKING



SSOP-B24 (UNIT:mm)

○ BLOCK DIAGRAM



○ Pin No, Pin Name, Function

PIN No	Pin name	Function
1	GND	GND
2	H1+	Hall input H1+ pin
3	H1-	Hall input H1- pin
4	H2+	Hall input H2+ pin
5	H2-	Hall input H2- pin
6	H3+	Hall input H3+ pin
7	H3-	Hall input H3- pin
8	HB	Hall bias pin
9	ST/SP	Start/Stop pin
10	CW/CCW	CW/CCW pin
11	PWM	PWM input pin
12	FG	FG (Composition of 1phase) pin
13	AL	Lock detection pin
14	LD	Lock protection pin
15	FG3	FG (Composition of 3phase) pin
16	LIMIT2	Current limit pin2
17	LIMIT	Current limit pin
18	W	Output W pin
19	V	Output V pin
20	U	Output U pin
21	CP1	Capacitor connection pin 1 for chage pump
22	CP2	Capacitor connection pin 2 for chage pump
23	VG	Capacitor connection pin for chage pump
24	VCC	Power supply pin

## Operation Notes

### (1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings, such as the applied voltage (VCC) or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.

### (2) Power Supply and Ground Wiring

The motor ground PGND pin is not connected to the IC GND pin. Separate the large-current PGND from the signal GND, and make one common ground point at a single reference point. These configurations will eliminate ground fluctuation between power sections and signal sections of the circuit. An overshooting, undershooting, or oscillation, on the power supply line, can occur due to instantaneous load fluctuations, which in turn, is due to a slow response of the power supply to instantaneous response. Fluctuating voltage on the power supply and ground lines may damage the device. Be sure to connect a bypass filter capacitor (1 $\mu$ F to 100 $\mu$ F) as close as possible to the IC between the power supply and ground pins. Check that the selected capacitance will not have an adverse influence on any characteristics, such as a drop in the electrolytic capacitor value that can occur at low temperatures. If it is necessary, add zener diode protection. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

### (3) Ground potential

Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

### (4) Thermal design

Use a proper thermal design that allows for a sufficient margin of the power dissipation (Pd) at actual operating conditions.

### (5) Pin short and wrong direction assembly of the device.

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if positive and ground power supply terminals are reversed. The IC may also be damaged if pins are shorted together or are shorted to other circuit's power lines.

### (6) Avoiding strong magnetic field

Malfunction may occur if the IC is used around a strong magnetic field.

### (7) ASO

Ensure that the output transistors of the motor driver are not driven under excess conditions of the absolute maximum ratings and ASO.

### (8) TSD (Thermal Shut Down) circuit

If the junction temperature (Tjmax) reaches 175°C (Typ.), the TSD circuit will operate, and the coil output circuit of the motor will open. There is a temperature hysteresis of approximately 25°C (Typ.). The TSD circuit is designed only to shut off the IC in order to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. The performance of the IC's characteristics is not guaranteed and it is recommended that the device is replaced after the TSD is activated.

### (9) PWM Drive

PWM drive occur the noise on the power supply. Be sure to connect a bypass capacitor as close as possible to the IC pin.

### (10) Testing an application board

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to, or removing it from a jig or fixture, during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting and storing the IC.

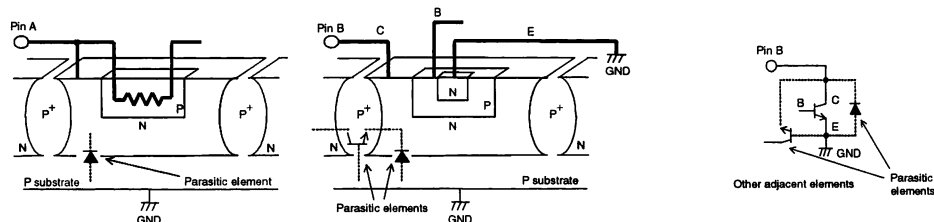
### (11) Regarding the input pin of the IC

This monolithic IC contains P<sup>+</sup> isolation and P substrate layers between adjacent elements to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic diode and transistor.

Parasitic elements can occur inevitably in the structure of the IC. The operation of parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic elements operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



Example of Simple IC Architecture

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