

# BLC6G22-75; BLC6G22LS-75

## Power LDMOS transistor

Rev. 01 — 7 February 2008

Objective data sheet

### 1. Product profile

#### 1.1 General description

75 W LDMOS power transistor for base station applications at frequencies from 2000 MHz to 2200 MHz.

**Table 1. Typical performance**

RF performance at  $T_{case} = 25^\circ\text{C}$  in a common source class-AB production test circuit.

Mode of operation	f (MHz)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	IMD3 (dBc)	ACPR (dBc)
2-carrier W-CDMA	2110 to 2170	28	17	18.5	31	-37 <sup>[1]</sup>	-41 <sup>[1]</sup>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7 dB at 0.01 % probability on CCDF per carrier; carrier spacing 10 MHz.

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

#### 1.2 Features

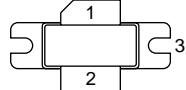
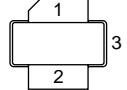
- Typical 2-carrier W-CDMA performance at frequencies of 2110 MHz and 2170 MHz, a supply voltage of 28 V and an  $I_{Dq}$  of 690 mA:
  - ◆ Average output power = 17 W
  - ◆ Gain = 18.5 dB
  - ◆ Efficiency = 31 %
  - ◆ IMD3 = -37 dBc
  - ◆ ACPR = -41 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2000 MHz to 2200 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for W-CDMA base stations and multicarrier applications in the 2000 MHz to 2200 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
<b>BLC6G22-75 (SOT895A)</b>			
1	drain		
2	gate		
3	source	[1]	  sym112
<b>BLC6G22LS-75 (SOT896B)</b>			
1	drain		
2	gate		
3	source	[1]	  sym112

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description	Version	
BLC6G22-75	-	plastic flanged cavity package; 2 mounting slots; 2 leads	SOT895A	
BLC6G22LS-75	-	plastic earless flanged cavity package; 2 leads	SOT896B	

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$I_D$	drain current		-	18	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Type	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80^\circ\text{C}$ ; $P_L = 17 \text{ W}$	BLC6G22-75	0.9	K/W
			BLC6G22LS-75	0.75	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}$ ; $I_D = 0.5 \text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10 \text{ V}$ ; $I_D = 100 \text{ mA}$	1.40	2	2.40	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 28 \text{ V}$ ; $I_D = 690 \text{ mA}$	1.60	2.2	2.60	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 28 \text{ V}$	-	-	3	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V}$ ; $V_{DS} = 10 \text{ V}$	14.9	18.5	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11 \text{ V}$ ; $V_{DS} = 0 \text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}$ ; $I_D = 5 \text{ A}$	-	7.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V}$ ; $I_D = 3.5 \text{ A}$	-	0.15	-	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0 \text{ V}$ ; $V_{DS} = 28 \text{ V}$ ; $f = 1 \text{ MHz}$	-	1.4	-	pF

## 7. Application information

**Table 7. Application information**

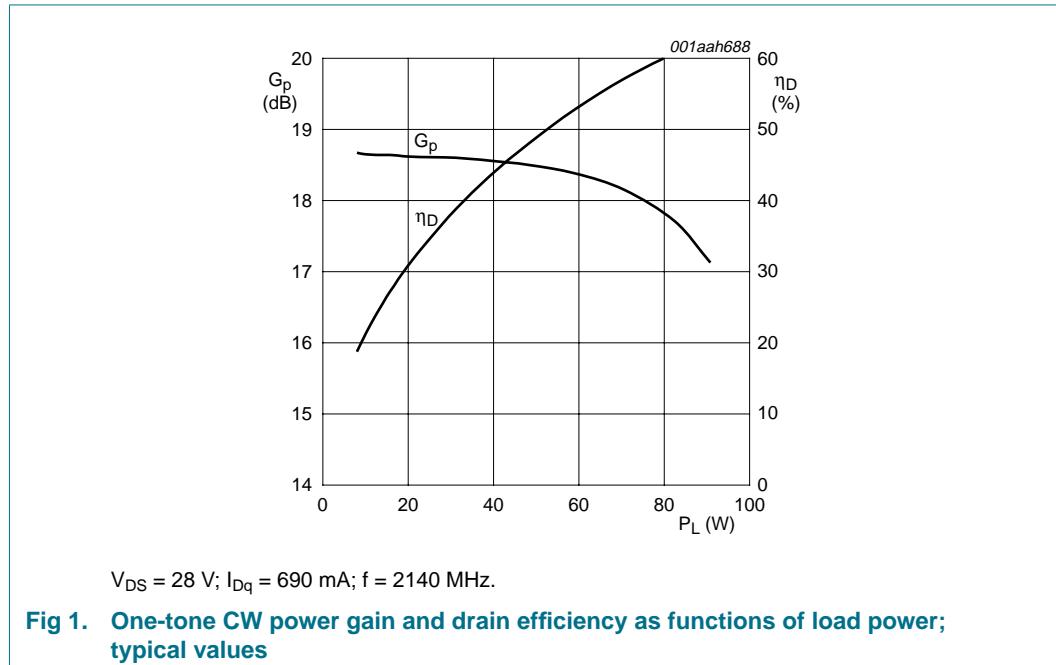
Mode of operation: 2-carrier W-CDMA; PAR 7 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 PDPCH;  $f_1 = 2112.5 \text{ MHz}$ ;  $f_2 = 2122.5 \text{ MHz}$ ;  $f_3 = 2157.5 \text{ MHz}$ ;  $f_4 = 2167.5 \text{ MHz}$ ; RF performance at  $V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 690 \text{ mA}$ ;  $T_{case} = 25^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	17	-	W
$G_p$	power gain	$P_{L(AV)} = 17 \text{ W}$	17.3	18.5	-	dB
IRL	input return loss	$P_{L(AV)} = 17 \text{ W}$	-	-9.2	-6.5	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 17 \text{ W}$	28	31	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)} = 17 \text{ W}$	-	-37	-34	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)} = 17 \text{ W}$	-	-41	-38.5	dBc

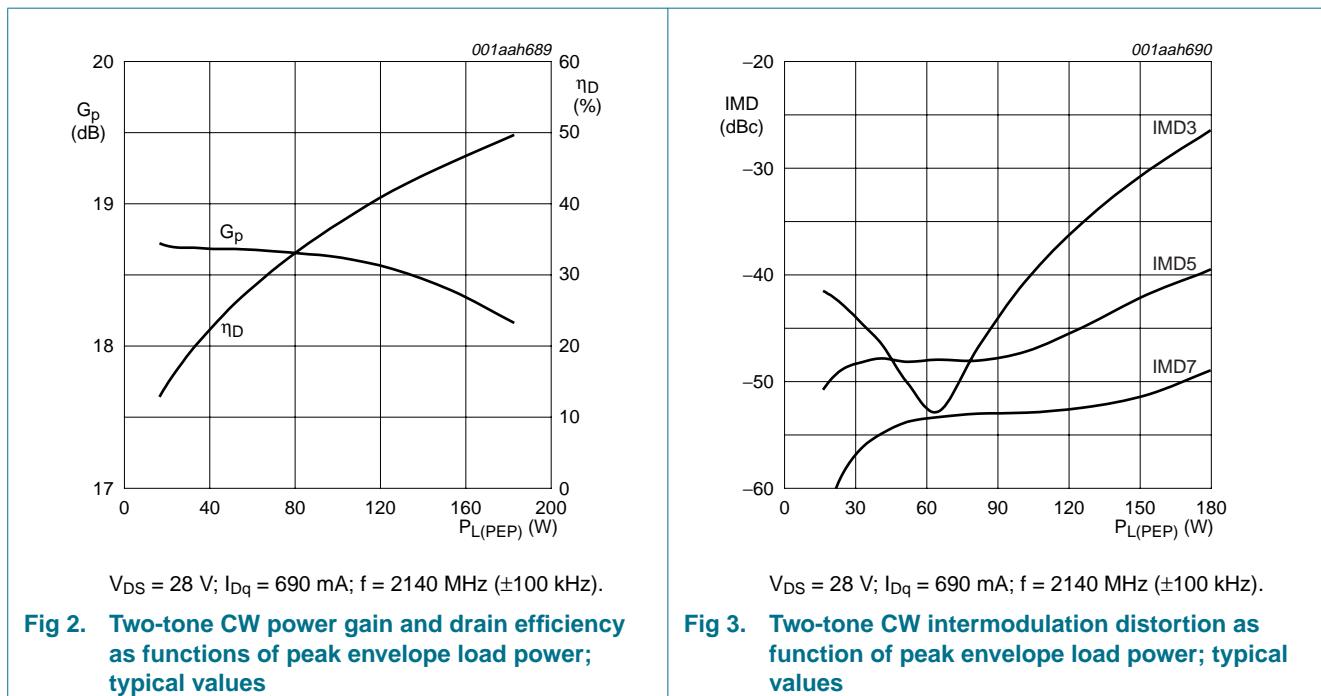
### 7.1 Ruggedness in class-AB operation

The BLC6G22-75 and BLC6G22LS-75 are capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28 \text{ V}$ ;  $I_{Dq} = 690 \text{ mA}$ ;  $P_L = 75 \text{ W}$  (CW);  $f = 2170 \text{ MHz}$ .

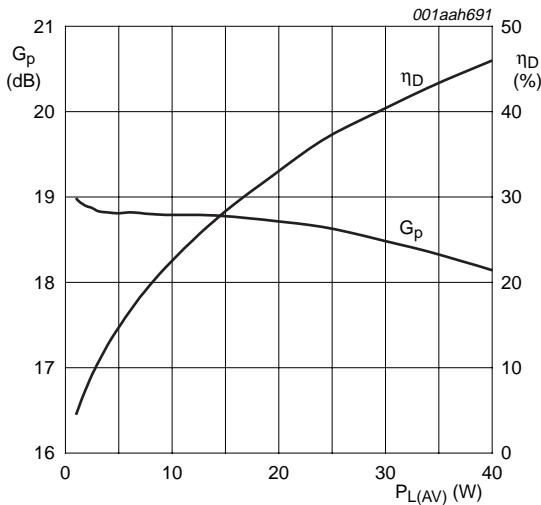
## 7.2 One-tone CW



## 7.3 Two-tone CW

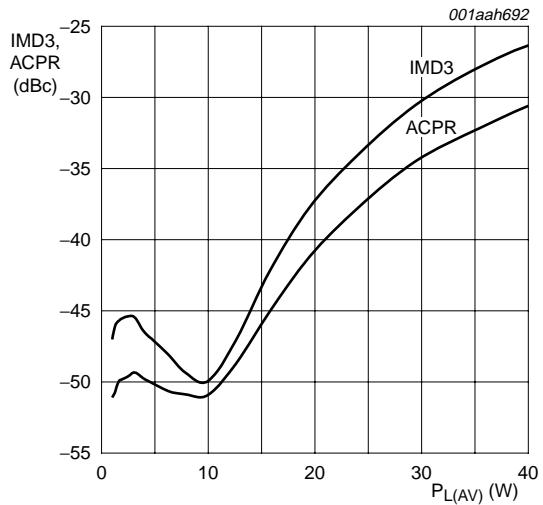


#### 7.4 2-carrier W-CDMA



$V_{DS} = 28$  V;  $I_{Dq} = 950$  mA;  $f = 2140$  MHz ( $\pm 5$  MHz); carrier spacing 10 MHz.

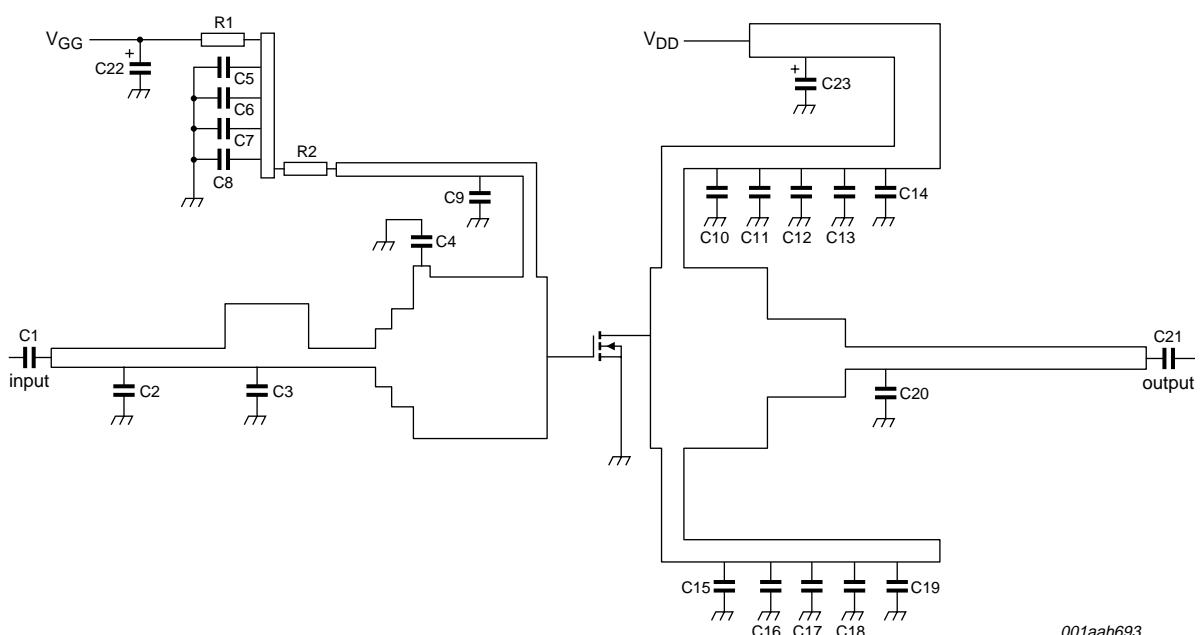
**Fig 4. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values**



$V_{DS} = 28$  V;  $I_{Dq} = 690$  mA;  $f = 2140$  MHz ( $\pm 5$  MHz); carrier spacing 10 MHz.

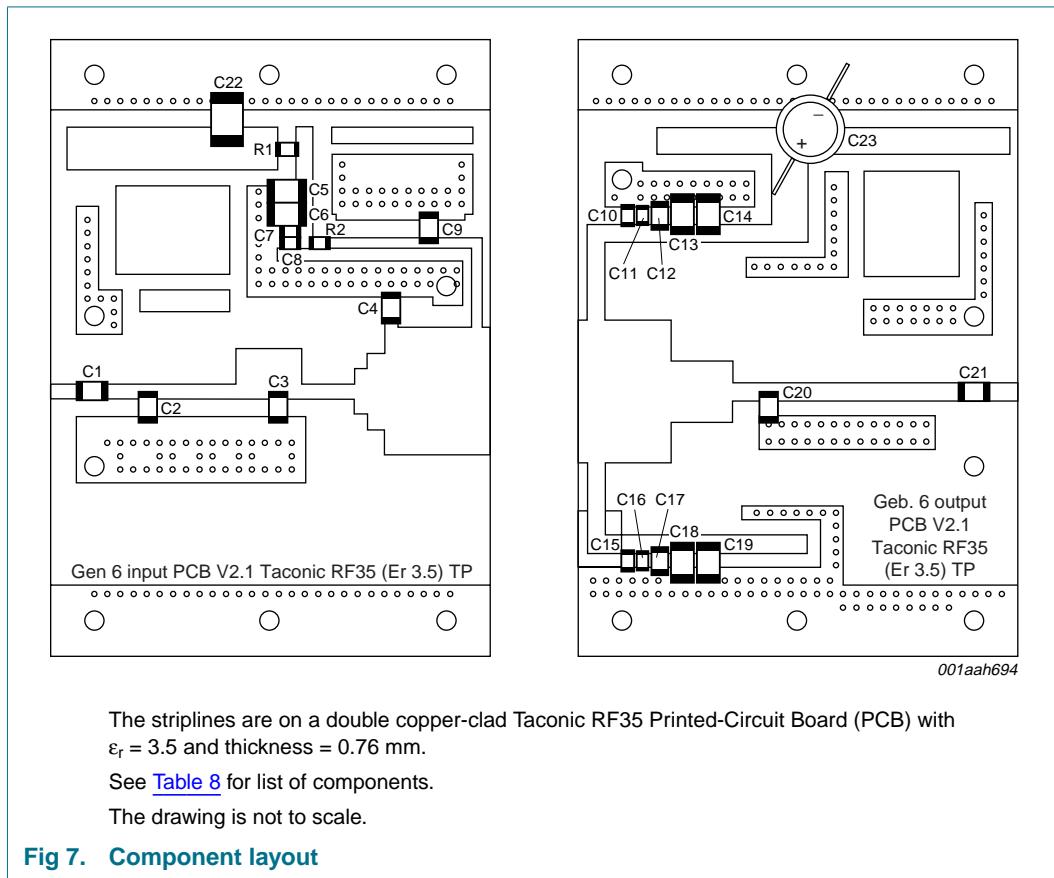
**Fig 5. 2-carrier W-CDMA adjacent channel power ratio and third order intermodulation distortion as functions of average load power; typical values**

### 8. Test information



The drawing is not to scale.

**Fig 6. Test circuit for operation at 800 MHz**

**Table 8. List of components (see [Figure 6](#) and [Figure 7](#))**

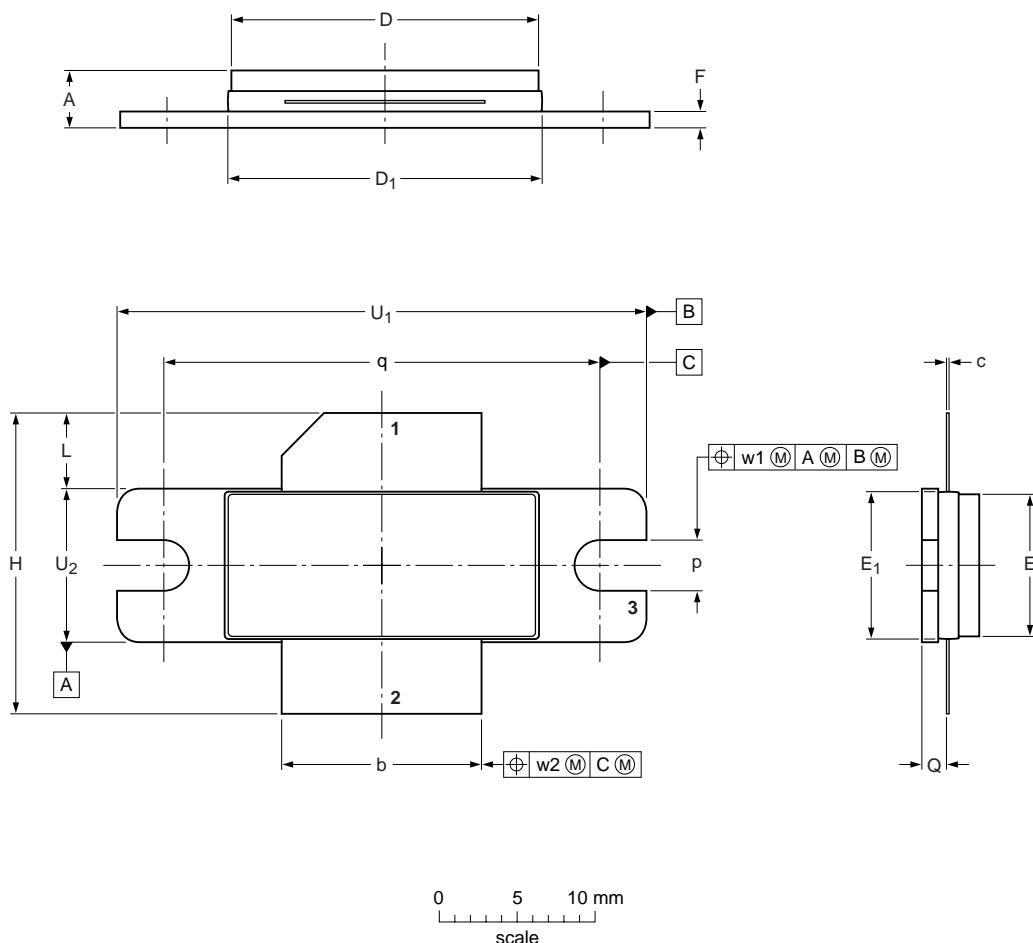
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	5.6 pF	<a href="#">[1]</a>
C2, C3	multilayer ceramic chip capacitor	0.5 pF	<a href="#">[1]</a>
C4	multilayer ceramic chip capacitor	0.6 pF	<a href="#">[1]</a>
C5, C6, C13, C14, C18, C19	multilayer ceramic chip capacitor	1.5 $\mu$ F	Murata 0603 or capacitor of same quality
C7, C8, C11, C16	multilayer ceramic chip capacitor	100 nF	
C9	multilayer ceramic chip capacitor	15 pF	<a href="#">[1]</a>
C10, C15	multilayer ceramic chip capacitor	220 nF	
C12, C17	multilayer ceramic chip capacitor	10 pF	<a href="#">[1]</a>
C20	multilayer ceramic chip capacitor	0.3 pF	<a href="#">[1]</a>
C21	multilayer ceramic chip capacitor	20 pF	<a href="#">[1]</a>
C22	tantalum capacitor	10 $\mu$ F; 35 V	
C23	electrolytic capacitor	220 $\mu$ F; 35 V	
R1	SMD resistor	3.6 $\Omega$	
R2	SMD resistor	5.1 $\Omega$	

[1] American Technical Ceramics type 100B or capacitor of same quality.

## 9. Package outline

Plastic flanged cavity package; 2 mounting slots; 2 leads

SOT895A



DIMENSIONS (mm are the original dimensions)

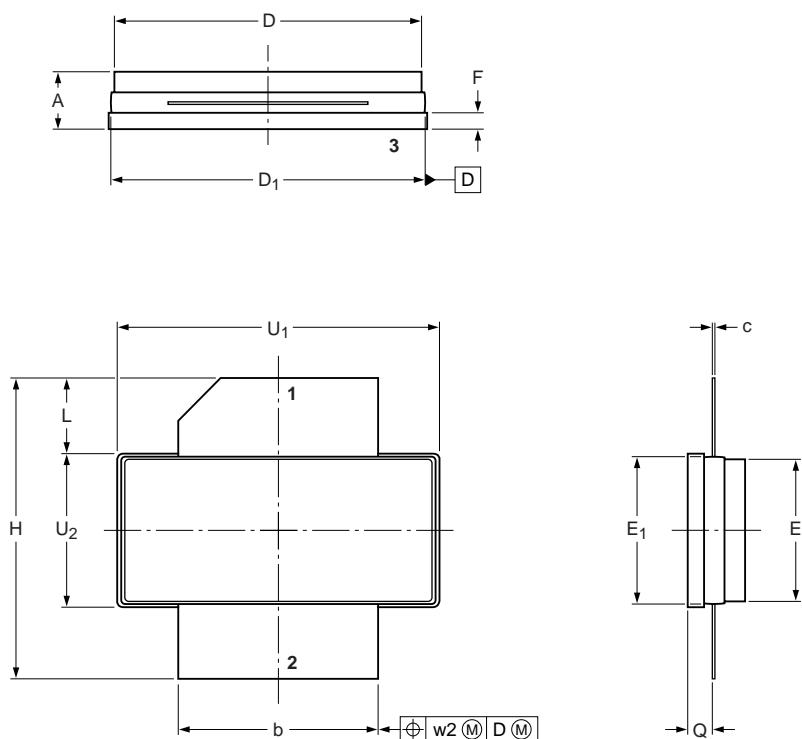
UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	w <sub>1</sub>	w <sub>2</sub>
mm	4.1 3.3	12.83 12.57	0.17 0.14	19.9 19.7	20.42 20.12	9.53 9.27	9.78 9.53	1.14 0.89	19.94 18.92	5.3 4.5	3.38 3.12	1.75 1.50	27.94 33.91	34.16 33.91	9.98 9.65	0.25 0.25	0.6
inches	0.161 0.130	0.505 0.495	0.0065 0.0055	0.785 0.775	0.804 0.792	0.375 0.365	0.385 0.375	0.045 0.035	0.785 0.745	0.209 0.177	0.133 0.123	0.069 0.059	1.100 1.335	1.345 1.335	0.392 0.380	0.01 0.023	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT895A						06-02-21 06-04-03

Fig 8. Package outline SOT895A

Plastic earless flanged cavity package; 2 leads

SOT896B



## DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	Q	U <sub>1</sub>	U <sub>2</sub>	w <sub>2</sub>
mm	4.1 3.3	12.83 12.57	0.17 0.14	19.9 19.7	20.42 20.12	9.53 9.27	9.78 9.53	1.14 0.89	19.94 18.92	5.3 4.5	1.75 1.50	20.70 20.45	9.98 9.65	0.6
inches	0.161 0.130	0.505 0.495	0.0065 0.0055	0.785 0.775	0.804 0.792	0.375 0.365	0.385 0.375	0.045 0.035	0.785 0.745	0.209 0.177	0.069 0.059	0.815 0.805	0.392 0.380	0.023

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT896B						06-02-21 06-04-03

Fig 9. Package outline SOT896B

## 10. Abbreviations

**Table 9. Abbreviations**

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCCH	Dedicated Physical CHannel
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 10. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC6G22-75_BLC6G22LS-75_1	20080207	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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