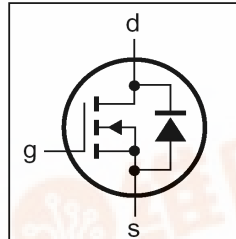




BLV830

N-channel Enhancement Mode Power MOSFET

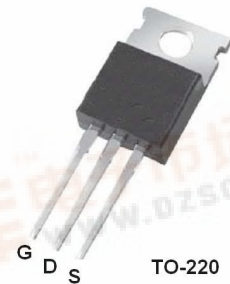
- Avalanche Energy Specified
- Fast Switching
- Simple Drive Requirements



BV_{DSS}	500V
$R_{DS(ON)}$	1.5Ω
I_D	4.5A

Description

This advanced high voltage MOSFET is produced using Belling's proprietary DMOS technology. Designed for high efficiency switch mode power supply.



Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Continuous Drain Current	4.5	A
	Continuous Drain Current ($T_C=100^{\circ}C$)	2.85	A
I_{DM}	Drain Current (pulsed) (Note 1)	18	A
P_D	Power Dissipation	75	W
	Linear Derating Factor	0.59	W/°C
E_{AS}	Single Pulsed Avalanche Energy (Note2)	250	mJ
I_{AR}	Avalanche Current	4.5	A
E_{AR}	Repetitive Avalanche Energy	7.5	mJ
T_j	Operating Junction Temperature Range	-55 to +150	°C
T_{SDG}	Storage Temperature Range	-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{th(j-c)}$	Thermal Resistance, Junction to case Max.	1.67	°C/W
$R_{th(j-a)}$	Thermal Resistance, Junction to Ambient Max.	62.5	°C/W



Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.6	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=2.7A$	-	-	1.5	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance(note3)	$V_{DS}=50V, I_D=2.7A$	2.5	-	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=500V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current $T_c=125^\circ\text{C}$	$V_{DS}=400V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = \pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge	$V_{DD}=400V$ $I_D=4.5A$	-	-	38	nC
Q_{gs}	Gate-Source Charge	$V_{GS}=10V$	-	-	5	nC
Q_{gd}	Gate-Drain Charge	note3	-	-	22	nC
$t_{(on)}$	Turn-on Delay Time	$V_{DD}=250V$ $I_D=4.5A$ $R_G=25\Omega$ note3	-	8.2	-	ns
t_r	Turn-on Rise Time		-	46	-	ns
$t_{(off)}$	Turn-off Delay Time		-	90	-	ns
t_f	Turn-off Fall Time		-	45	-	ns
C_{iss}	Input Capacitance	$V_{DS}=25V$ $V_{GS}=0V$ $f = 1\text{MHz}$	-	800	-	pF
C_{oss}	Output Capacitance		-	100	-	pF
C_{rss}	Reverse Transfer Capacitance		-	50	-	pF

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_S	Continuous Source Diode Forward Current		-	-	4.5	A
I_{SM}	Pulsed Source Diode Forward Current (note1)		-	-	18	A
V_{SD}	Forward On Voltage	$V_{GS}=0V, I_S=4.5A$	-	-	1.6	V
t_{rr}	Reverse Recovery Time	$V_{GS}=0V, I_S=4.5A$	-	320	-	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	1	-	μC

Note:

- (1) Repetitive Rating: Pulse width limited by maximum junction temperature
- (2) $L=25\text{mH}$, $I_{as}=4.5A$, $V_{dd}=50V$, $R_g=25\Omega$, starting $T_j=25^\circ\text{C}$
- (3) Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$

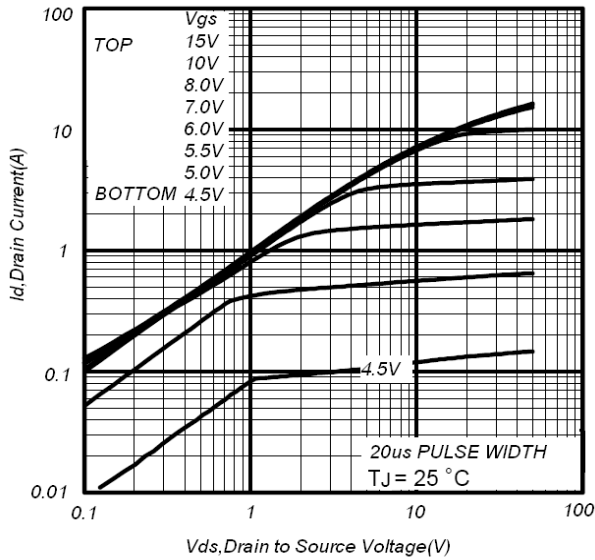
Typical Characteristics


Fig 1. Typical Output Characteristics

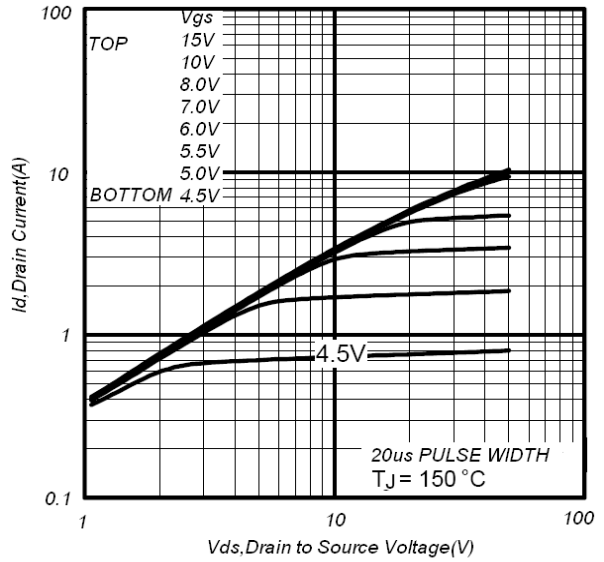


Fig 2. Typical Output Characteristics

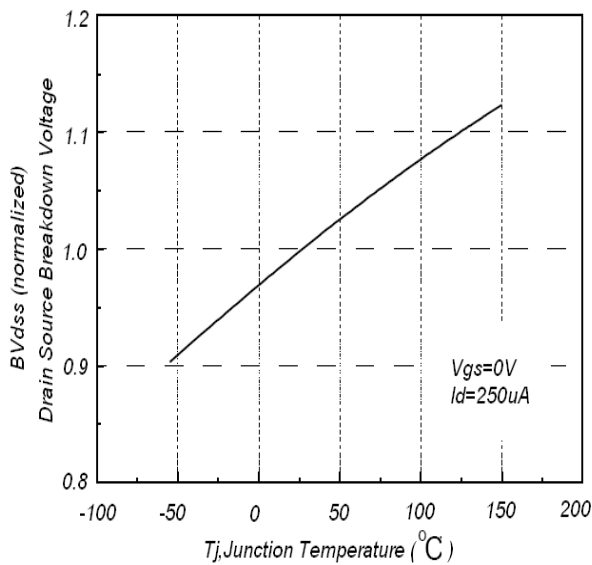
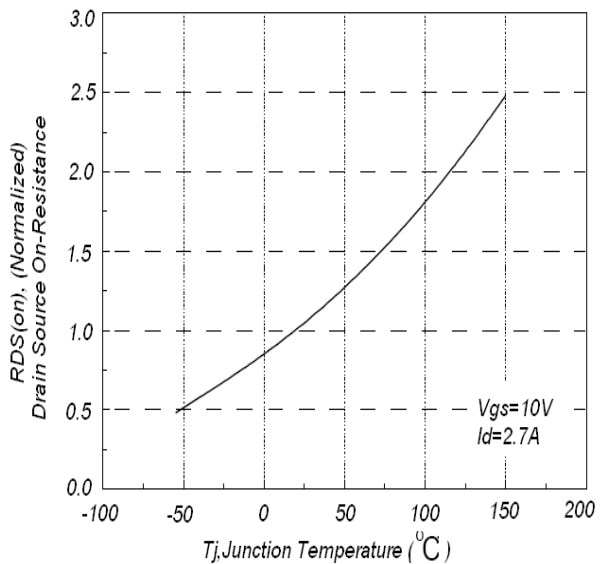

 Fig 3. Normalized BV_{dss} vs. Junction Temperature


Fig 4. Normalized On-Resistance vs. Junction Temperature

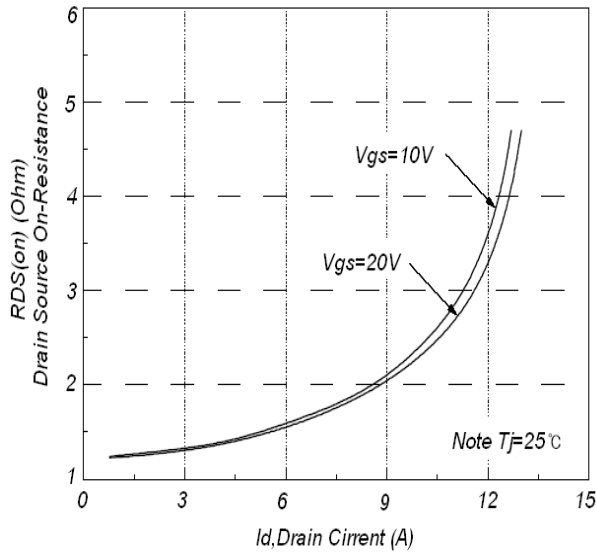
Typical Characteristics (continued)


Fig 5. On-Resistance Variation vs. Drain Current and Gate Voltage

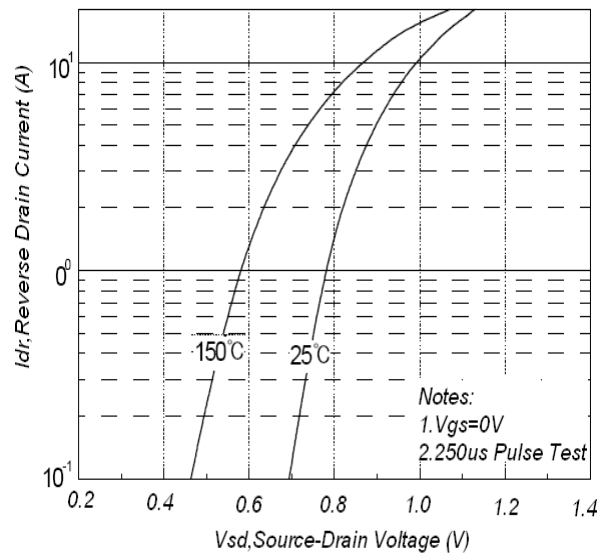


Fig 6. Body Diode Forward Voltage Variation vs. Source Current and Temperature

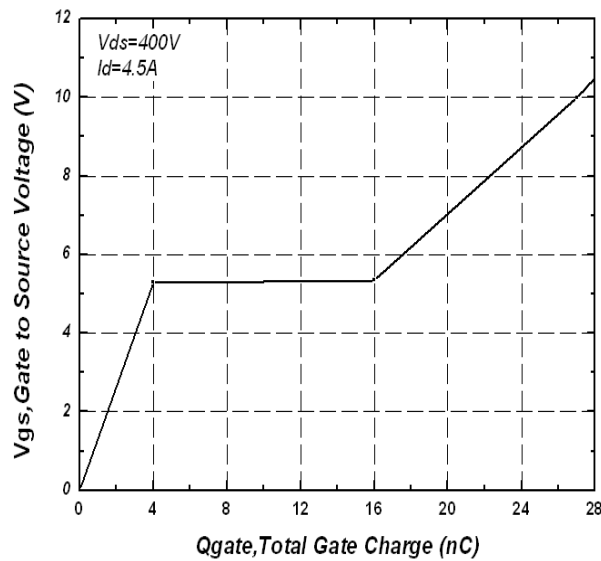


Fig 7. Gate Charge Characteristics

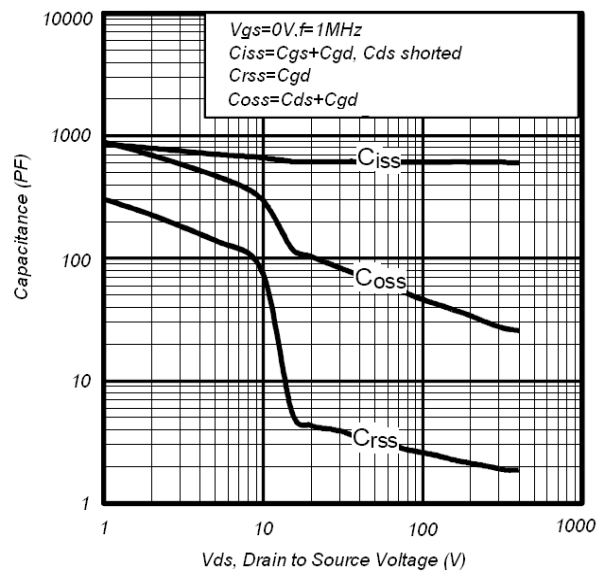


Fig 8. Capacitance Characteristics

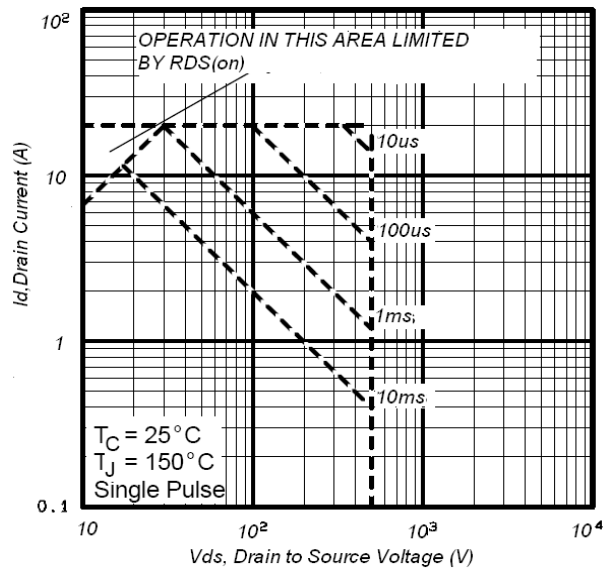
Typical Characteristics (continued)


Fig 9. Maximum Safe Operating Area

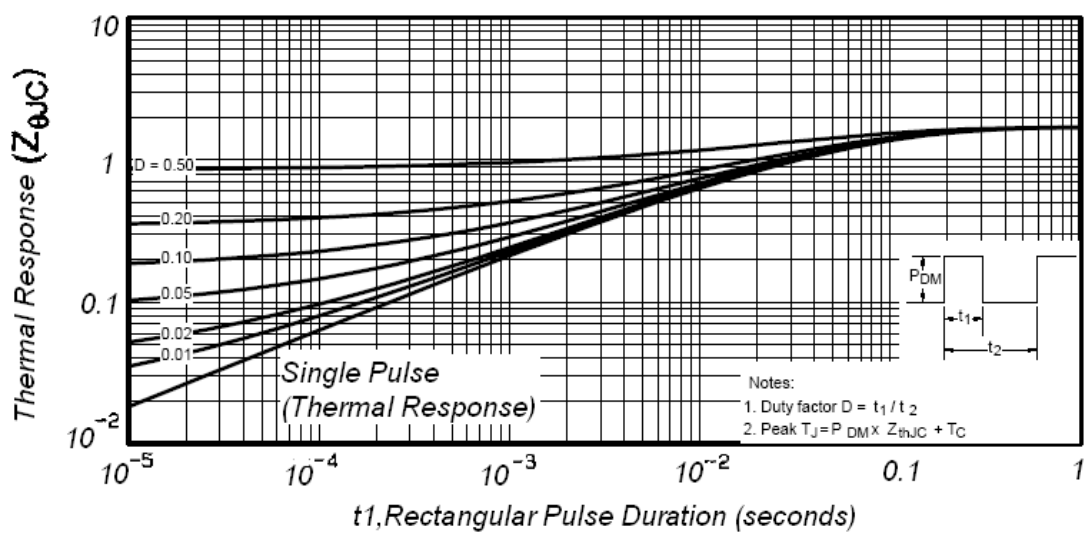


Fig 10. Transient Thermal Response Curve

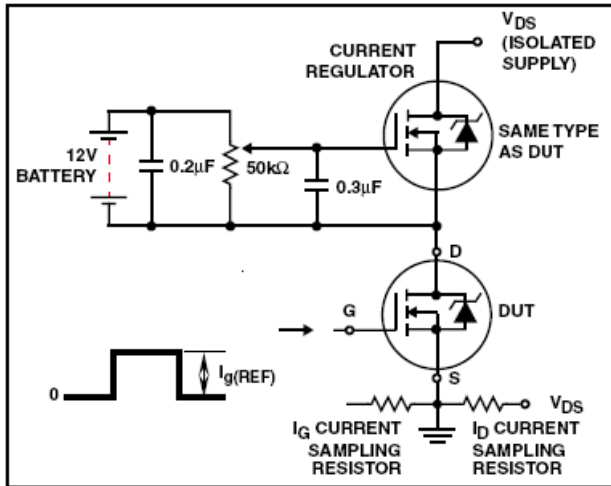
Test Circuit and Waveform


Fig 11. Gate Charge Circuit

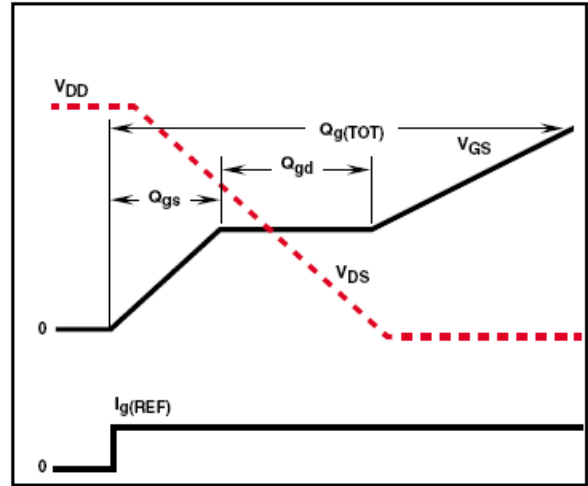


Fig 12. Gate Charge Waveform

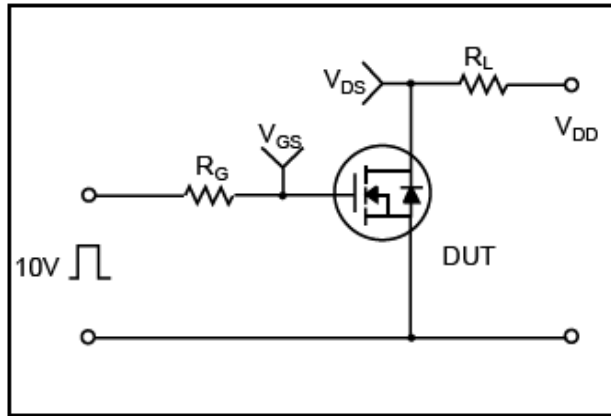


Fig 13. Switching Time Circuit

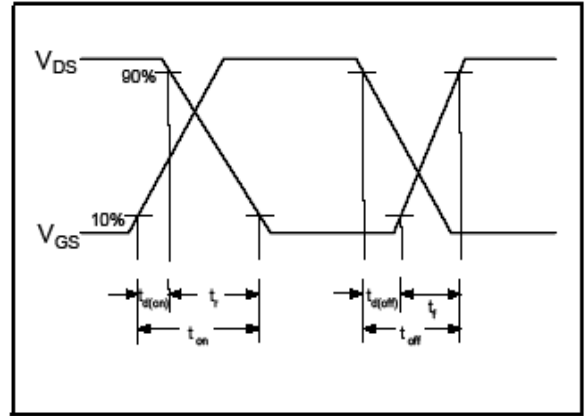


Fig 14. Switching Time Waveform

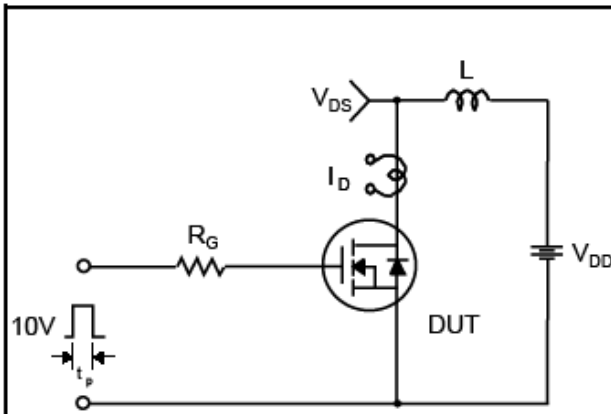


Fig 15. Unclamped Inductive Switching Test Circuit

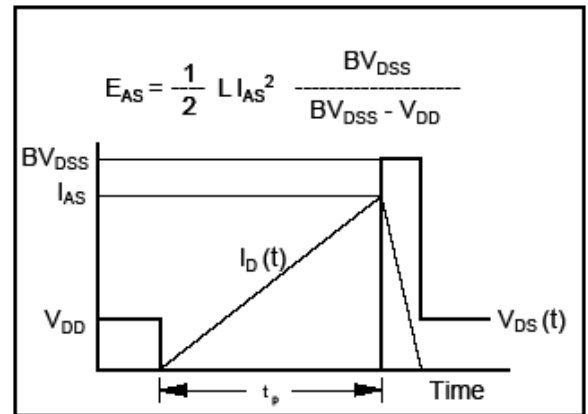


Fig 16. Unclamped Inductive Switching Waveforms