CY241V08A-01,04
CY241V8A-01

MPEG Clock Generator with VCXO

Features

- **Integrated phase-locked loop (PLL)**
- **Low-jitter, high-accuracy outputs**
- **VCXO with analog adjust**
- **3.3V operation**
- **Compatible with MK3727 (–1, –4)**
- **Application compatibility for a wide variety of designs**
- **Enables design compatibility**
- **Lower drive strength settings (CY241V08A–04)**

Benefits

- Digital VCXO control
- Second source for existing designs
- Highest-performance PLL tailored for multimedia applications
- Meets critical timing requirements in complex system designs
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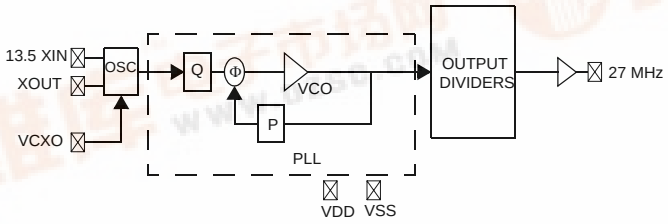
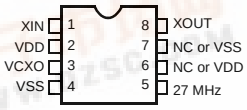
CY241V08A-01,-04 Logic Block Diagram



Pin Configurations

CY241V08A-01,-04
8-pin SOIC



Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Control Curve	Other Features
CY241V08A-01	1	13.5-MHz pullable crystal input per Cypress specification	1 copy of 27 MHz	linear	Compatible with MK3727
CY241V08A-04	1	13.5-MHz pullable crystal input per Cypress specification	1 copy of 27 MHz	linear	Same as CY241V08A-01 except lower drive strength settings

Pin Description

Name	Pin Number	Description
XIN	1	**Reference crystal input**
VDD	2	**Voltage supply**
VCXO	3	**Input analog control for VCXO**
VSS	4	**Ground**
27 MHz	5	**27-MHz clock output**
NC/VDD	6	**No connect or voltage supply**
NC/VSS	7	**No connect or ground**
XOUT	8	**Reference crystal output**

Absolute Maximum Conditions

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage (V_{DD}) .....–0.5 to +7.0V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5

Storage Temperature (Non-condensing) .... –55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention @ Tj = 125°C .....> 10 years

Package Power Dissipation ..... 350 mW

ESD (Human Body Model) MIL-STD-883 ..... > 2000V

Pullable Crystal Specifications[1]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	–	13.5	–	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal drive level	No external series resistor assumed	150	–	–	μW
F_{3SEPHI}	Third overtone separation from $3*F_{NOM}$	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from $3*F_{NOM}$	Low side	–	–	–150	ppm
C_0	Crystal shunt capacitance		–	–	7	pF
C_0/C_1	Ratio of shunt to motional capacitance		180	–	250	–
C_1	Crystal motional capacitance		14.4	18	21.6	fF

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
VDD	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
t_{PU}	Power-up time for all VDD pins to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

DC Electrical Specifications

Parameter	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output HIGH Current	$V_{OH} = V_{DD} – 0.5V$, $V_{DD} = 3.3V$	12	24	–	mA
I_{OL}	Output LOW Current	$V_{OL} = 0.5V$, $V_{DD} = 3.3V$	12	24	–	mA
C_{IN}	Input Capacitance	Except XIN, XOUT pins	–	–	7	pF
V_{VCXO}	VCXO Input Range		0	–	V_{DD}	V
$f_{\Delta XO}$[2]	VCXO Pullability Range	Low Side	–	–	–115	ppm
		High Side	115	–	–	ppm
I_{VDD}	Supply Current		–	30	35	mA

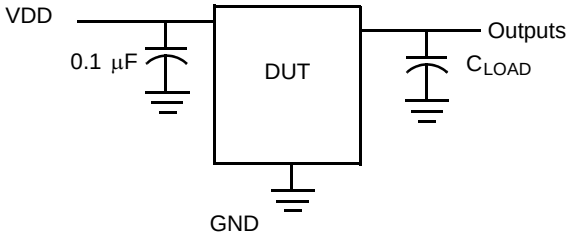
Notes:

1. Crystals that meet this specification includes: Ecliptek ECX-5788-13.500M,Siward XTL001050A-13.5-14-400, Raltron A-13.500-14-CL,PDI HA13500XFSA14XC.
2. –115/+115 ppm assumes 2.5pF of additional board level load capacitance. This range will be shifted down with more board capacitance or shifted up with less board capacitance.

AC Electrical Specifications (V_{DD} = 3.3V) [3]

Parameter[3]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
ER_{OR}	Rising Edge Rate –01	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, CLOAD = 15 pF See *Figure 2*.	0.8	1.4	–	V/ns
ER_{OF}	Falling Edge Rate –01	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, CLOAD = 15 pF See *Figure 2*.	0.8	1.4	–	V/ns
ER_{OR}	Rising Edge Rate –04	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, CLOAD = 15 pF See *Figure 2*.	0.7	1.1	–	V/ns
ER_{OF}	Falling Edge Rate –04	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, CLOAD = 15 pF See *Figure 2*.	0.7	1.1	–	V/ns
t_9	Clock Jitter	Peak-to-peak period jitter	–	–	100	ps
t_{10}	PLL Lock Time		–	–	3	ms

Test and Measurement Set-up



Voltage and Timing Definitions

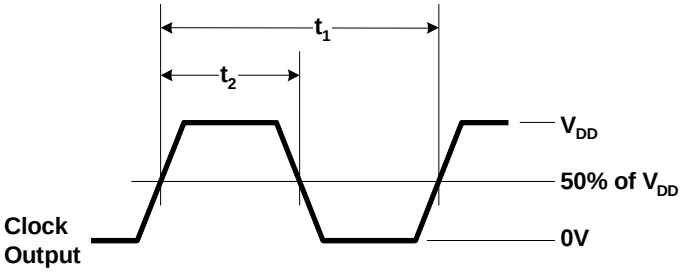


Figure 1. Duty Cycle Definition

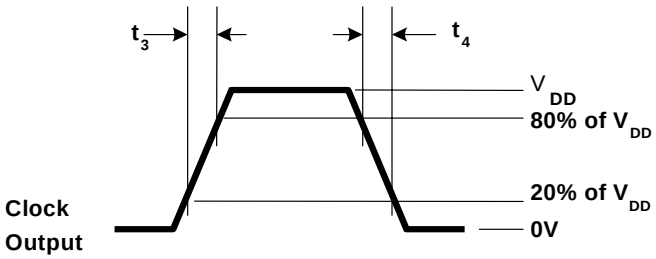


Figure 2. ER = (0.6 x V_{DD})/t_3, EF = (0.6 x V_{DD})/t_4

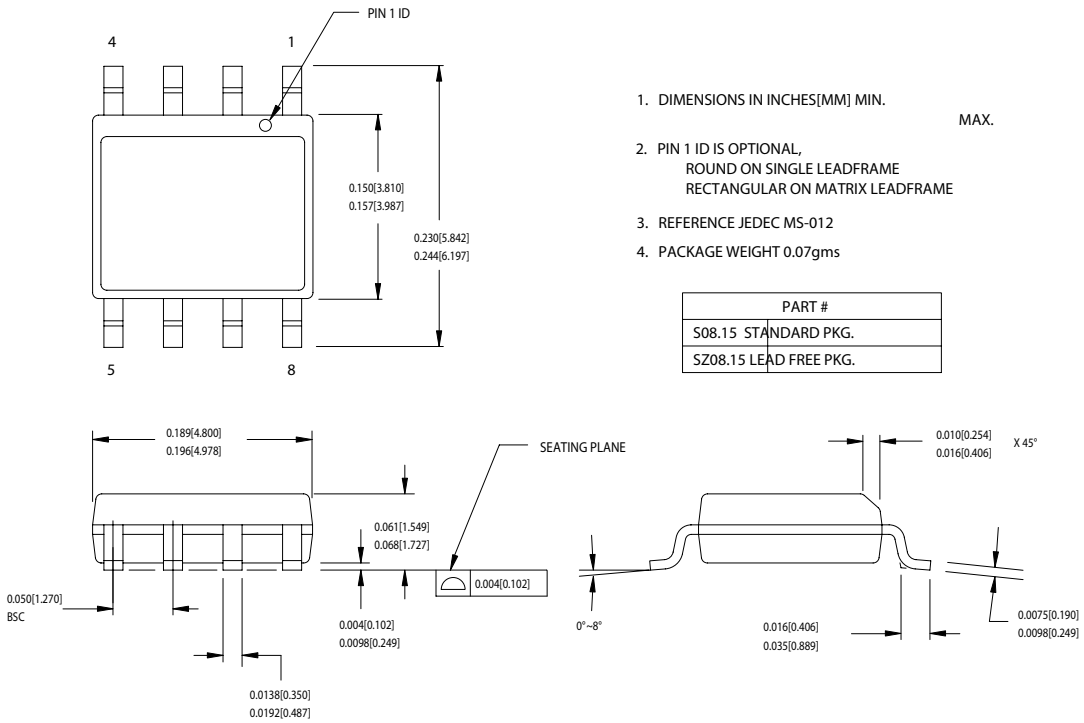
Note:
3. Not 100% tested.

Ordering Information

Ordering Code	Package Type	Operating Range	Operating Voltage	Features
CY241V08ASC–01	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY241V08ASC–01T	8-pin SOIC – Tape and Reel	Commercial	3.3V	Linear VCXO control curve
CY241V08ASC–04	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY241V08ASC–04T	8-pin SOIC – Tape and Reel	Commercial	3.3V	Linear VCXO control curve
Lead-free				
CY241V8ASXC-01	8-pin SOIC	Commercial	3.3V	Linear VCXO control curve
CY241V8ASXC-01T	8-pin SOIC - Tape and Reel	Commercial	3.3V	Linear VCXO control curve

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8



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Document History Page

Document Title: CY241V08A-01,04/ CY241V8A-01MPEG Clock Generator with VCXO Document Number: 38-07656				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	214069	See ECN	RGL	New Data Sheet
*A	220404	See ECN	RGL	Minor Change: To post on web
*B	393122	See ECN	RGL	Added Lead-free device for -01 Added the CY241V8A-01 in the title
*C	414184	See ECN	RGL	Minor Change: Deleted unneccesary text in the benefit section