16-BIT, 1.0 GSPS 2x-4x INTERPOLATING DIGITAL-TO-ANALOG CONVERTER (DAC)

FEATURES

- 16-Bit Digital-to-Analog Converter (DAC)
- 1.0 GSPS Update Rate
- 16-Bit, 1.0 GSPS Input LVDS Data Bus
  - 8 Sample Input FIFO
  - On-Chip Delay Lock Loop
- High Performance
  - 73 dBc ACLR WCDMA TM1 at 180 MHz
- 2x-32x Clock Multiplying PLL/VCO
- 2x or 4x Interpolation Filters
  - Stopband Transition 0.4–0.6 Fdata
  - Filters configurable in either Low-Pass or High-Pass mode–allows selection or higher order image
- On-Chip 1.2-V Reference
- Differential Scalable Output: 2 to 20 mA
- Package: 64-Pin 9 × 9 mm QFN

APPLICATIONS

- Cellular Base Stations
- Broadband Wireless Access (BWA)
- WiMAX 802.16
- Fixed Wireless Backhaul
- Cable Modem Termination System (CMTS)

DESCRIPTION

The DAC5681Z is a 16-bit 1.0 GSPS digital-to-analog converter (DAC) with wideband LVDS data input, integrated 2x/4x interpolation filters, on-board clock multiplier, and internal voltage reference. The DAC5681Z offers superior linearity and noise performance.

The DAC5681Z integrates a wideband LVDS port with on-chip termination, providing full 1.0 GSPS data transfer into the DAC, or half-rate data and 1/4-rate input data can be interpolated by on-board 2x or 4x FIR filters. Each interpolation FIR is configurable in either Low-Pass or High-Pass mode, allowing selection of a higher order output sectral image. An on-chip delay lock loop (DLL) simplifies LVDS interfacing by providing skew control for the LVDS input data clock.

The current-steering architecture of the DAC5681Z consists of a segmented array of current sinking switches directing up to 20mA of full-scale current to complementary output nodes. An accurate on-chip voltage reference is temperature-compensated and delivers a stable 1.2-V reference voltage. Optionally, an external reference may be used.

The DAC5681Z is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin QFN package. The device is pin upgradeable to the dual-channel DAC5682Z as well as the single-channel, non-interpolating DAC5681.

PRODUCT PREVIEW

ORDERING INFORMATION

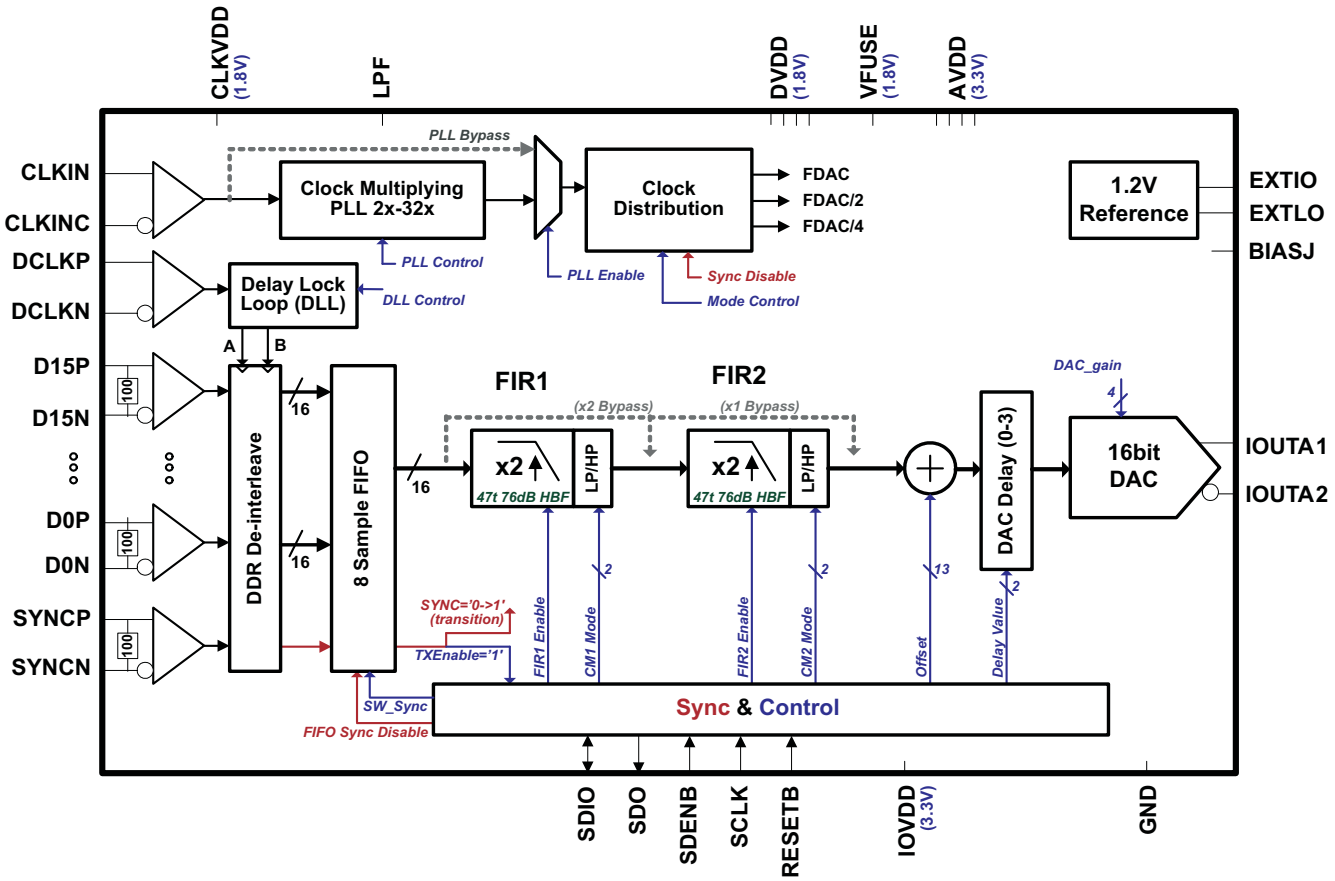
T_A	ORDER CODE	PACKAGE DRAWING/TYPE (1) (2) (3)	TRANSPORT MEDIA	QUANTITY
–40°C to 85°C	DAC5681ZIRGCT	RGC / 64QFN Quad Flatpack No-Lead	Small Tape and Reel	250
	DAC5681ZIRGCR		Large Tape and Reel	2000

(1) Thermal Pad Size: 7,4 mm × 7,4 mm
(2) MSL Peak Temperature: Level-3-260C-168 HR
(3) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

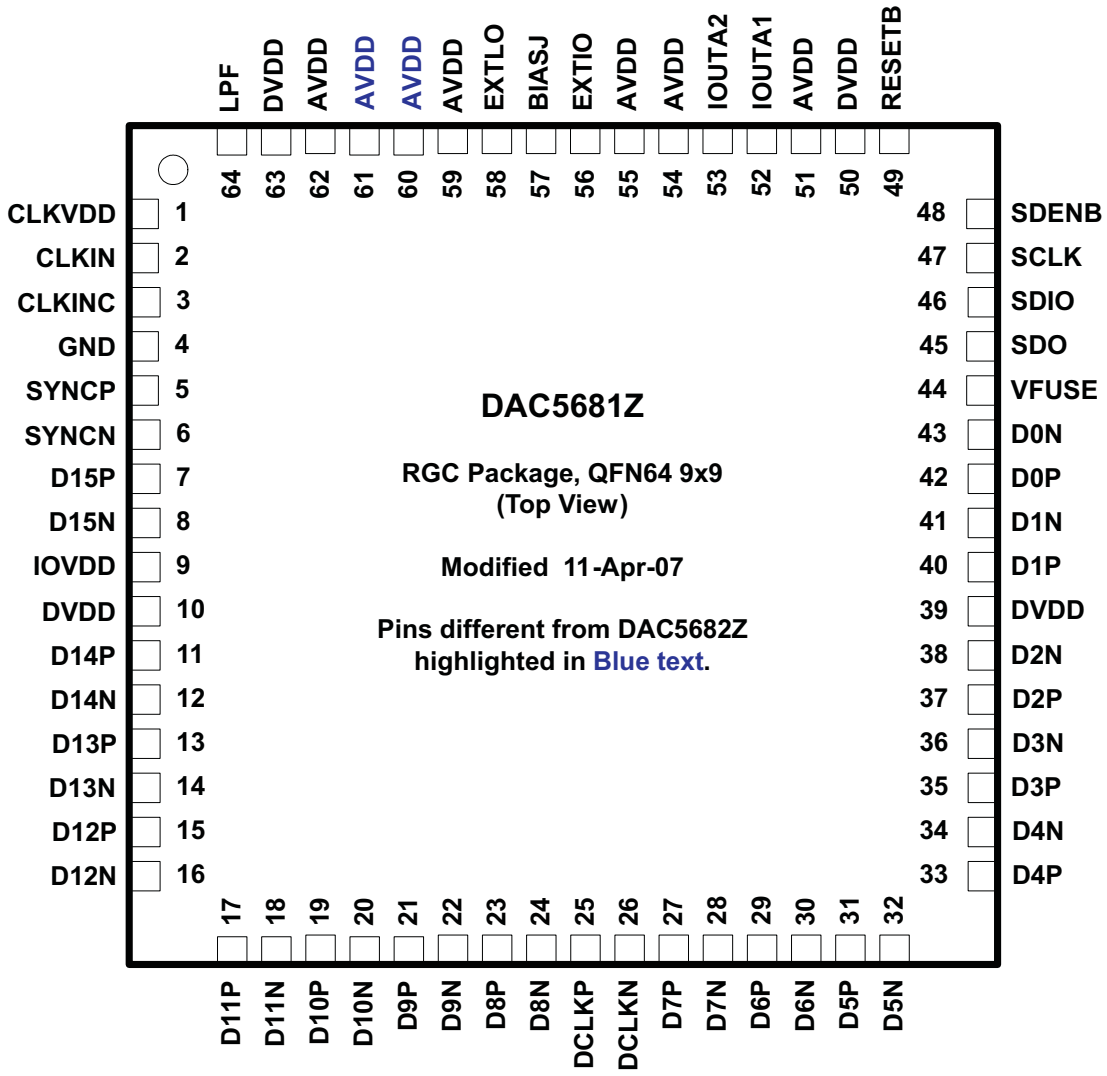
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

DAC5681Z
RGC PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AVDD	51, 54, 55, 59, 62	I	Analog supply voltage. (3.3V)
BIASJ	57	O	Full-scale output current bias
CLKIN	2	I	Positive external clock input. With the clock multiplier PLL enabled, CLKIN provides lower frequency reference clock. If the PLL is disabled, CLKIN directly provides clock for DAC up to 1GHz.
CLKINC	3	I	Complementary external clock input.
CLKVDD	1	I	Internal clock buffer supply voltage. (1.8 V)
D[15..0]P	7, 11, 13, 15, 17, 19, 21, 23, 27, 29, 31, 33, 35, 37, 40, 42	I	LVDS positive input data bits 0 through 15. Each positive/negative LVDS pair has an internal 100 Ω termination resistor. Order of bus can be reversed via **rev_bus** bit in CONFIG5 register. Data format relative to DCLKP/N clock is Double Data Rate (DDR) with two data samples input be DLCKP/N clock cycle. In dual-channel mode, data for the A-channel is input while DCLKP is high. D15P is most significant data bit (MSB) – pin 7 D0P is least significant data bit (LSB) – pin 42

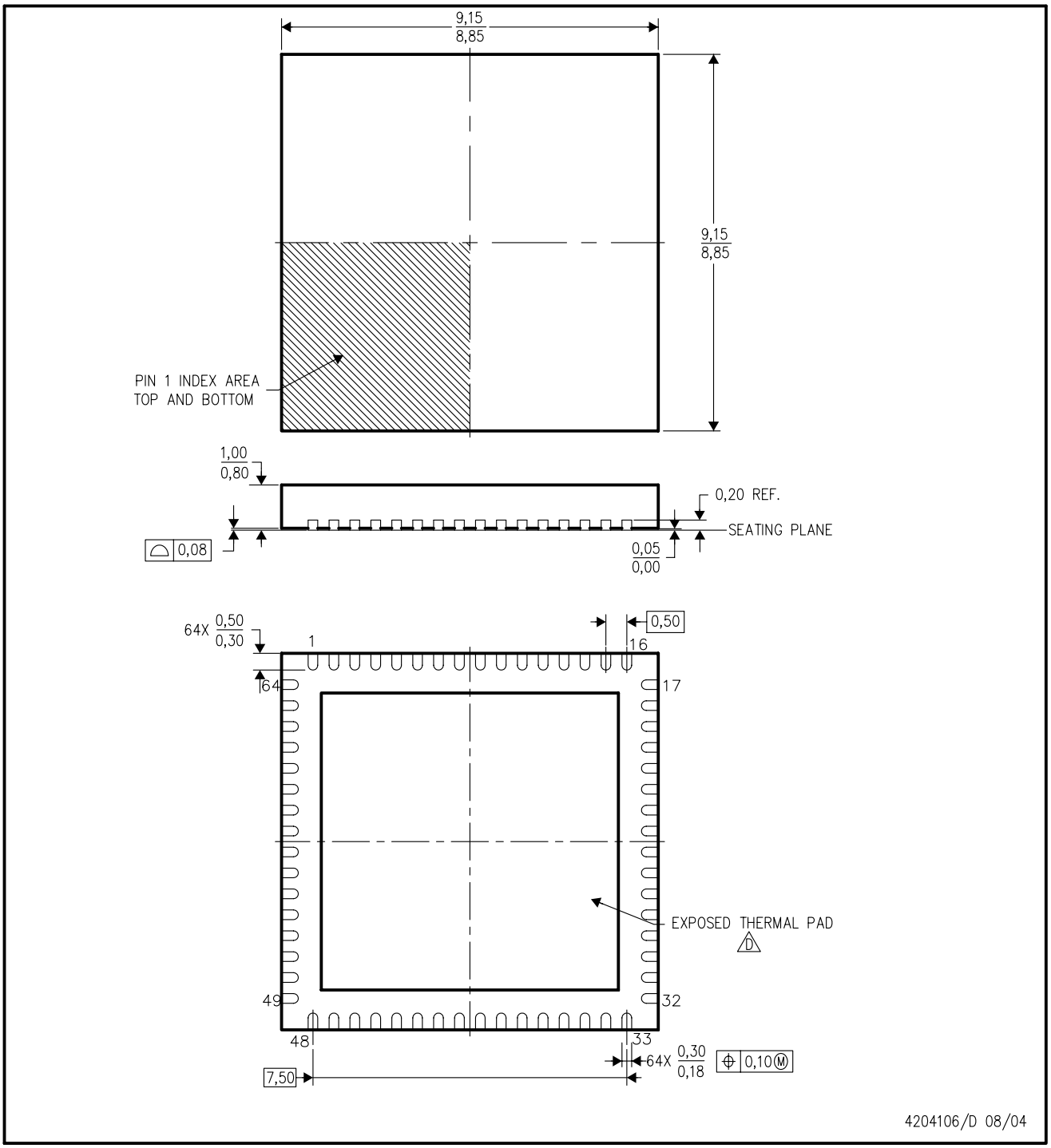
TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D[15..0]N	8, 12, 14, 16, 18, 20, 22, 24, 28, 30, 32, 34, 36, 38, 41, 43	I	LVDS negative input data bits 0 through 15. (See D[15:0]P description above) D15N is most significant data bit (MSB) – pin 8 D0N is least significant data bit (LSB) – pin 43
DCLKP	25	I	LVDS positive input clock. Unlike the other LVDS inputs, the DCLKP/N pair is self-biased and does **not** have an internal termination resistor in order to optimize operation of the DLL circuit. See the "DLL Operation" section. For proper external termination, connect a 100 Ω resistor across LVDS clock source lines followed by series 0.01 µF capacitors connected to each of DCLKP and DCLKN pins (see Figure 2). For best performance, the resistor and capacitors should be placed as close as possible to these pins.
DCLKN	26	I	LVDS negative input clock. (See the DCLKP description)
DVDD	10, 39, 50, 63	I	Digital supply voltage. (1.8 V)
EXTIO	56	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as internal reference output when EXTLO = GND, requires a 0.1 µF decoupling capacitor to AGND when used as reference output.
EXTLO	58	O	Internal reference ground. Connect to AVDD to disable the internal reference.
GND	4, Thermal Pad	I	Pin 4 and the Thermal Pad located on the bottom of the QFN package is ground for AVDD, DVDD and IOVDD supplies.
IOUTA1	52	O	A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin. In single DAC mode, outputs appear on the IOUTA1/A2 pair only.
IOUTA2	53	O	A-Channel DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0mA sink and the most positive voltage on the IOUTA2 pin.
IOUTB1	61	O	B-Channel DAC current output. See the IOUTA1 description above.
IOUTB2	60	O	B-Channel DAC complementary current output. See the IOUTA2 description above.
IOVDD	9	I	Digital I/O supply voltage (3.3V) for pins RESETB, SCLK, SDENB, SDIO, SDO.
LPF	64	I	PLL loop filter connection. If not using the clock multiplying PLL, the LPF pin may be left open. Set both **PLL_bypass** and **PLL_sleep** control bits for reduced power dissipation.
RESETB	49	I	Resets the chip when low. Internal pull-up.
SCLK	47	I	Serial interface clock. Internal pull-down.
SDENB	48	I	Active low serial data enable, always an input to the DAC5681Z. Internal pull-up.
SDIO	46	I/O	Serial interface data, bi-directional. Default setting sets SDIO as an input. Internal pull-down.
SDO	45	O	Serial interface data, uni-directional data output, if SDIO is an input. SDO is 3-stated when the 3 pin interface mode is selected (register 0x08 bit 1). Internal pull-down.
SYNCP	5	I	LVDS SYNC positive input data. The SYNCP/N LVDS pair has an internal 100 Ω termination resistor. By default, the **SYNCP/N input must be logic '1' to enable a DAC analog output**. See the *LVDS SYNCP/N Operation* paragraph for a detailed description.
SYNCN	6	I	LVDS SYNC negative input data.
VFUSE	44	I	Digital supply voltage. (1.8V) **Connect to DVDD pins for normal operation**. This supply pin is also used for factory fuse programming.

DAC5682Z Data Sheet Reference

Prior to market release, please refer to the DAC5682Z (dual channel) data sheet SLLS853 for relevant single-channel functional descriptions and performance characteristics on the DAC5681Z device.

RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

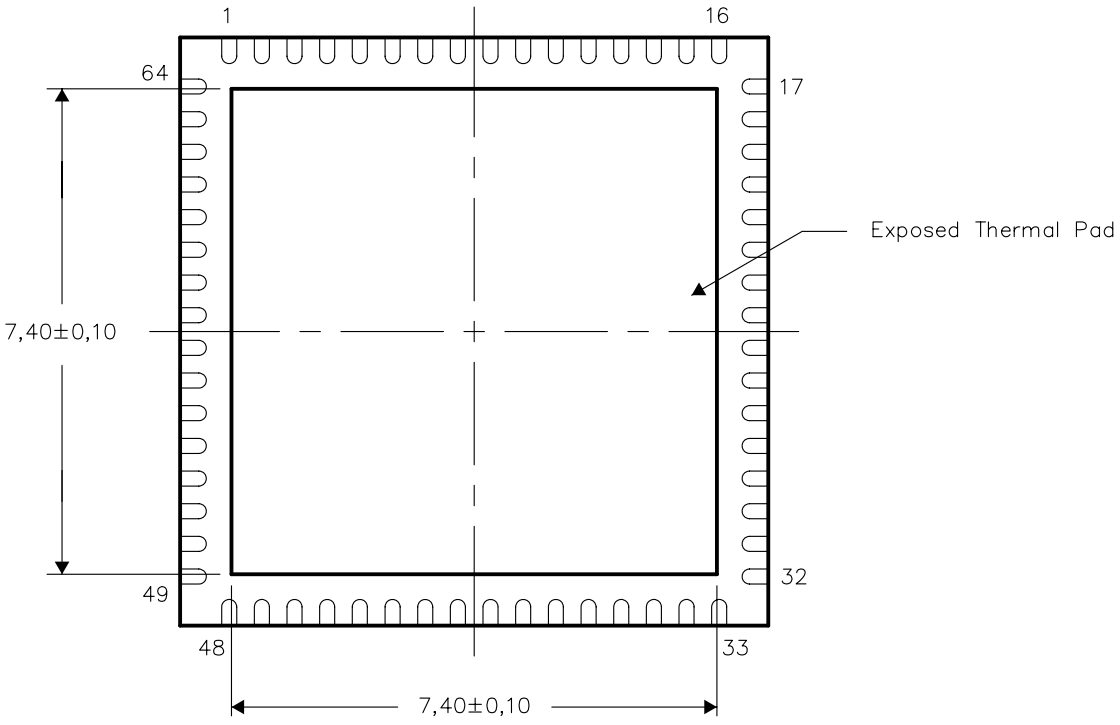
RGC (S–PQFP–N64)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

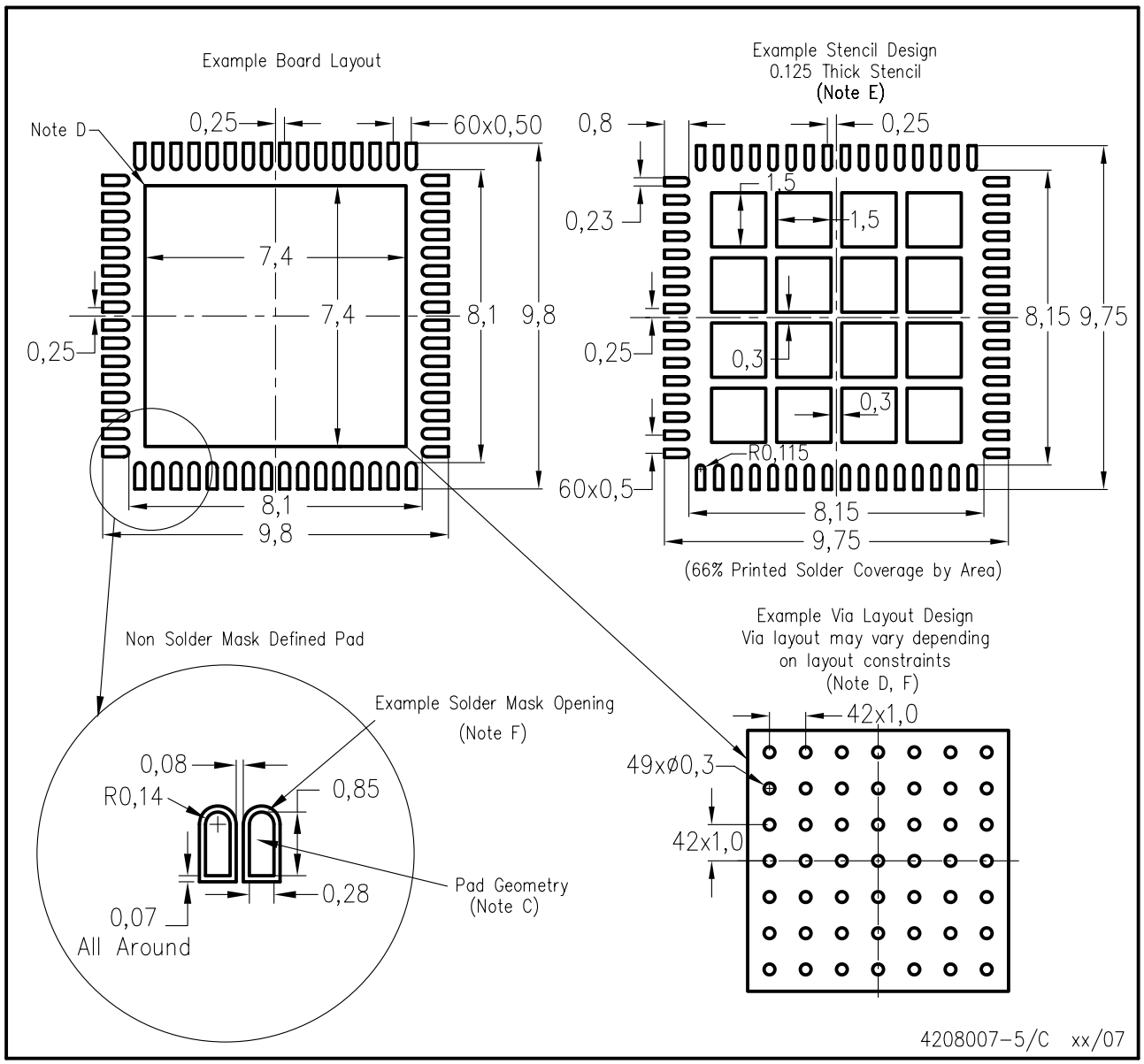


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGC (S–PQFP–N64)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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