



# DDC (XXXX) U

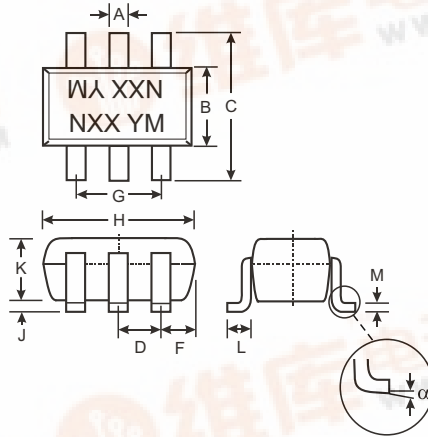
## NPN PRE-BIASED SMALL SIGNAL SOT-363 DUAL SURFACE MOUNT TRANSISTOR

### Features

- Epitaxial Planar Die Construction
- Complementary PNP Types Available (DDA)
- Built-In Biasing Resistors
- Also Available in Lead Free Version

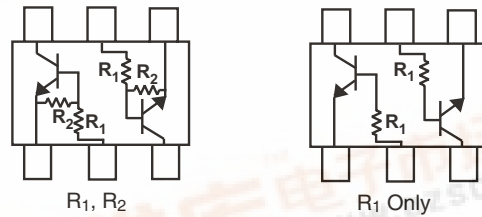
### Mechanical Data

- Case: SOT-363, Molded Plastic
- Moisture sensitivity: Level 1 per J-STD-020A
- Case material - UL Flammability Rating 94V-0
- Terminals: Solderable per MIL-STD-202, Method 208
- Also Available in Lead Free Plating (Matte Tin Finish). Please see Ordering Information, Note 4, on Page 3
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 3)
- Weight: 0.006 grams (approx.)
- Ordering Information (See Page 3)



SOT-363		
Dim	Min	Max
A	0.10	0.30
B	1.15	1.35
C	2.00	2.20
D	0.65 Nominal	
F	0.30	0.40
H	1.80	2.20
J	—	0.10
K	0.90	1.00
L	0.25	0.40
M	0.10	0.25
$\alpha$	0°	8°
All Dimensions in mm		

P/N	R1	R2	MARKING
DDC124EU	22K $\Omega$	22K $\Omega$	N17
DDC144EU	47K $\Omega$	47K $\Omega$	N20
DDC114YU	10K $\Omega$	47K $\Omega$	N14
DDC123JU	2.2K $\Omega$	47K $\Omega$	N06
DDC114EU	10K $\Omega$	10K $\Omega$	N13
DDC143TU	4.7K $\Omega$	-	N07
DDC114TU	10K $\Omega$	-	N12



SCHEMATIC DIAGRAM

### Maximum Ratings @ T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Supply Voltage, (3) to (1)	V <sub>CC</sub>	50	V
Input Voltage, (2) to (1)	V <sub>IN</sub>	-10 to +40 -10 to +40 -6 to +40 -5 to +12 -10 to +40 -5 V <sub>max</sub> -5 V <sub>max</sub>	V
Output Current	I <sub>O</sub>	30 30 70 100 50 100 100	mA
Output Current	I <sub>C</sub> (Max)	100	mA
Power Dissipation (Total)	P <sub>d</sub>	200	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R <sub>θJA</sub>	625	°C/W
Operating and Storage and Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.  
2. 150mW per element must not be exceeded.



**Electrical Characteristics** @  $T_A = 25^\circ\text{C}$  unless otherwise specified

Characteristic (DDC143TU & DDC114TU only)	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	$BV_{CBO}$	50	—	—	V	$I_C = 50\mu\text{A}$
Collector-Emitter Breakdown Voltage	$BV_{CEO}$	50	—	—	V	$I_C = 1\text{mA}$
Emitter-Base Breakdown Voltage	$BV_{EBO}$	5	—	—	V	$I_E = 50\mu\text{A}$
Collector Cutoff Current	$I_{CBO}$	—	—	0.5	$\mu\text{A}$	$V_{CB} = 50\text{V}$
Emitter Cutoff Current	$I_{EBO}$	—	—	0.5	$\mu\text{A}$	$V_{EB} = 4\text{V}$
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	—	—	0.3	V	$I_C/I_B = 2.5\text{mA} / 0.25\text{mA}$ DDC143TU $I_C/I_B = 1\text{mA} / 0.1\text{mA}$ DDC114TU
DC Current Transfer Ratio	$h_{FE}$	100	250	600	—	$I_C = 1\text{mA}, V_{CE} = 5\text{V}$
Input Resistor ( $R_1$ ) Tolerance	$\Delta R_1$	-30	—	+30	%	—
Gain-Bandwidth Product*	$f_T$	—	250	—	MHz	$V_{CE} = 10\text{V}, I_E = -5\text{mA}, f = 100\text{MHz}$

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Input Voltage	$V_{I(off)}$	0.5	1.1	—	V	$V_{CC} = 5\text{V}, I_O = 100\mu\text{A}$
		0.3	1.1	—		
	$V_{I(on)}$	—	1.9	3.0	V	$V_O = 0.3, I_O = 5\text{mA}$ $V_O = 0.3, I_O = 2\text{mA}$ $V_O = 0.3, I_O = 1\text{mA}$ $V_O = 0.3, I_O = 5\text{mA}$ $V_O = 0.3, I_O = 10\text{mA}$
		—	1.9	3.0		
Output Voltage	$V_{O(on)}$	—	0.1	0.3	V	$I_O/I_I = 10\text{mA} / 0.5\text{mA}$ $I_O/I_I = 10\text{mA} / 0.5\text{mA}$ $I_O/I_I = 5\text{mA} / 0.25\text{mA}$ $I_O/I_I = 5\text{mA} / 0.25\text{mA}$ $I_O/I_I = 10\text{mA} / 0.5\text{mA}$
		—	0.1	0.3		
Input Current	$I_I$	—	—	0.36 0.18 0.88 3.6 0.88	mA	$V_I = 5\text{V}$
Output Current	$I_{O(off)}$	—	—	0.5	$\mu\text{A}$	$V_{CC} = 50\text{V}, V_I = 0\text{V}$
DC Current Gain	$G_I$	56 68 68 80 30	—	—	—	$V_O = 5\text{V}, I_O = 5\text{mA}$ $V_O = 5\text{V}, I_O = 5\text{mA}$ $V_O = 5\text{V}, I_O = 10\text{mA}$ $V_O = 5\text{V}, I_O = 10\text{mA}$ $V_O = 5\text{V}, I_O = 5\text{mA}$
Input Resistor ( $R_1$ ) Tolerance	$\Delta R_1$	-30	—	+30	%	—
Resistance Ratio Tolerance	$R_2/R_1$	-20	—	+20	%	—
Gain-Bandwidth Product*	$f_T$	—	250	—	MHz	$V_{CE} = 10\text{V}, I_E = 5\text{mA}, f = 100\text{MHz}$

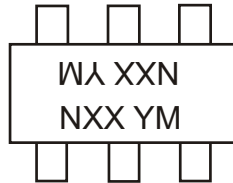
\* Transistor - For Reference Only

**Ordering Information** (Note 3)

Device	Packaging	Shipping
DDC124EU-7	SOT-363	3000/Tape & Reel
DDC144EU-7	SOT-363	3000/Tape & Reel
DDC114YU-7	SOT-363	3000/Tape & Reel
DDC123JU-7	SOT-363	3000/Tape & Reel
DDC114EU-7	SOT-363	3000/Tape & Reel
DDC143TU-7	SOT-363	3000/Tape & Reel
DDC114TU-7	SOT-363	3000/Tape & Reel

- Notes:
- For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.
  - For Lead Free version (with Lead Free terminal finish) part number, please add "-F" suffix to part number above.  
Example: DDC114TU-7-F.

**Marking Information**



NXX = Product Type Marking Code  
See Sheet 1 Diagrams  
YM = Date Code Marking  
Y = Year ex: N = 2002  
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**TYPICAL CURVES - DDC123JK  
ONE SECTION**

**NEW PRODUCT**

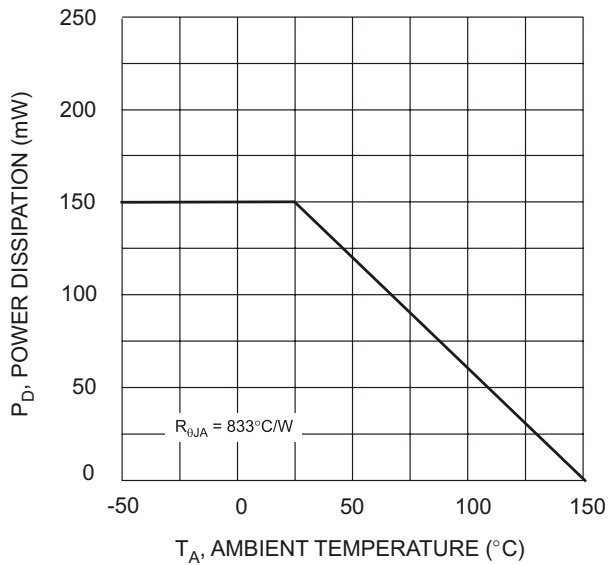


Fig. 1 Derating Curve

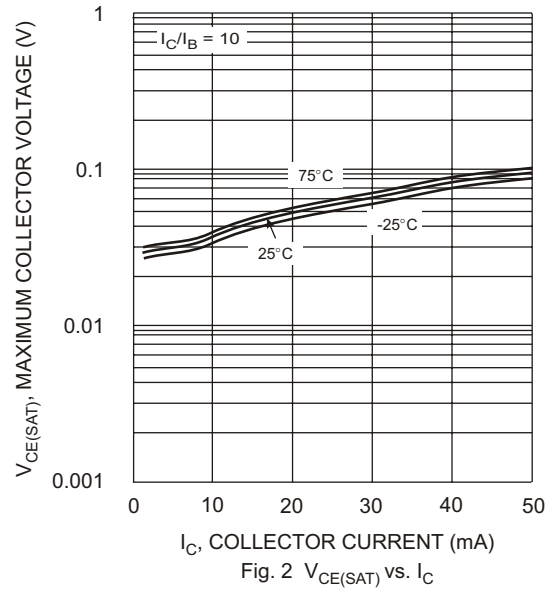


Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$

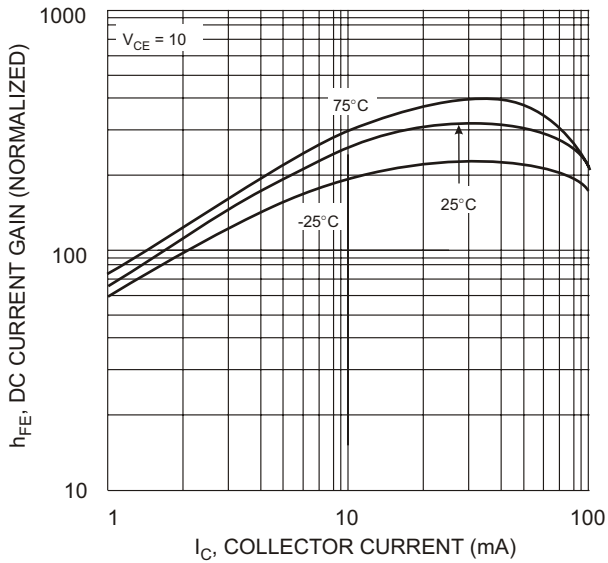


Fig. 3 DC Current Gain

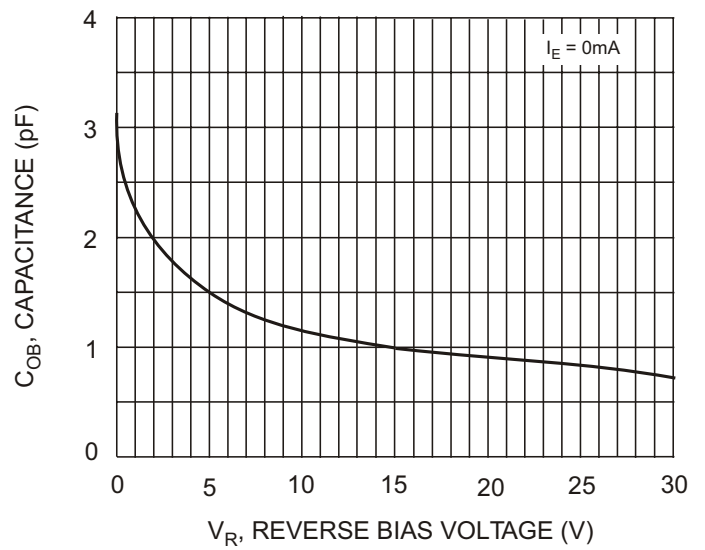


Fig. 4 Output Capacitance

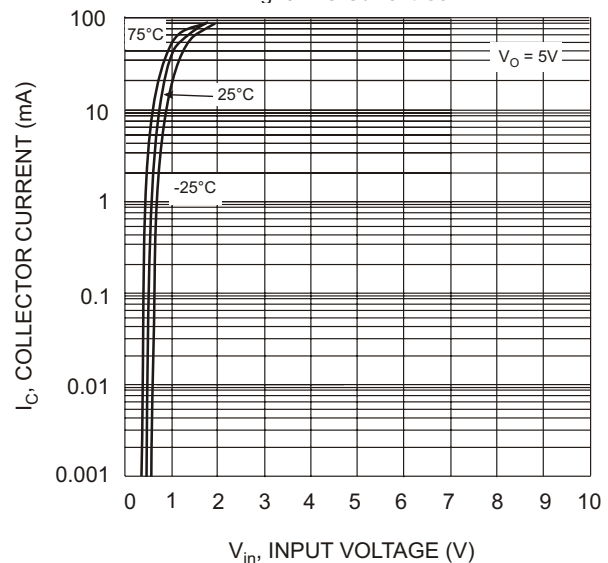


Fig. 5 Collector Current Vs. Input Voltage

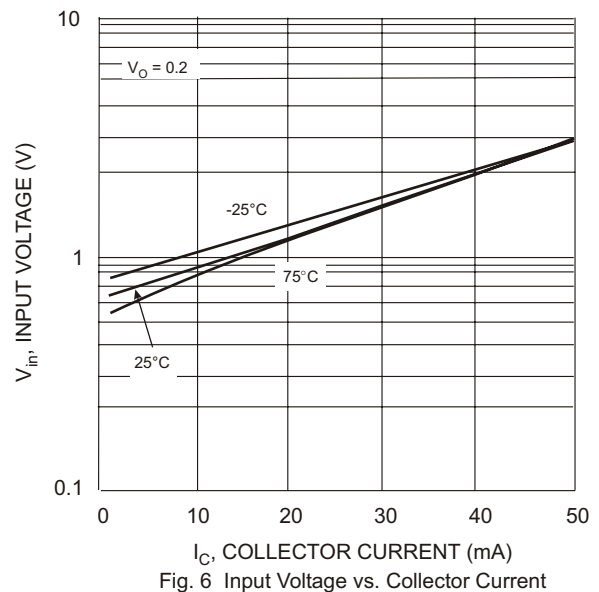


Fig. 6 Input Voltage vs. Collector Current

**TYPICAL CURVES - DDC114TK**

**ONE SECTION**

**NEW PRODUCT**

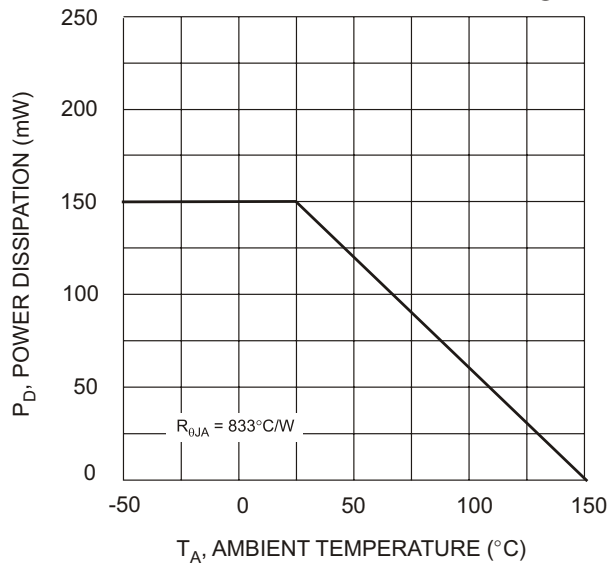


Fig. 1 Derating Curve

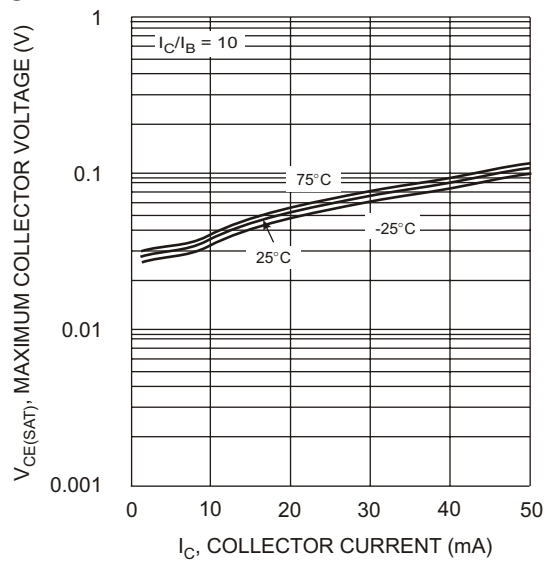


Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$

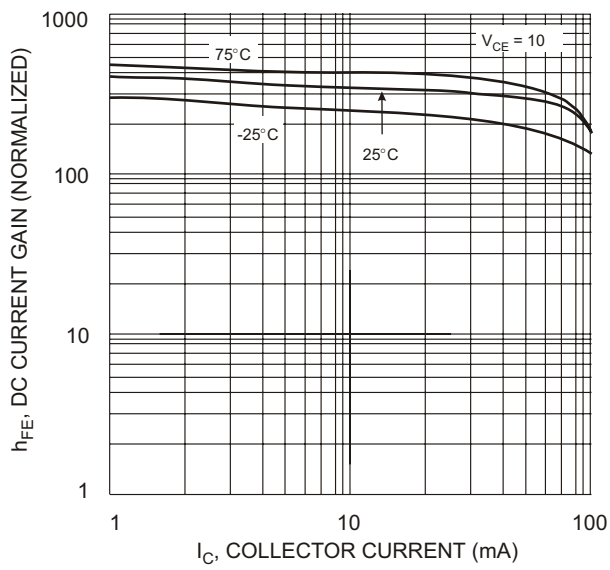


Fig. 3 DC Current Gain

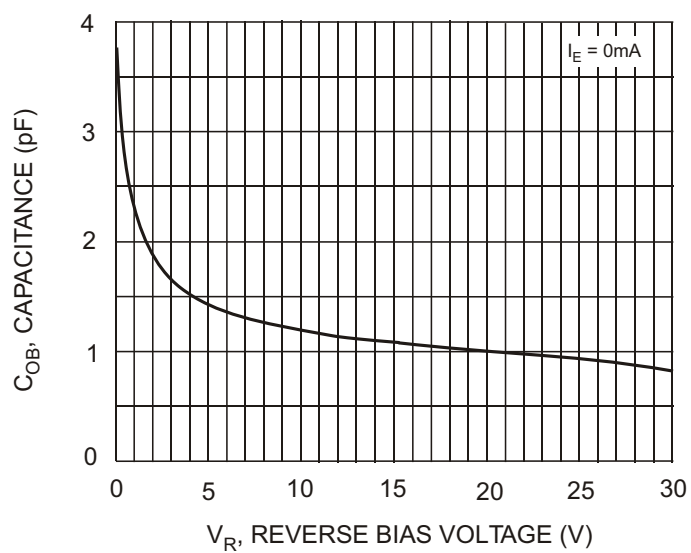


Fig. 4 Output Capacitance

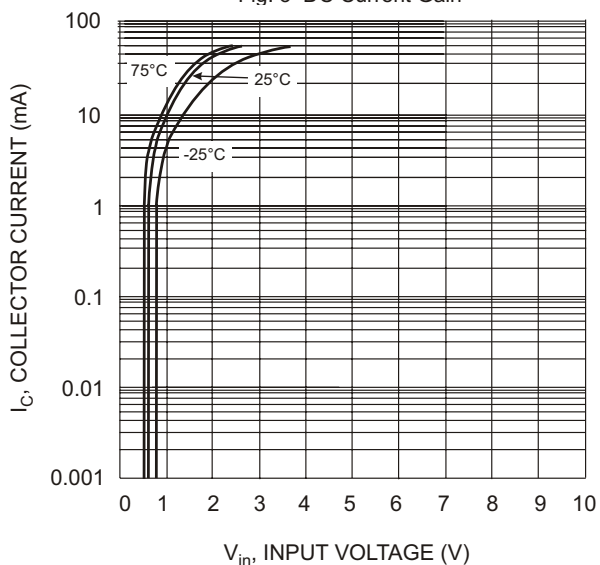


Fig. 5 Collector Current Vs. Input Voltage

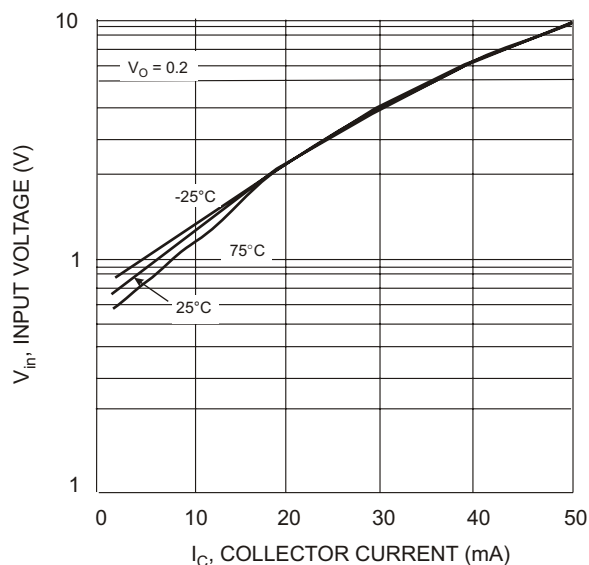


Fig. 6 Input Voltage vs. Collector Current