Low-Voltage, Low r_{ON}, Dual DPDT Analog Switch

FEATURES

- Low Voltage Operation (2.7 V to 3.3 V)
- Low On-Resistance - r_{ON}: 0.85 Ω
- 3 dB Loss @ 100 MHz
- Fast Switching: t_{ON} = 40 ns, t_{OFF} = 35 ns
- QFN-16 Package

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8-V Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

DESCRIPTION

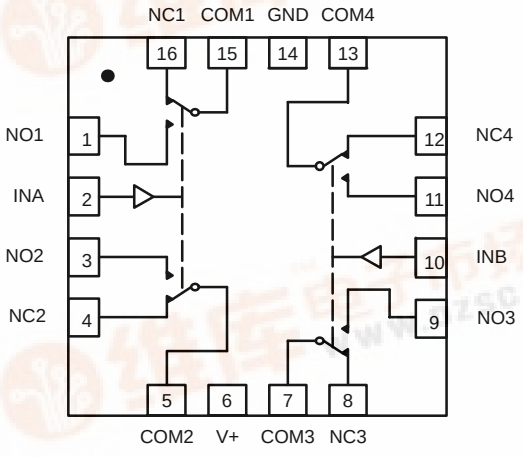
The DG2015 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2015 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2015 is built on Vishay Siliconix's low voltage JI2 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG2015
QFN-16 (4 X 4)



Top View

TRUTH TABLE		
Logic	**NC1, 2, 3 and 4**	**NO1, 2, 3 and 4**
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	16-Pin QFN (4 x 4 mm)	DG2015DN

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ . . . . . -0.3 to +6 V

IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)

Current (Any terminal except NO, NC or COM) . . . . . 30 mA

Continuous Current (NO, NC, or COM) . . . . . ±150 mA

Peak Current . . . . . ±200 mA

(Pulsed at 1 ms, 10% duty cycle)

Storage Temperature (D Suffix) . . . . . -65 to 150°C

Package Solder Reflow Conditions[d]

16-Pin QFN (4 x 4 mm) . . . . . 240°C

Power Dissipation (Packages)[b]

QFN-16[c] . . . . . 1880 mW

Notes:

a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 23.5 mW/°C above 70°C
d. Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC}, V_{COM}		Full	0		V+	V
On-Resistance	r_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V/1.5 V, I_{NO}, I_{NC} = 100 mA	Room Full		0.85	1.6 1.7	Ω
r_{ON} Flatness	r_{ON} Flatness	V+ = 2.7 V V_{COM} = 0 to V+, I_{NO}, I_{NC} = 100 mA	Room		0.16		Ω
r_{ON} Match	Δr_{ON}		Room		0.15		Ω
Switch Off Leakage Current	$I_{NO(off)}$, $I_{NC(off)}$	V+ = 3.3 V, V_{NO}, V_{NC} = 1 V/3 V V_{COM} = 3 V/1 V	Room Full	-1 -10		1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10		1 10	nA
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	-1 -10		1 10	nA
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	V
Input Capacitance	C_{in}		Full		4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	-1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2.0 V, R_L = 300 Ω, C_L = 35 pF	Room Full		40	65 67	ns
Turn-Off Time	t_{OFF}		Room Full		35	60 62	ns
Break-Before-Make Time	t_d		Full	1	3		ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		7		pC
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		-67		dB
Crosstalk[d]	X_{TALK}		Room		-70		dB
N_O, N_C Off Capacitance[d]	$C_{NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		63		pF
	$C_{NC(off)}$		Room		67		pF
Channel-On Capacitance[d]	$C_{NO(on)}$		Room		200		pF
	$C_{NC(on)}$		Room		196		pF

SPECIFICATIONS (V+ = 3 V)

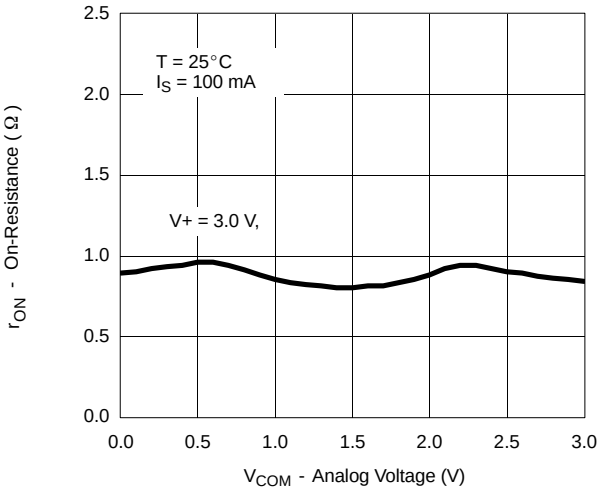
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.4 or 2.0 V[e]	Temp[a]	Limits -40 to 85°C Min[b]	Typ[c]	Max[b]	Unit
Power Supply							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	V_{IN} = 0 or V+	Full			1.0	µA
Power Consumption	P_C		Full			3.3	µW

Notes:

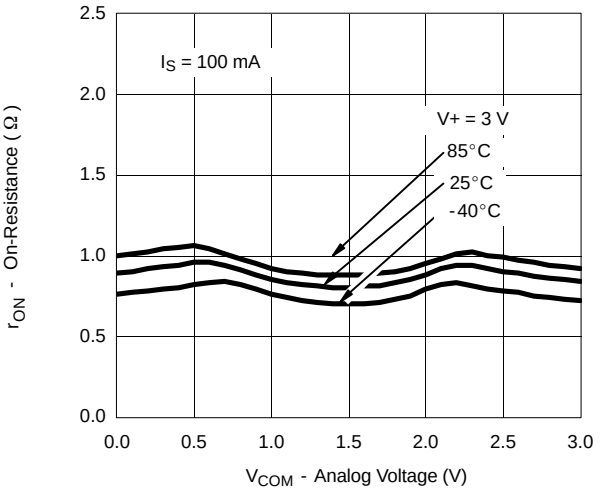
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Guaranteed by 5-V leakage testing, not production tested.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

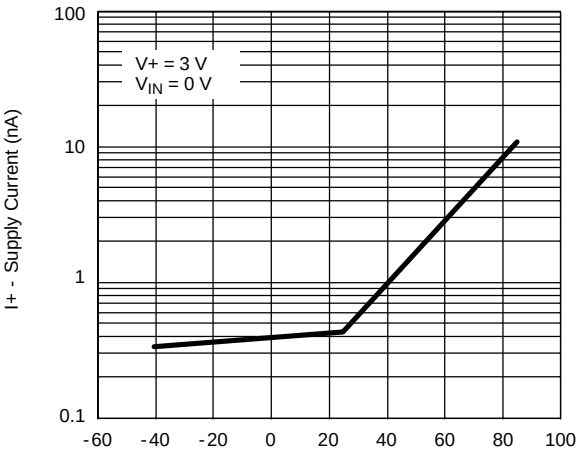
r_{ON} vs. V_{COM} and Supply Voltage



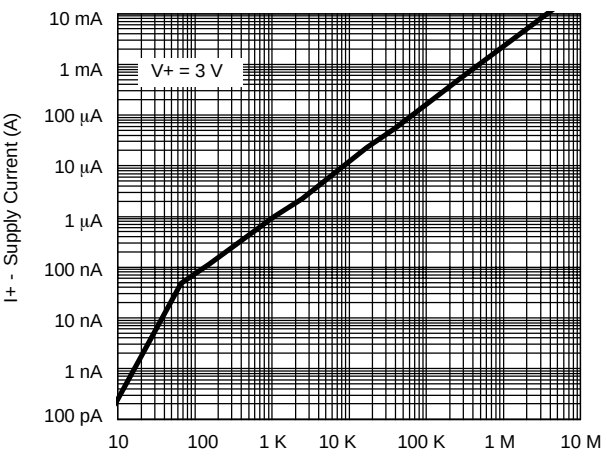
r_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

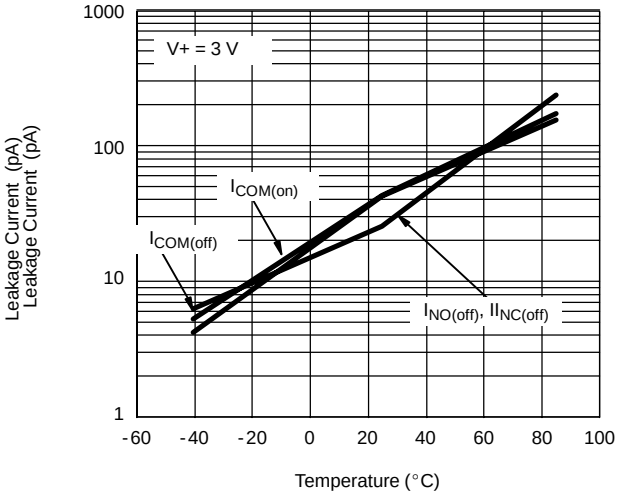


Supply Current vs. Input Switching Frequency

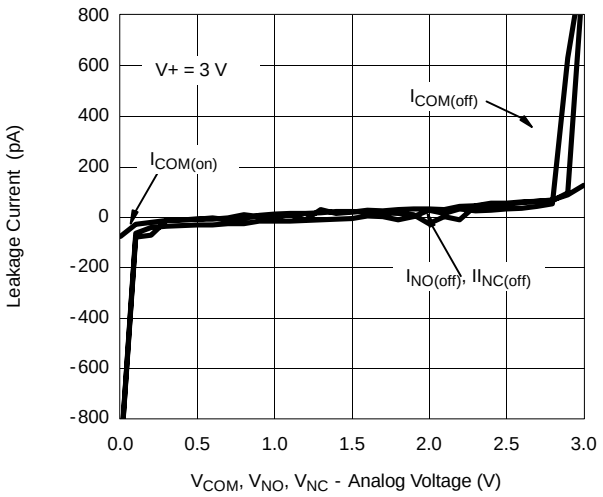


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

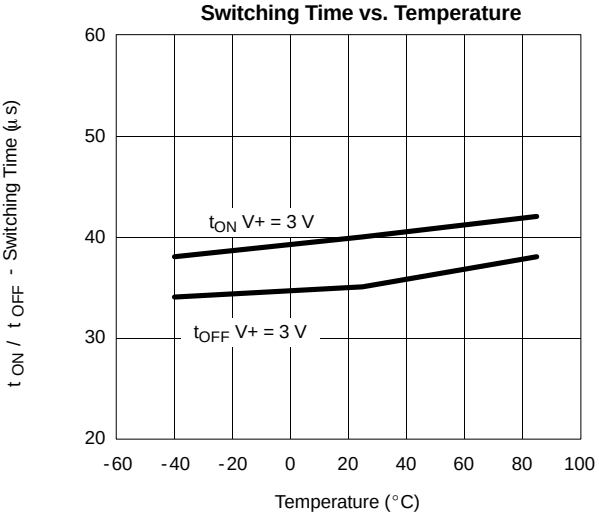
Leakage Current vs. Temperature



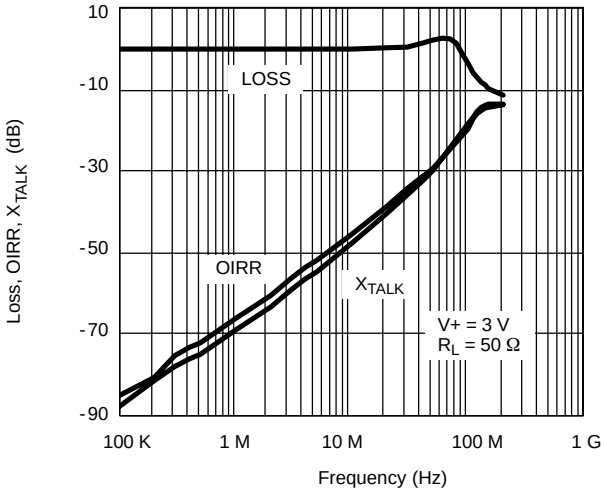
Leakage vs. Analog Voltage



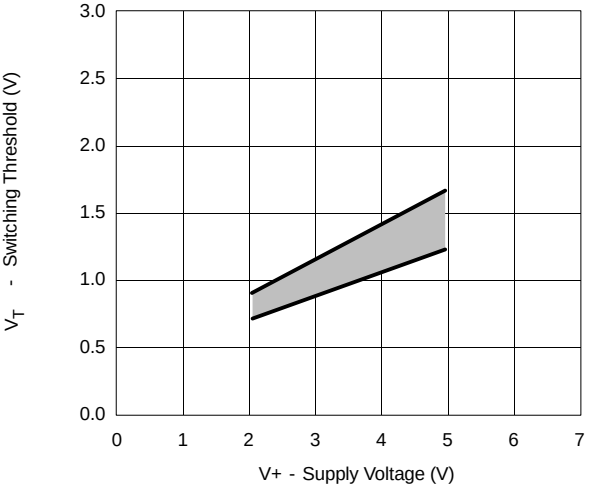
Switching Time vs. Temperature



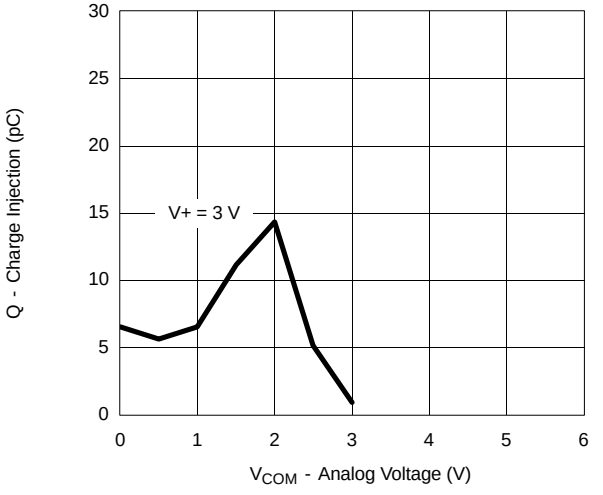
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



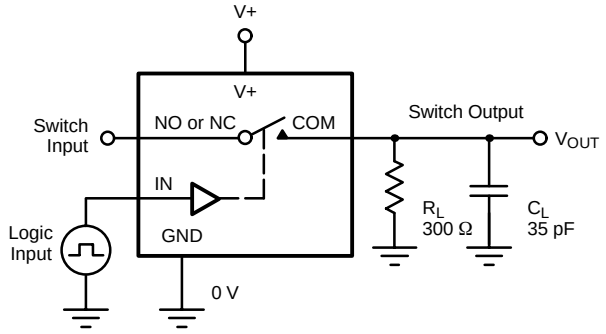
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

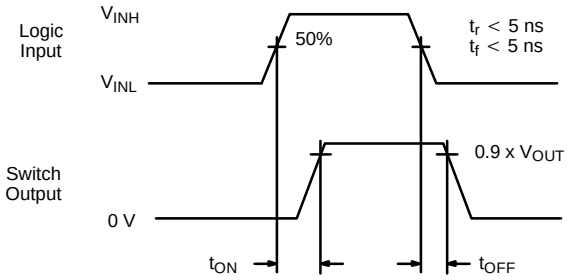


TEST CIRCUITS



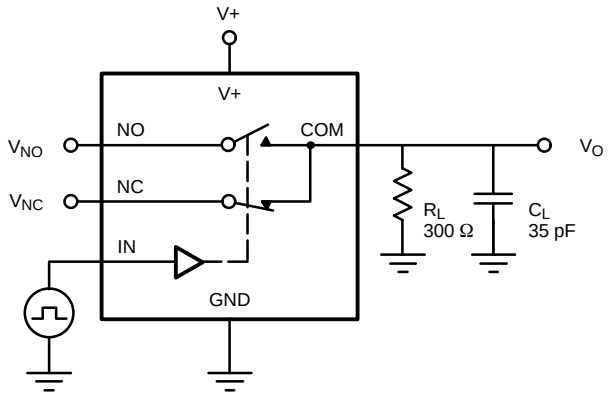
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

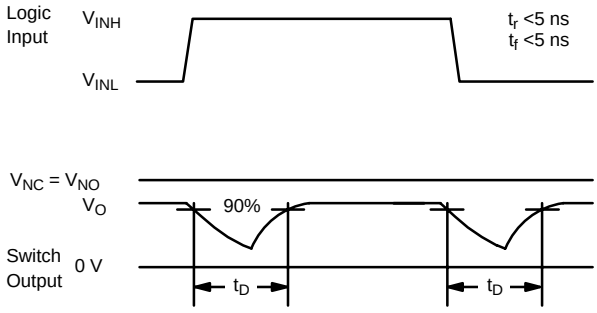
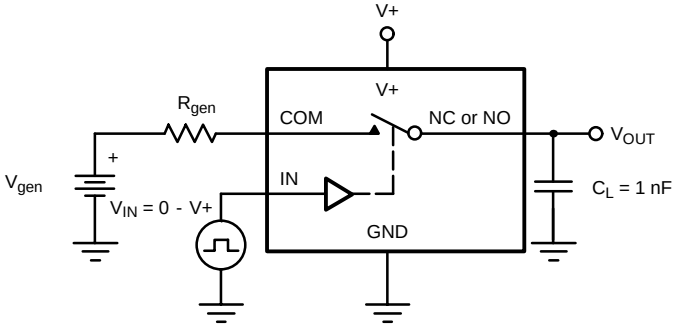
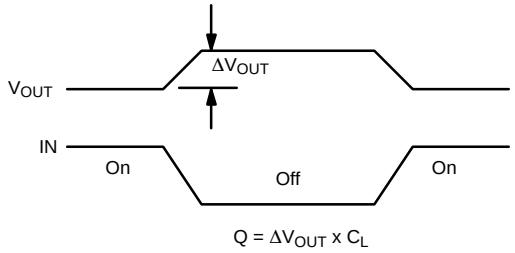


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

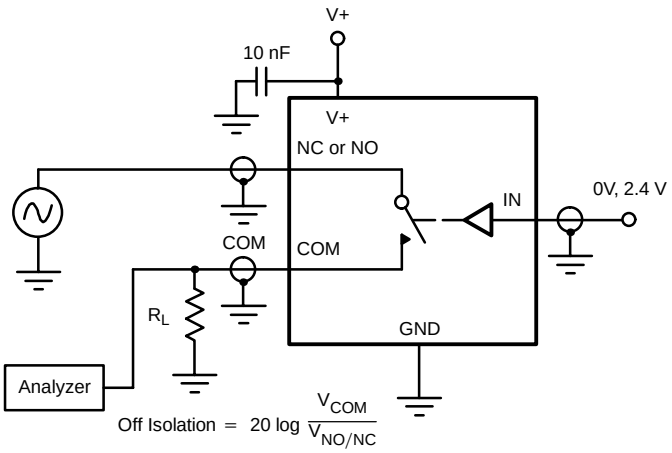


Figure 4. Off-Isolation

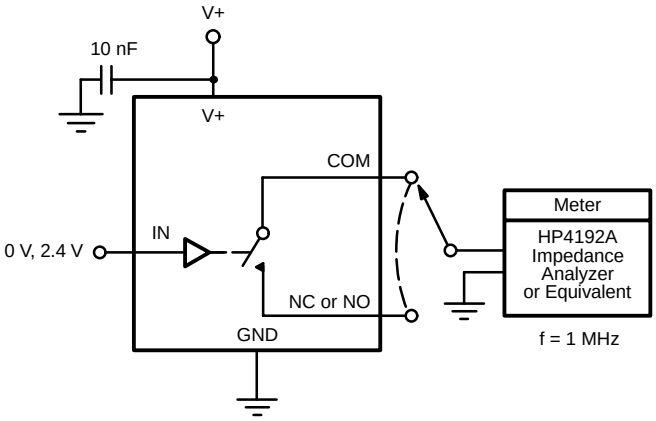


Figure 5. Channel Off/On Capacitance