Siliconix incorporated

DG243
Monolithic General Purpose CMOS Analog Switch

T-51-11

FEATURES

- PLUS-40 Process
- Make-Before-Break Operation
- Full Rail-to-Rail Analog Signal Range
- True TTL Compatibility

BENEFITS

- Reduced Power Supply Considerations
- Reduced Switching Noise
- Reduced Need for Buffers
- Pull-Up Resistors Not Required

APPLICATIONS

- Programmable Gain Amplifiers
- Analog Multiplexing
- Servo Control Systems

DESCRIPTION

The DG243 is a monolithic dual SPDT analog switch designed for general switching applications in communication, instrumentation, and process control systems. Featuring make-before-break action, the DG243 can be used in closed loop systems to switch gain or bandwidth networks without opening the loop.

The DG243 is designed on the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 40 V. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 Volts peak-to-peak when OFF. ON resistance is fairly flat over the full ±15 V analog signal range.

Packaging for this device includes a 16-pin CerDIP and plastic options. Performance grades include military, A suffix (–55 to 125°C) and commercial, C suffix (0 to 70°C) temperature ranges.

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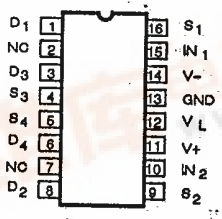
PIN CONFIGURATION

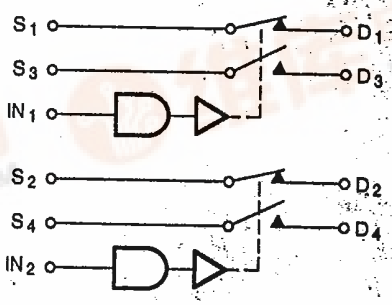
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG243AK, DG243AK/883
Plastic: DG243CK, DG243CJ

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

T-51-11

Voltages referenced to V–

V+ ..... 44 V

V_L ..... (GND –0.3 V) to 44 V

GND ..... 25 V

Digital Inputs[a] V_S, V_D ..... –2 V to (V+ +2V) or ..... 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A Suffix) .....–65 to 150°C
(C Suffix) .....–65 to 125°C

Operating Temperature (A Suffix) .....–55 to 125°C
(C Suffix) .....0 to 70°C

Power Dissipation*
16-Pin CerDIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 450 mW

* All leads soldered or welded to PC board.
** Derate 12 mW/°C above 75°C.
*** Derate 6 mW/°C above 75°C.

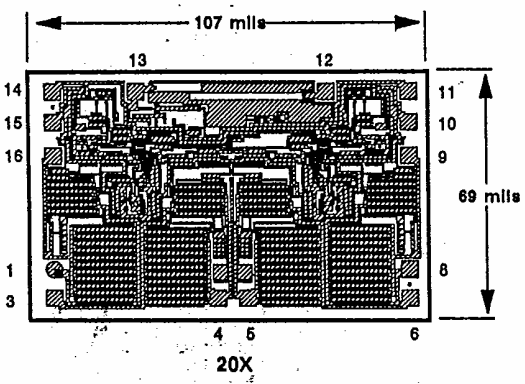
ELECTRICAL CHARACTERISTICS[a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = +15 V, V– = –15 V, GND = 0, V_L = 5 V	LIMITS 1=25°C 2=125,85,70°C 3=–55,–0°C		A SUFFIX –55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
SWITCH									
Analog Signal Range[c]	V_{ANALOG}		1,2,3		–15	15	–15	15	V
Drain-Source ON Resistance	$r_{DS(ON)}$	V_D = ± 10 V, I_S = 10 mA	1,3 2	30		50 75		50 75	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 14 V, V_D = –14 V	1 2	0.2		1 100		1 100	nA
		V_S = –14 V, V_D = 14 V	1 2	–0.3	–1 –100		–1 –100		
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = –14 V, V_D = 14 V	1 2	0.17		1 100		1 100	
		V_S = 14 V, V_D = –14 V	1 2	–0.35	–1 –100		–1 –100		
Drain ON Leakage Current	$I_{D(ON)}$	V_S = V_D = 14 V	1 2	0.05		2 200		2 200	
		V_S = V_D = –14 V	1 2	–0.04	–2 –200		–2 –200		
INPUT									
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 2.0 V	1 2	–0.01	–1 –1	1 1	–1 –1	1 1	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0.8 V	1 2	–0.005	–1 –1	1 1	–1 –1	1 1	

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V+ = +15 V, V- = -15 V, GND = 0, V_L = 5 V	LIMITS 1=25°C, 2=125,85,70°C, 3=-55,0°C		A SUFFIX -55 to 125°C		C SUFFIX 0 to 70°C		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
DYNAMIC									
Turn-ON Time	t_{ON}	See Switching Time Test Circuit	1	250		500		700	ns
Turn-OFF Time	t_{OFF}		1	390		1000		1200	
Charge Injection	Q	C_L = 1000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	1	60					pC
Source-OFF Capacitance	$C_{S(OFF)}$	$V_D = V_S$ = 0 V, V_{IN} = 0 V, f = 1 MHz	1	15					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		1	17					
Channel ON Capacitance	$C_{D(ON)} + C_{S(ON)}$		1	45					
OFF Isolation [e]		V_{IN} = 5 V, Z_L = 75 Ω	1	75					dB
Crosstalk (Channel-to-Channel)		V_S = 2.0 V, f = 1MHz	1	89					
SUPPLY									
Positive Supply Current	I+	All Channels ON or OFF	1	180		300		300	µA
Negative Supply Current	I-		1	-150	-300		-300		
Logic Supply Current	I_L		1	100		300		300	
Ground Supply Current	I_{GND}		1	-140	-300		-300		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
   For Logic "1" - V_{INH} = 2.0 V
   For Logic "0" - V_{INL} = 0.8 V



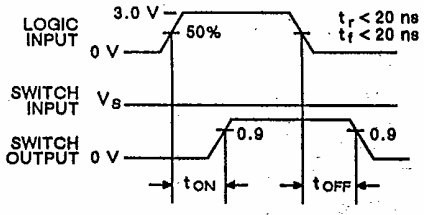
Pad No.	Function
1	Drain 1
3	Drain 3
4	Source 3
5	Source 4
6	Drain 4
8	Drain 2
9	Source 2
10	Input 2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	Input 1
16	Source 1

ICMKC

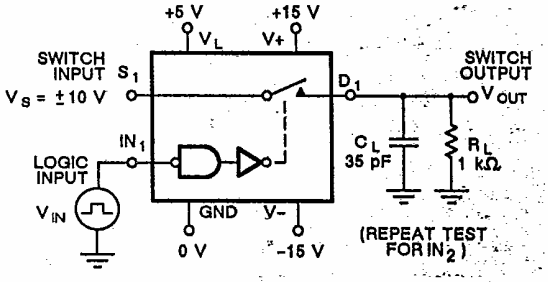
9 Capacitors
6 Resistors
31 P-channel enhancement MOSFET
33 N-channel enhancement MOSFETs
9 Diodes

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

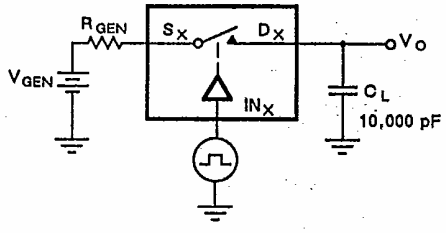


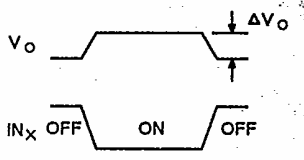
NOTE: Logic input waveform is inverted for switches that have the opposite logic sense control.



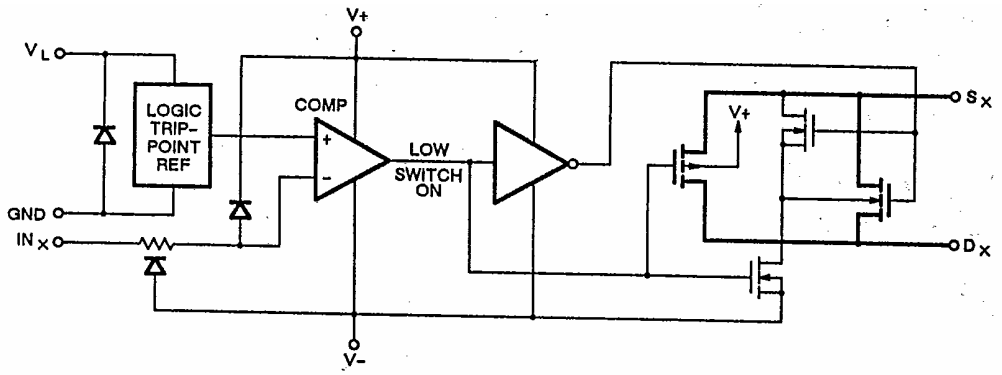
$$V_{OUT} = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

CHARGE INJECTION TEST CIRCUIT





ΔV_O = measured voltage error due to charge injection.
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$.



APPLICATIONS

The make-before-break operation of the DG243 provides simple transient suppression in these two important applications.

Figure 1 shows a minimum amount of glitching during changes of gain states. The relatively low impedance of the gain setting resistors 10 k, 1 kΩ, 100 Ω shunt the injected charge to ground minimizing transient effects occurring at the inverting input of the op amp. Consequently, these transients are not amplified to V_{OUT}.

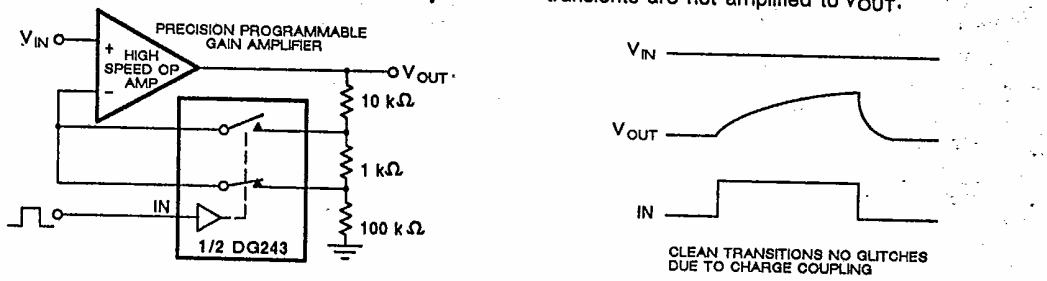


Figure 1. Improving Transient Response in Programmable Gain Amplifiers. "Getting Rid of Glitches".

Figure 2 takes advantage of the make-before-break operation of the DG243 by shorting transition current to real ground instead of virtual ground. The best results are obtained by selecting an op amp with the proper offset voltage specification.

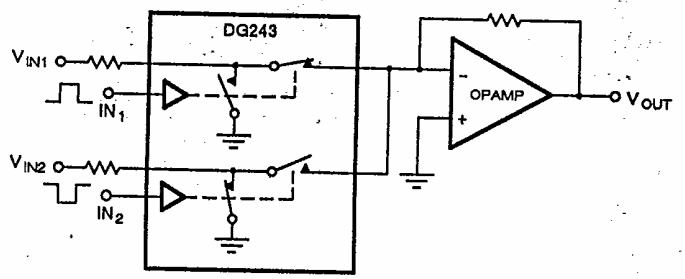


Figure 2. Minimizing Glitches in Audio Switching