



**DG3157**

Vishay Siliconix

## High-Speed, Low $r_{ON}$ , SPDT Analog Switch (2:1 Multiplexer/Demultiplexer Bus Switch)

### DESCRIPTION

The DG3157 is a high-speed single-pole double-throw, low power, TTL-Compatible bus switch. Using sub-micro CMOS technology, the DG3157 achieves low on-resistance and negligible propagation delay.

The DG3157 can handle both analog and digital signals and permits signals with amplitudes of up to  $V_{CC}$  to be transmitted in either direction.

When the Select pin is low,  $B_0$  is connected to the output A pin. When the Select pin is high,  $B_1$  is connected to the output A pin. The path that is open will have a high-impedance state with respect to the output. Make-before-break is guaranteed. An epitaxial layer prevents latch-up.

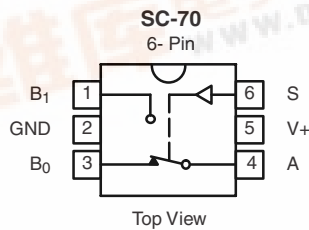
### FEATURES

- Direct Cross to Industry Standard *SN74LVC1G3157, NC7SB3157, NLASB3175, PI5A3157, and STG3157*
- SC-70 6-Lead Package
- 1.65 V to 5.5 V  $V_{CC}$  Operation
- 5  $\Omega$  Connection Between Ports
- Minimal Propagation Delay
- Break-Before-Make Switching
- Zero Bounce In Flow-Through Mode



**RoHS\***  
COMPLIANT

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: G1

TRUTH TABLE	
Logic Input (S)	Function
0	$B_0$ Connected to A
1	$B_1$ Connected to A

ORDERING INFORMATION		
Temp Range	Package	Part Number
- 40 to 85 °C	SC70-6	DG3157DL-T1 DG3157DL-T1-E3





ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
S, A, B <sup>a</sup>		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature	D Suffix	- 65 to 150	°C
Power Dissipation (Packages) <sup>b</sup>	6-Pin SC70 <sup>c</sup>	250	mW

Notes:

- a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 3.1 mW/°C above 70 °C.

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V <sub>S</sub> = 0.25 V to 0.7 V+ <sup>e</sup>		Temp <sup>a</sup>	Limits - 40 to 85 °C			Unit
					Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>DC Characteristics</b>								
High Level Input Voltage	V <sub>SH</sub>	V+ = 1.65 to 1.95 V		Full	0.75 V+		V	
		V+ = 2.3 to 5.5 V		Full	0.7 V+			
Low Level Input Voltage	V <sub>SL</sub>	V+ = 1.65 to 1.95 V		Full		0.25 V+	V	
		V+ = 2.3 to 5.5 V		Full		0.3 V+		
On Resistance	R <sub>ON</sub>	V+ = 4.5 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 30 mA	Full		6	7	Ω
			V <sub>BN</sub> = 2.3 V, I <sub>A</sub> = - 30 mA	Full		6	12	
			V <sub>BN</sub> = 4.5 V, I <sub>A</sub> = - 30 mA	Full		9	15	
		V+ = 3.0 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 24 mA	Full		8	9	
			V <sub>BN</sub> = 3.0 V, I <sub>A</sub> = - 24 mA	Full		12	20	
		V+ = 2.3 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 8 mA	Full		9	12	
			V <sub>BN</sub> = 2.3 V, I <sub>A</sub> = - 8 mA	Full		13	30	
		V+ = 1.65 V	V <sub>BN</sub> = 0 V, I <sub>A</sub> = 4 mA	Full		12	20	
V <sub>BN</sub> = 1.8 V, I <sub>A</sub> = - 4 mA	Full			18	50			
On Resistance Flatness	R <sub>FLAT</sub>	0 < V <sub>BN</sub> < V+	V+ = 4.5 V, I <sub>A</sub> = - 30 mA	Room		6		
			V+ = 3.0 V, I <sub>A</sub> = - 24 mA	Room		12		
			V+ = 2.3 V, I <sub>A</sub> = - 8 mA	Room		22		
			V+ = 1.65 V, I <sub>A</sub> = - 4 mA	Room		90		
On Resistance Matching Between Channels	ΔR <sub>ON</sub>		V+ = 4.5 V, V <sub>BN</sub> = 3.15 V, I <sub>A</sub> = - 30 mA	Room		0.32		
			V+ = 3.0 V, V <sub>BN</sub> = 2.1 V, I <sub>A</sub> = - 24 mA	Room		0.31		
			V+ = 2.3 V, V <sub>BN</sub> = 1.6 V, I <sub>A</sub> = - 8 mA	Room		0.30		
			V+ = 1.65 V, V <sub>BN</sub> = 1.15 V, I <sub>A</sub> = - 4 mA	Room		0.29		
Input Leakage Current	I <sub>S</sub>	V+ = 5.5 V, V <sub>A</sub> = 5.5 V		Room Full	- 0.1 - 1.0		μA	
Off Stage Switch Leakage	I <sub>BN(off)</sub>	V+ = 5.5 V, V <sub>A</sub> /V <sub>B</sub> = 0 V/5.5 V		Room Full	- 0.1 - 1.0			
On State Switch Leakage	I <sub>BN(on)</sub>	V+ = 5.5 V, V <sub>A</sub> /V <sub>B</sub> = 0 V/5.5 V		Room Full	- 0.1 - 1.0			
<b>Power Supply</b>								
Power Supply Range	V+			Full	1.65		5.5	V
Quiescent Supply Current	I+	V+ = 5.5 V, V <sub>A</sub> = V <sub>B</sub> = V+ or GND		Room Full			1 10	μA



SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 3.0\text{ V}$ , $V_S = 0.25\text{ V to }0.7\text{ V}^{+e}$			Limits - 40 to 85 °C			Unit
		Temp <sup>a</sup>	Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>			
<b>AC Electrical Characteristic</b>								
Prop Delay Time <sup>f</sup>	$t_{PHL}/t_{PLH}$	$V_A = 0\text{ V}$	$V_+ = 1.65\text{ to }1.95\text{ V}$	Full				ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Full		1.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Full		0.8		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Full		0.3		
Output Enable Time <sup>f</sup>	$t_{PZL}/t_{PZH}$	$V_{LOAD} = 2 \times V_+$ for $t_{PZL}$ $V_{LOAD} = 0\text{ V}$ for $t_{PZH}$	$V_+ = 1.65\text{ to }1.95\text{ V}$	Room Full		10.2 10.4		ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Room Full		5.9 6.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Room Full		4.1 4.5		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Room Full		2.6 2.9		
Output Disable Time <sup>f</sup>	$t_{PLZ}/t_{PHZ}$	$V_{LOAD} = 2 \times V_+$ for $t_{PLZ}$ $V_{LOAD} = 0\text{ V}$ for $t_{PHZ}$	$V_+ = 1.65\text{ to }1.95\text{ V}$	Room Full		10.2 10.4		ns
			$V_+ = 2.3\text{ to }2.7\text{ V}$	Room Full		5.9 6.2		
			$V_+ = 3.0\text{ to }3.6\text{ V}$	Room Full		4.1 4.5		
			$V_+ = 4.5\text{ to }5.5\text{ V}$	Room Full		2.6 2.9		
Break-Before-Make Time <sup>d</sup>	$t_{BBM}$	$V_+ = 1.65\text{ to }1.95\text{ V}$	Full	0.5				
		$V_+ = 2.3\text{ to }2.7\text{ V}$	Full	0.5				
		$V_+ = 3.0\text{ to }3.65$	Full	0.5				
		$V_+ = 4.5\text{ to }5.5\text{ V}$	Full	0.5				
Charge Injection <sup>d</sup>	Q	$C_L = 0.1\text{ nF}$ , $V_{GEN} = 0\text{ V}$ $R_{GEN} = 0\ \Omega$	$V_+ = 5\text{ V}$	Room		7	pC	
			$V_+ = 3.3\text{ V}$	Room		3		
<b>Analog Switch Characteristics</b>								
Off Isolation <sup>d</sup>	OIRR	$R_L = 50\ \Omega$ , $f = 10\text{ MHz}$	Room		- 57.6		dB	
Crosstalk <sup>d</sup>	$X_{TALK}$		Room		- 58.7			
- 3-db Bandwidth <sup>d</sup>	BW	$R_L = 50\ \Omega$	Room		> 250		MHz	
<b>Capacitance</b>								
Control Pin Capacitance <sup>d</sup>	$C_{IN}$	$V_+ = 0\text{ V}$	Room		4.9		pF	
B Port Off Capacitance <sup>d</sup>	$C_{IO-B}$	$V_+ = 5\text{ V}$	Room		< 6.5			
A Port Capacitance When Switch Enable <sup>d</sup>	$C_{IO-A(on)}$		Room		< 18.5			

Notes:

- a. Room = 25 °C, Full = as determined by the operating suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for design aid only, not guaranteed nor subject to production testing.
- d. Guarantee by design, nor subjected to production test.
- e.  $V_{IN}$  = input voltage to perform proper function.
- f. Guaranteed by design and not production tested. The bus switch propagation delay is a function of the RC time constant contributed by the on-resistance and the specified load capacitance with an ideal voltage source (zero output impedance) driving the switch.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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## LOGIC DIAGRAM (POSITIVE LOGIC)

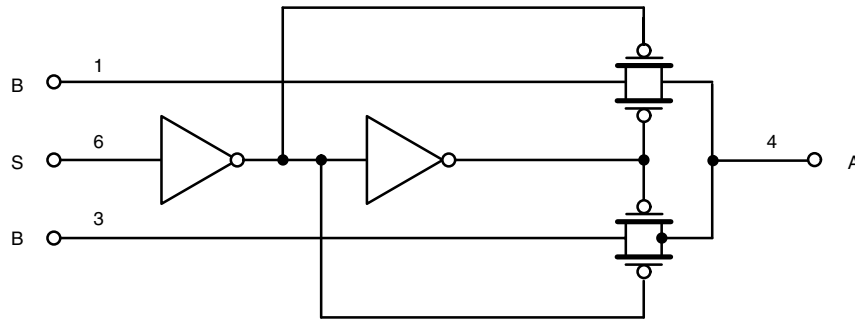
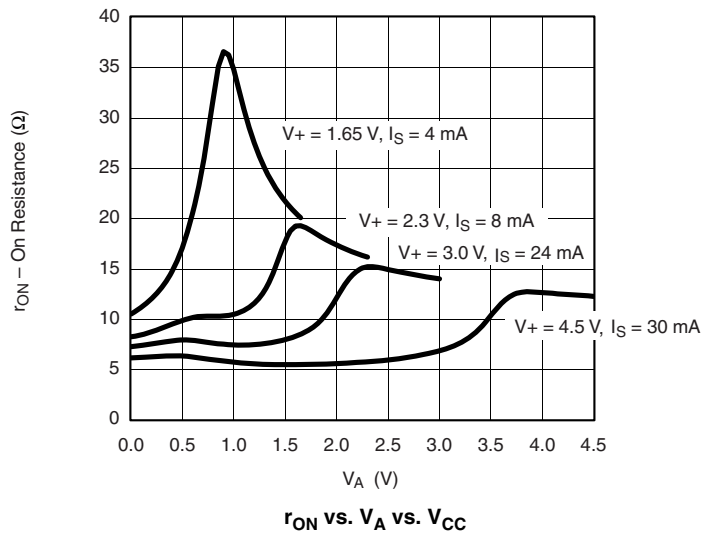
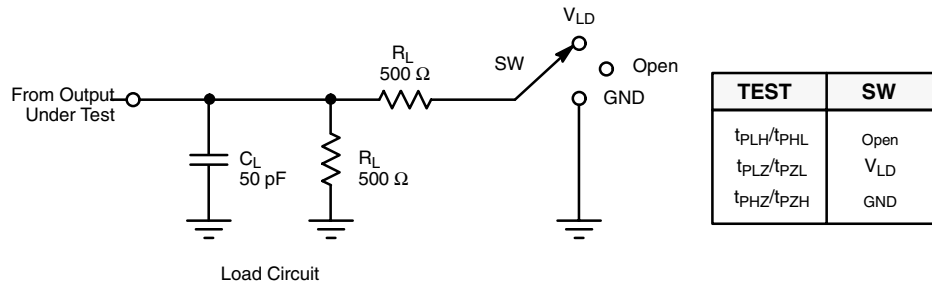


Figure 1.

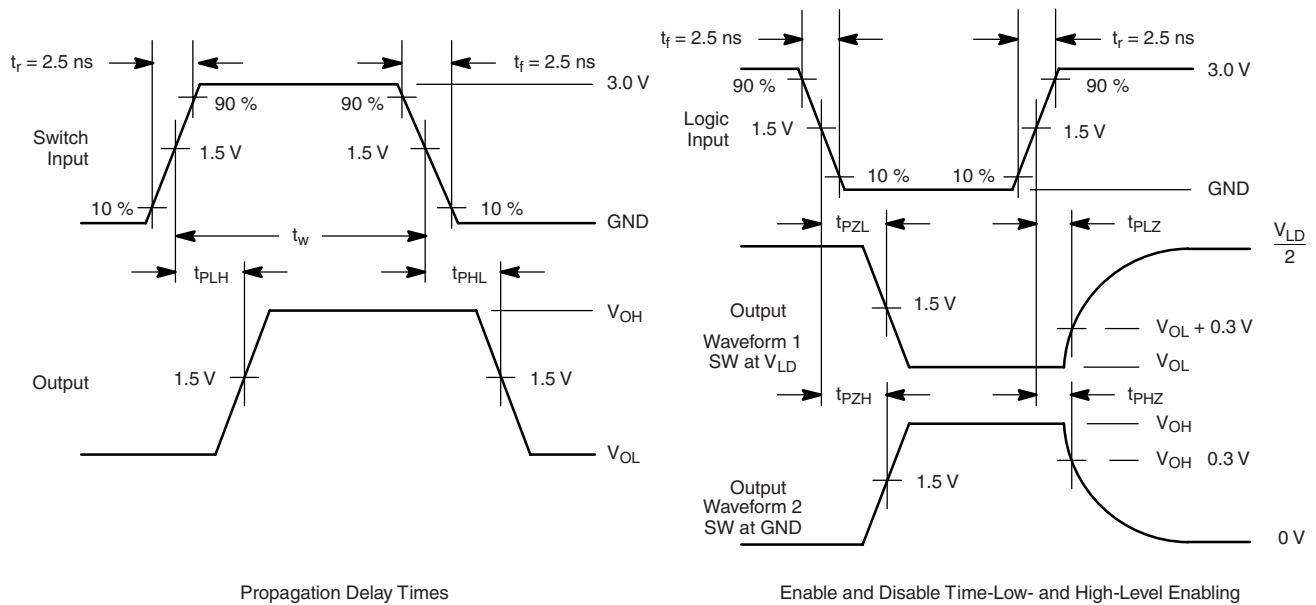
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



**AC LOADING AND WAVEFORMS**



**Figure 2. AC Test Circuit**

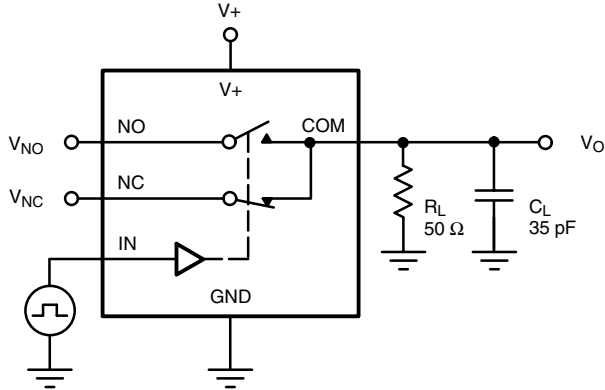


**Figure 3. AC Waveforms**

**Notes:**

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
- Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ .
- The outputs are measured one at a time with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{dis}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{dis}$ .
- $V_{LD} = 2 \text{ V+}$ .

TEST CIRCUITS



$C_L$  (includes fixture and stray capacitance)

Figure 4. Break-Before-Make Interval

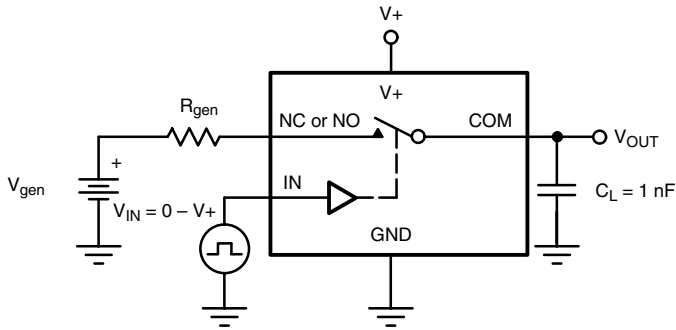
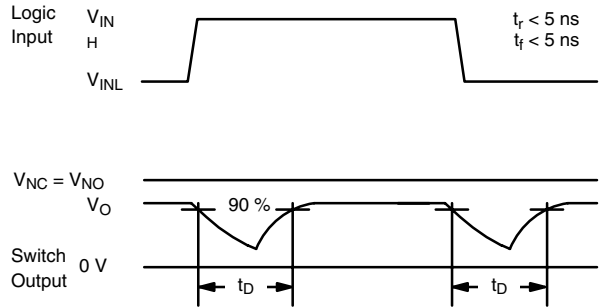
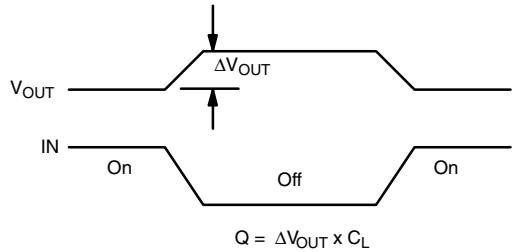
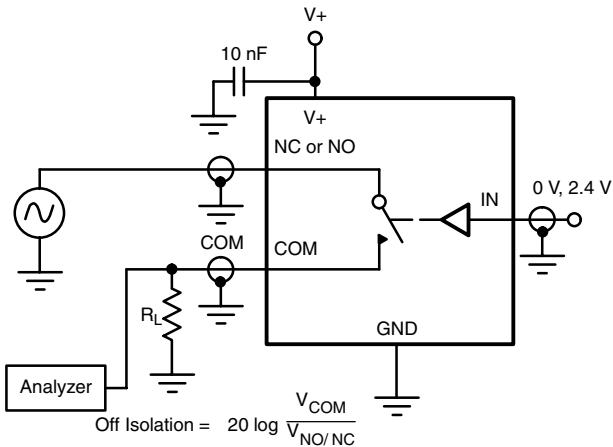


Figure 5. Charge Injection



IN depends on switch configuration: input polarity determined by sense of switch.



$$\text{Off Isolation} = 20 \log \frac{V_{COM}}{V_{NO/NC}}$$

Figure 6. Off-Isolation

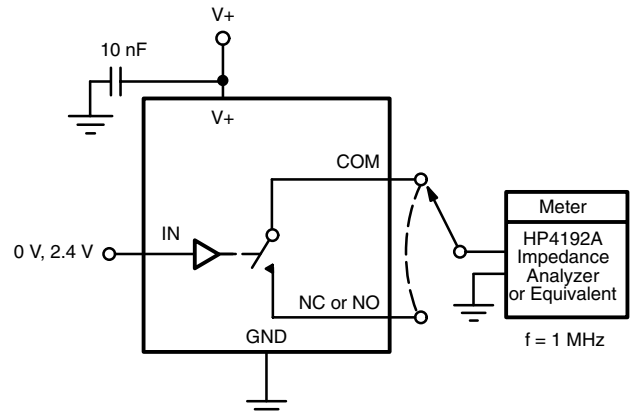


Figure 7. Channel Off/On Capacitance



### Disclaimer

All product specifications and data are subject to change without notice.

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