



# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

DG406/DG407

## General Description

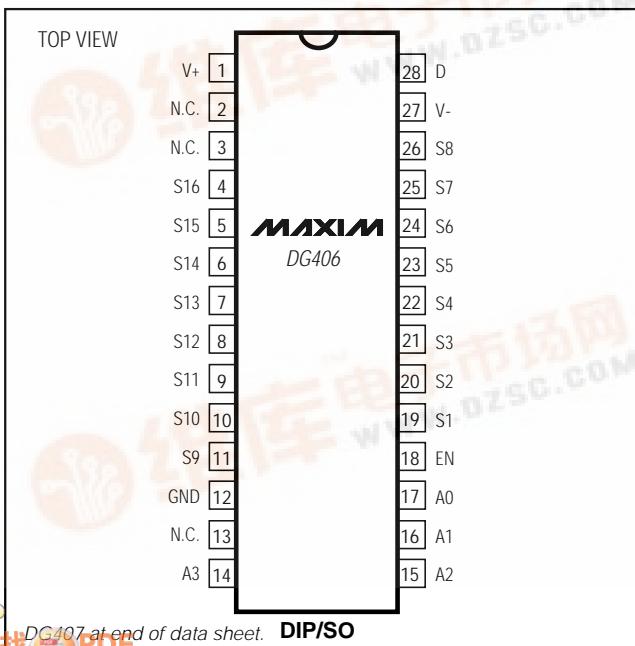
Maxim's redesigned DG406 and DG407 CMOS analog multiplexers now feature guaranteed matching between channels ( $8\Omega$  max) and flatness over the specified signal range ( $9\Omega$  max). These low on-resistance muxes ( $100\Omega$  max) conduct equally well in either direction and feature guaranteed low charge injection ( $15\text{pC}$  max). In addition, these new muxes offer low input off-leakage current over temperature—less than  $5\text{nA}$  at  $+85^\circ\text{C}$ .

The DG406 is a 1 of 16 multiplexer/demultiplexer and the DG407 is a dual 8-channel multiplexer/demultiplexer. Both muxes operate with a  $+4.5\text{V}$  to  $+30\text{V}$  single supply and with  $\pm 4.5\text{V}$  to  $\pm 20\text{V}$  dual supplies. ESD protection is guaranteed to be greater than  $2000\text{V}$  per Method 3015.7 of MIL-STD 883. These improved muxes are pin-compatible plug-in upgrades for the industry standard DG406 and DG407.

## Applications

- Sample-and-Hold Circuits
- Test Equipment
- Guidance and Control Systems
- Communications Systems
- Data-Acquisition Systems
- Audio Signal Routing

## Pin Configurations



## Features

- ♦ Pin-Compatible Plug-In Upgrade for Industry Standard DG406/DG407
- ♦ Guaranteed Matching Between Channels,  $8\Omega$  Max
- ♦ Guaranteed On-Resistance Flatness,  $9\Omega$  Max
- ♦ Guaranteed Low Charge Injection,  $15\text{pC}$  Max
- ♦ Low On-Resistance  $100\Omega$  Max
- ♦ Input Leakage,  $5\text{nA}$  Max at  $+85^\circ\text{C}$
- ♦ Low Power Consumption,  $1.25\text{mW}$  Max
- ♦ Rail-to-Rail Signal Handling
- ♦ Digital Input Controls TTL/CMOS Compatible
- ♦ ESD Protection  $>2000\text{V}$  per Method 3015.7

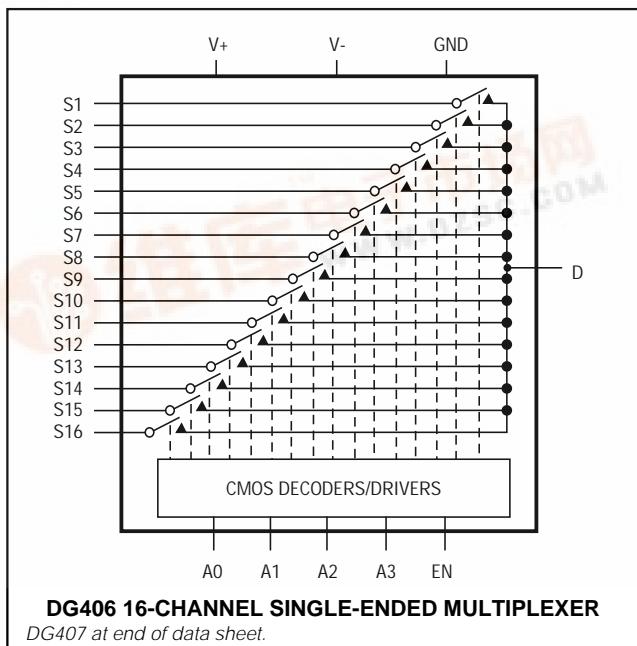
## Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
<b>DG406CJ</b>	$0^\circ\text{C}$ to $+70^\circ\text{C}$	28 Plastic DIP
DG406CWI	$0^\circ\text{C}$ to $+70^\circ\text{C}$	28 Wide SO
DG406C/D	$0^\circ\text{C}$ to $+70^\circ\text{C}$	Dice*
DG406DJ	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	28 Plastic DIP
DG406DWI	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	28 Wide SO
DG406DN	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	28 PLCC
DG406AK	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	28 CERDIP

**Ordering Information continued at end of data sheet.**

\* Contact factory for dice specifications.

## Functional Diagrams



# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

## ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+	-0.3V, 44V
GND	-0.3V, 25V

Digital Inputs, S, D (Note 1)	(V <sub>-</sub> - 2V) to (V <sub>+</sub> + 2V) or 30mA (whichever occurs first)
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Continuous Current (any terminal)	30mA
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Peak Current, S or D (pulsed at 1ms, 10% duty cycle max)	100mA
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Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
-------------------------------------------------------	--

Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
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**Note 1:** Signals on S<sub>-</sub>, D<sub>-</sub>, A<sub>0</sub>, A<sub>1</sub>, A<sub>2</sub>, A<sub>3</sub>, or EN exceeding V<sub>+</sub> or V<sub>-</sub> are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS—Dual Supplies

(V<sub>+</sub> = 15V, V<sub>-</sub> = -15V, GND = 0V, V<sub>AH</sub> = +2.4V, V<sub>AL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
<b>SWITCH</b>								(Note 2)
Analog Signal Range	V <sub>ANALOG</sub>	(Note 3)			-15	15		
Drain-Source On-Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -1.0mA, V <sub>D</sub> = ±10V	T <sub>A</sub> = +25°C		60	100		Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			125		
On-Resistance Matching Between Channels	Δr <sub>DS(ON)</sub>	I <sub>S</sub> = -1.0mA, V <sub>D</sub> = ±10V (Note 4)	T <sub>A</sub> = +25°C		1.5	8		Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			10		
On-Resistance Flatness	r <sub>FLAT</sub>	I <sub>S</sub> = -1.0mA, V <sub>D</sub> = ±5V or 0V	T <sub>A</sub> = +25°C		1.8	9		Ω
			T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>			12		
Source-Off Leakage Current (Note 5)	I <sub>S(OFF)</sub>	V <sub>D</sub> = ±10V, V <sub>S</sub> = ±10V, V <sub>EN</sub> = 0V	T <sub>A</sub> = +25°C		-0.5	0.01	0.5	nA
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>	C, D	-5	5		
				A	-50	50		
Drain-Off Leakage Current (Note 5)	I <sub>D(OFF)</sub>	V <sub>D</sub> = ±10V, V <sub>S</sub> = ±10V, V <sub>EN</sub> = 0V	T <sub>A</sub> = +25°C		-1	0.02	1	nA
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>	C, D	-40	40		
				A	-200	200		
		V <sub>D</sub> = ±10V, V <sub>S</sub> = ±10V, V <sub>EN</sub> = 0V	T <sub>A</sub> = +25°C		-1	0.02	1	
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>	C, D	-20	20		
				A	-100	100		
Drain-On Leakage Current (Note 5)	I <sub>D(ON)</sub> + I <sub>S(ON)</sub>	V <sub>D</sub> = ±10V, V <sub>S</sub> = ±10V, sequence each switch on	T <sub>A</sub> = +25°C		-1	0.02	1	nA
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>	C, D	-40	40		
				A	-200	200		
		V <sub>D</sub> = ±10V, V <sub>S</sub> = ±10V, sequence each switch on	T <sub>A</sub> = +25°C		-1	0.02	1	
			TA = T <sub>MIN</sub> to T <sub>MAX</sub>	C, D	-20	20		
				A	-100	100		

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## ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

( $V_+ = 15V$ ,  $V_- = -15V$ ,  $GND = 0V$ ,  $V_{AH} = +2.4V$ ,  $V_{AL} = +0.8V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>INPUT</b>							
Input Current with Input Voltage High	$I_{AH}$	$V_A = 2.4V$ or $15V$			-1.0	1.0	$\mu A$
Input Current with Input Voltage Low	$I_{AL}$	$V_{EN} = 0V$ or $2.4V$ , $V_A = 0V$			-1.0	1.0	$\mu A$
<b>SUPPLY</b>							
Power-Supply Range					$\pm 4.5$	$\pm 20$	V
Positive Supply Current	$I_+$	$V_{EN} = V_A = 0V$ or $4.5V$		$T_A = +25^\circ C$	16	30	$\mu A$
				$T_A = T_{MIN}$ to $T_{MAX}$	75		
Negative Supply Current	$I_-$	$V_{EN} = 2.4V$ , $V_{A(ALL)} = 0V$ or $2.4V$		$T_A = +25^\circ C$	0.075	0.5	mA
				$T_A = T_{MIN}$ to $T_{MAX}$	1		
<b>DYNAMIC</b>							
Transition Time	$t_{TRANS}$	Figure 2		$T_A = +25^\circ C$	110	300	ns
				$T_A = T_{MIN}$ to $T_{MAX}$	400		
Break-Before-Make Interval	$t_{OPEN}$	Figure 4		$T_A = +25^\circ C$	10	40	ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		$T_A = +25^\circ C$	130	200	ns
				$T_A = T_{MIN}$ to $T_{MAX}$	400		
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		$T_A = +25^\circ C$	55	150	ns
				$T_A = T_{MIN}$ to $T_{MAX}$	300		
Charge Injection (Note 3)	$Q$	$C_L = 1.0nF$ , $V_S = 0V$ , $R_S = 0\Omega$ , Figure 5		$T_A = +25^\circ C$	2	15	pC
Off Isolation (Note 6)	$V_{ISO}$	$V_{EN} = 0V$ , $R_L = 1k\Omega$ , $f = 100kHz$ , Figure 6		$T_A = +25^\circ C$	-69		dB
Crosstalk Between Channels	$V_{CT}$	$V_{EN} = 2.4V$ , $f = 100kHz$ , $V_{GEN} = 1V_{P-P}$ , $R_L = 1k\Omega$ , Figure 7		$T_A = +25^\circ C$	-92		dB
Logic Input Capacitance	$C_{IN}$	$f = 1MHz$		$T_A = +25^\circ C$	8		pF
Source-Off Capacitance	$C_{S(OFF)}$	$f = 1MHz$ , $V_{EN} = V_S = 0V$ , Figure 8		$T_A = +25^\circ C$	8		pF
Drain-Off Capacitance	$C_{D(OFF)}$	$f = 1MHz$ , $V_{EN} = 0.8V$ , $V_D = 0V$ , Figure 8	$DG406$	$T_A = +25^\circ C$	130		pF
			$DG407$		65		
Drain-Source On Capacitance	$C_{D(ON)} + C_{S(ON)}$	$f = 1MHz$ , $V_{EN} = 2.4V$ , $V_D = 0V$ , Figure 8	$DG406$	$T_A = +25^\circ C$	140		pF
			$DG407$		70		

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## ELECTRICAL CHARACTERISTICS—Single Supply

(V<sub>+</sub> = 12V, V<sub>-</sub> = 0V, GND = 0V, V<sub>AH</sub> = +2.4V, V<sub>AL</sub> = +0.8V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
<b>SWITCH</b>							
Analog Signal Range	V <sub>ANALOG</sub>	(Note 3)		0		12	V
Drain-Source On-Resistance	r <sub>DS(ON)</sub>	I <sub>S</sub> = -1.0mA V <sub>D</sub> = 3V or 10V	T <sub>A</sub> = +25°C		120	175	Ω
<b>DYNAMIC</b>							
Transition Time (Note 3)	t <sub>TRANS</sub>	V <sub>S1</sub> = 8V, V <sub>S16</sub> = 0V, V <sub>A</sub> = 0V, Figure 2	T <sub>A</sub> = +25°C		130	450	ns
Enable Turn-On Time (Note 3)	t <sub>ON(EN)</sub>	V <sub>AL</sub> = 0V, V <sub>S1</sub> = 5V, Figure 3	T <sub>A</sub> = +25°C		105	600	ns
Enable Turn-Off Time (Note 3)	t <sub>OFF(EN)</sub>	V <sub>AL</sub> = 0V, V <sub>S1</sub> = 5V, Figure 3	T <sub>A</sub> = +25°C		80	300	ns
Charge Injection (Note 3)	Q	C <sub>L</sub> = 1.0nF, V <sub>S1</sub> = 0V, R <sub>S</sub> = 0Ω	T <sub>A</sub> = +25°C		2	10	pC

**Note 2:** The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

**Note 3:** Guaranteed by design.

**Note 4:** ΔR<sub>ON</sub> = R<sub>ON(MAX)</sub> - R<sub>ON(MIN)</sub>. On-resistance match between channels and flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.

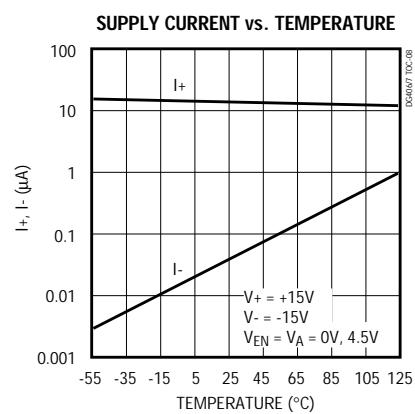
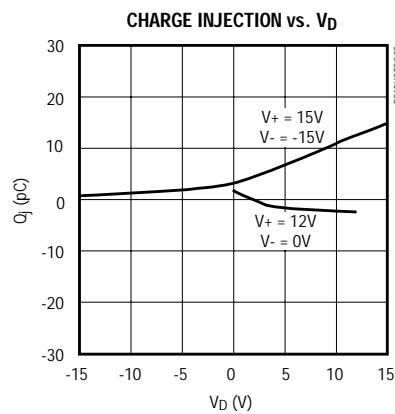
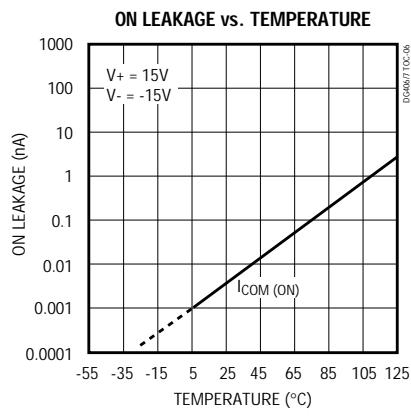
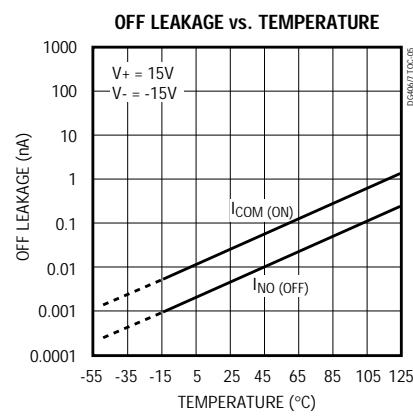
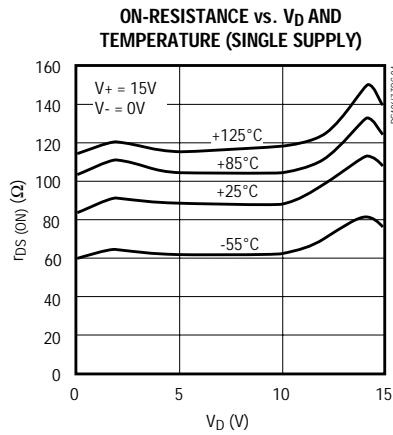
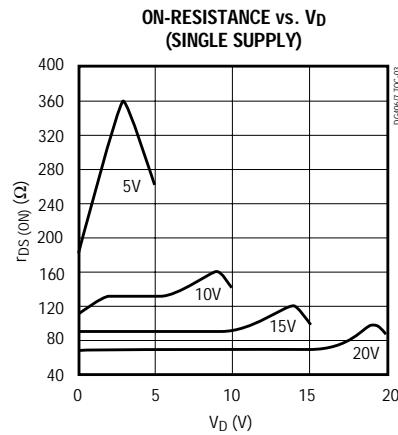
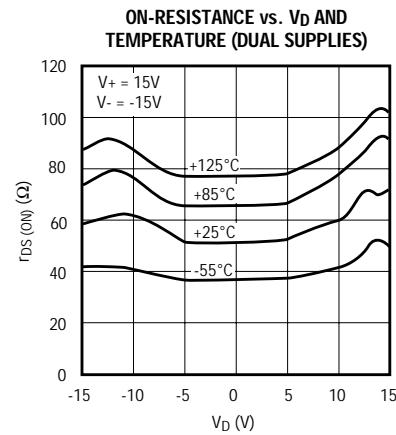
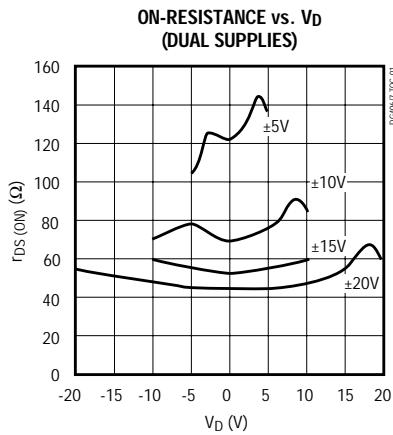
**Note 5:** Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

**Note 6:** Off isolation = 20log V<sub>D</sub>/V<sub>S</sub>, where V<sub>D</sub> = output and V<sub>S</sub> = input to off switch.

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## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



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## Pin Descriptions

DG406 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2, 3, 13	N.C.	No Internal Connections
4–11	S16–S9	Bidirectional Analog Inputs
12	GND	Ground
14–17	A3–A0	Address Inputs
18	EN	Enable Inputs
19–26	S1–S8	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	D	Bidirectional Output

DG407 PIN	NAME	FUNCTION
1	V+	Positive Supply Voltage Input
2	DB	Bidirectional Output B
3, 13, 14	N.C.	No Internal Connection
4–11	S8B–S1B	Bidirectional Analog Inputs
12	GND	Ground
15, 16, 17	A2, A1, A0	Address Inputs
18	EN	Enable Input
19–26	S1A–S8A	Bidirectional Analog Inputs
27	V-	Negative Supply Voltage Input
28	DA	Bidirectional Output A

## Applications Information

### Operation with Supply Voltages Other than $\pm 15V$

Using supply voltages other than  $\pm 15V$  reduces the analog signal range. The DG406/DG407 switches operate with  $\pm 4.5V$  to  $\pm 20V$  bipolar supplies or with a  $+4.5V$  to  $+30V$  single supply; connect V- to GND when operating with a single supply. Also, both device types can operate with unbalanced supplies such as  $+24V$  and  $-5V$ . The *Typical Operating Characteristics* graphs show typical on-resistance with  $20V$ ,  $15V$ ,  $10V$ , and  $5V$  supplies. (Switching times increase by a factor of two or more for operation at  $5V$ .)

### Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs and analog signals. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog

signal range to 1V above V+ and 1V below V-, but low switch resistance and low leakage characteristics are unaffected. Device operation is unchanged, and the difference between V+ and V- should not exceed  $+44V$ .

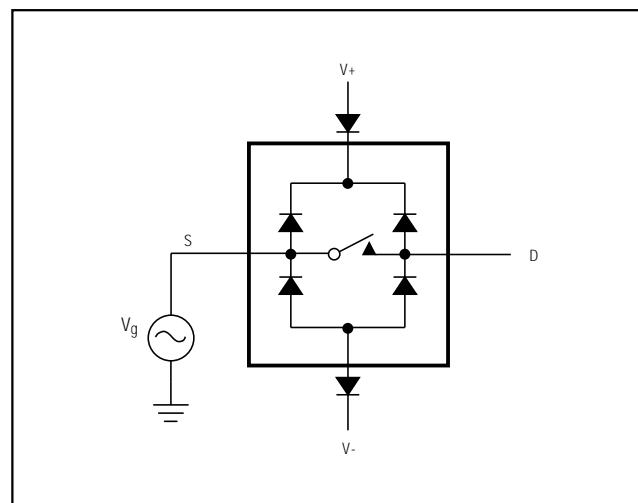


Figure 1. Overvoltage Protection Using External Blocking Diodes

# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

## Test Circuits/Timing Diagrams

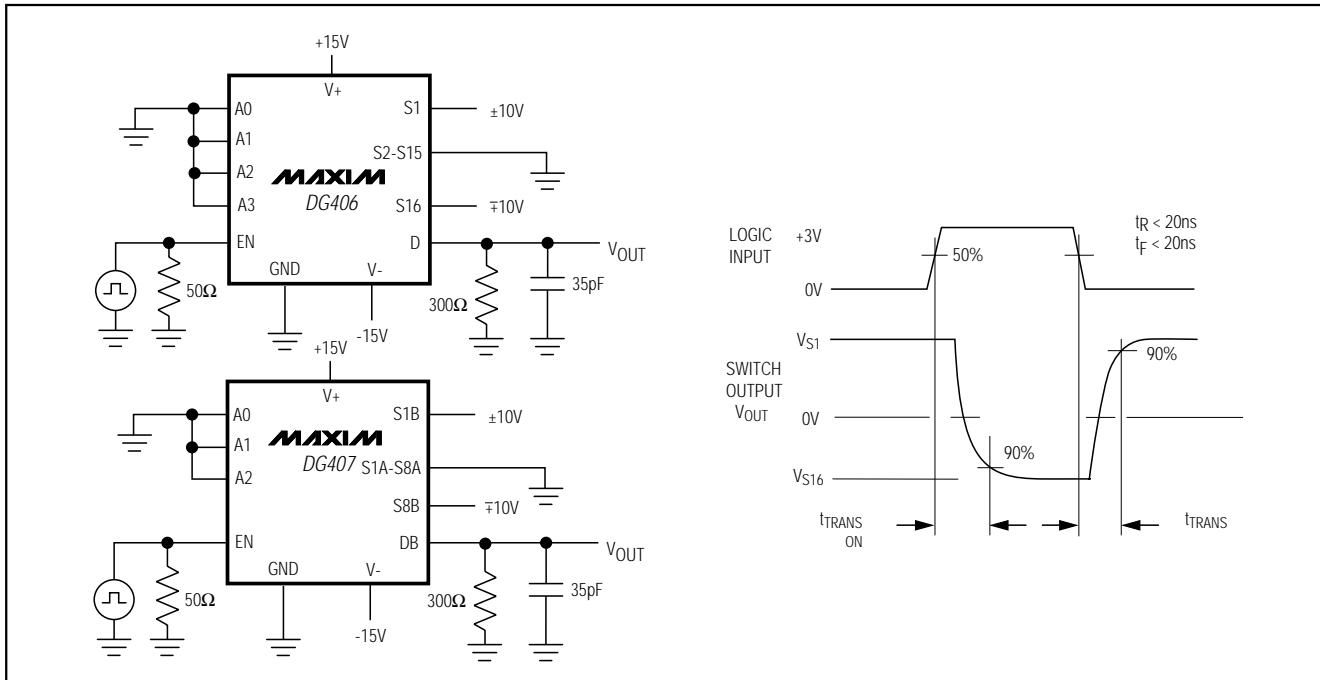


Figure 2. Transition Time

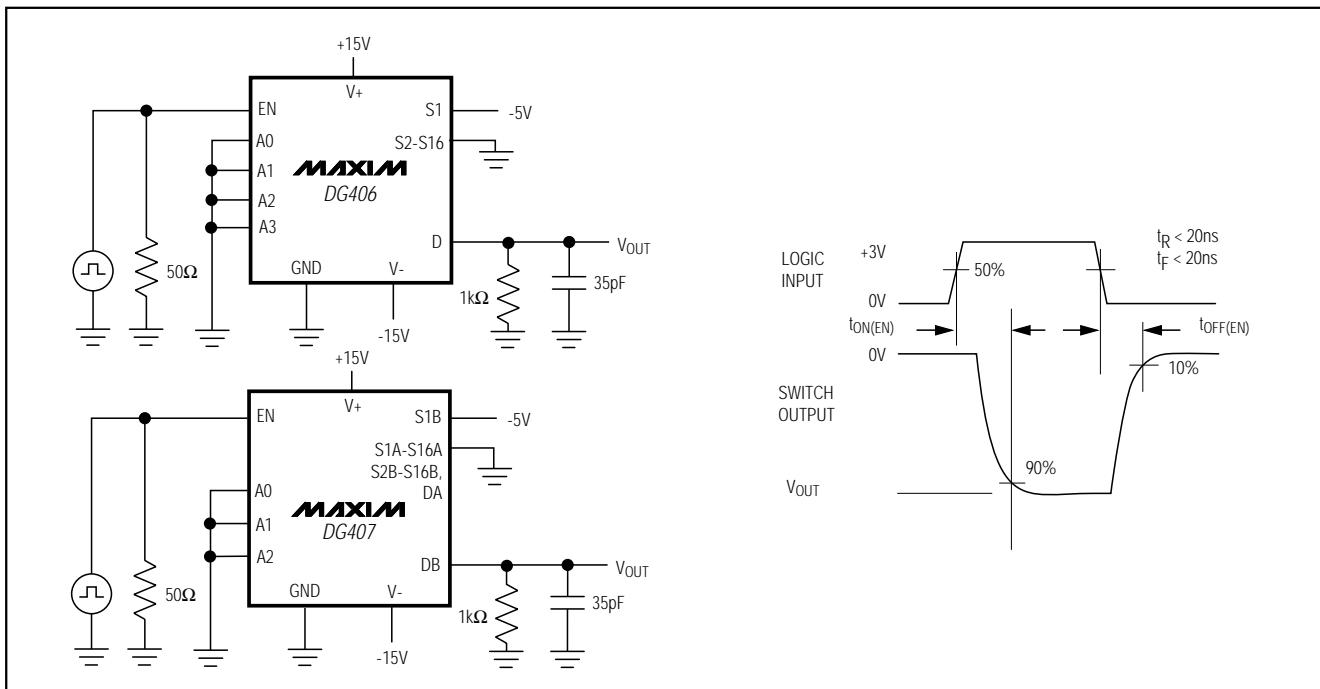


Figure 3. Enable Switching Time

## Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

### Test Circuits/Timing Diagrams (continued)

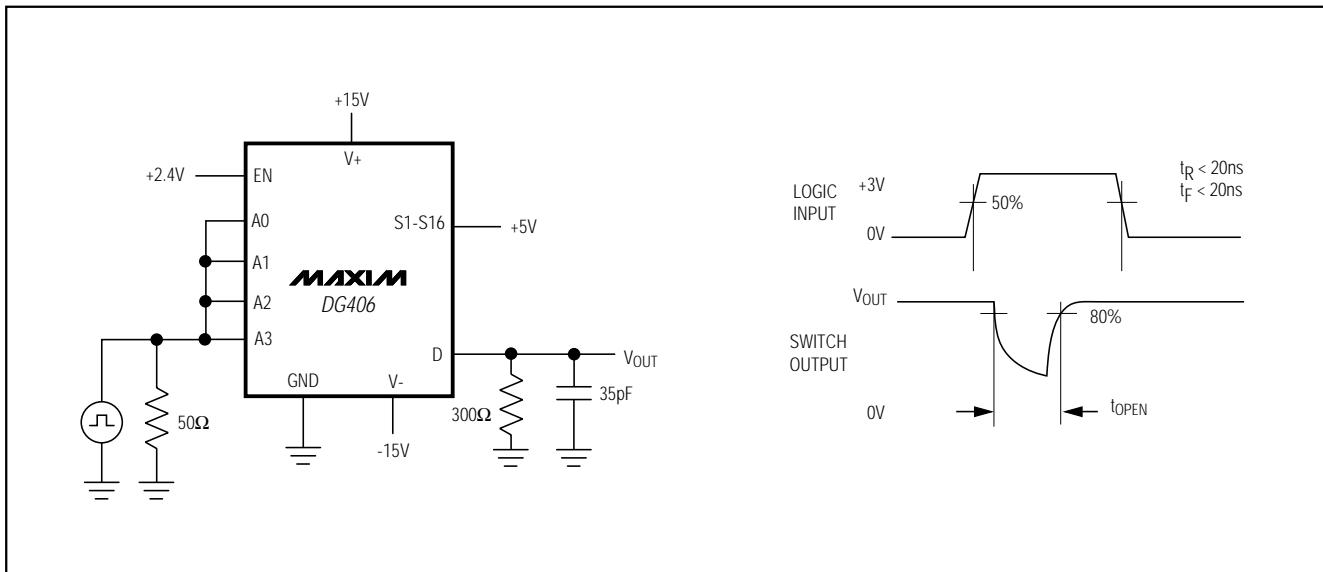


Figure 4. Break-Before-Make Interval

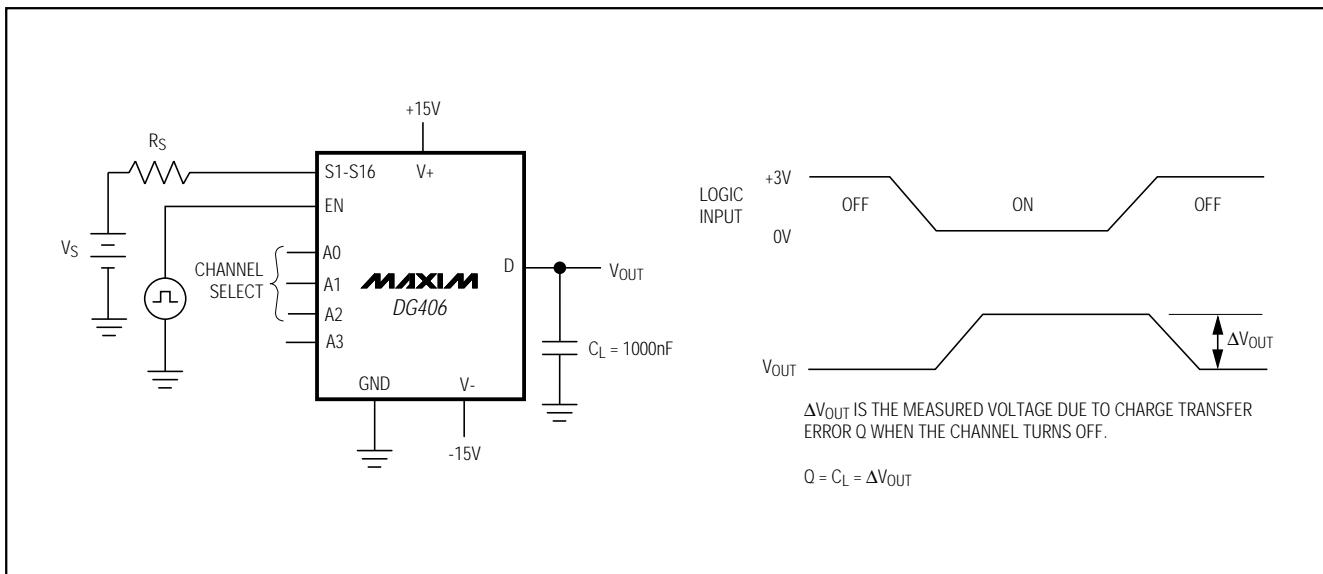


Figure 5. Charge Injection

# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

## Test Circuits/Timing Diagrams (continued)

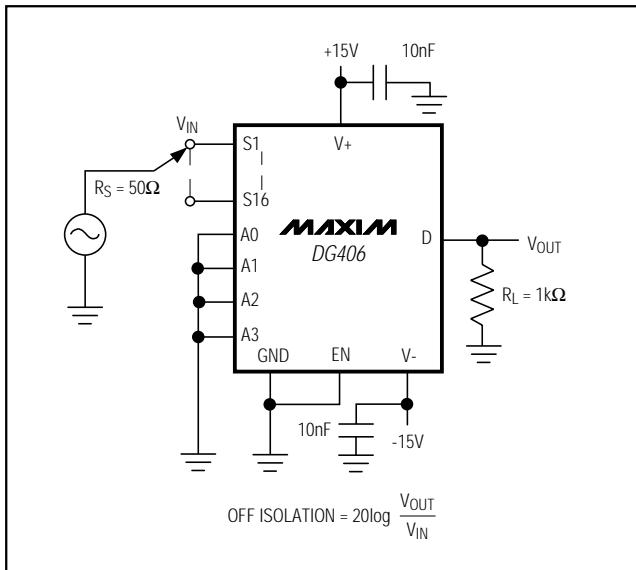


Figure 6. Off Isolation

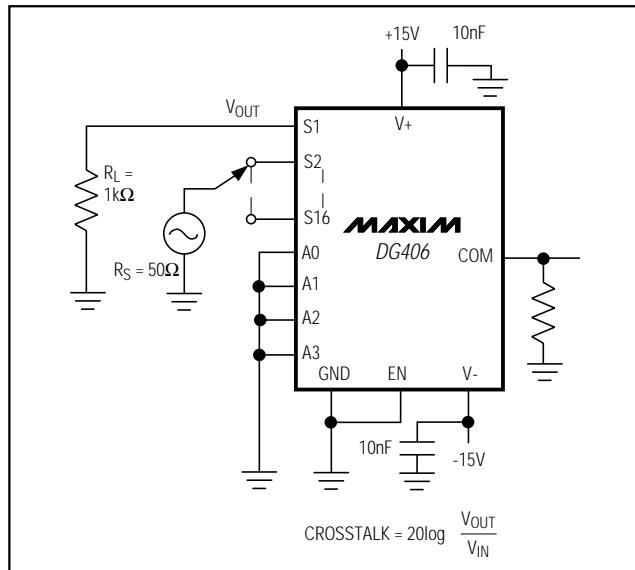


Figure 7. Crosstalk

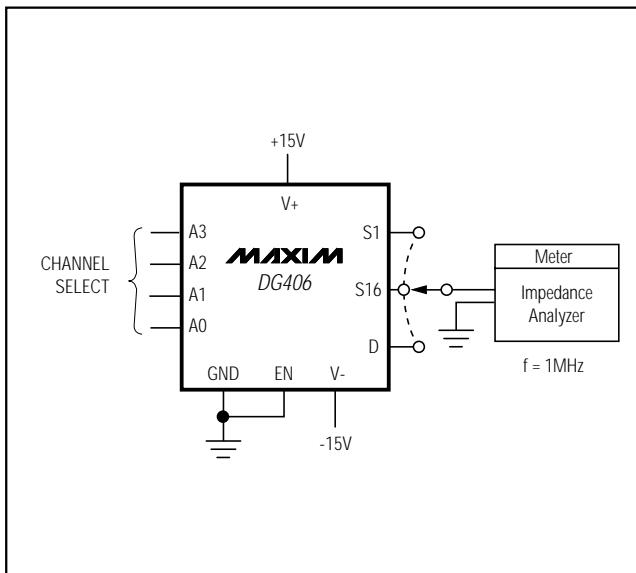
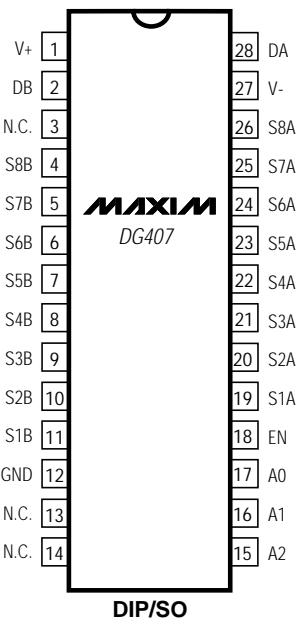


Figure 8. Source/Drain Capacitance

# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

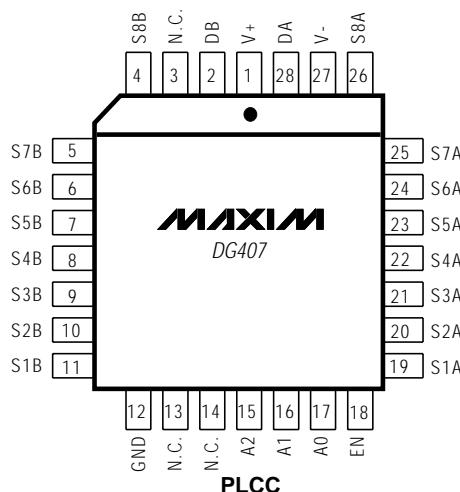
## Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG406

LOGIC "0"  $V_{AL} \leq 0.8V$ , LOGIC "1" =  $V_{AH} \geq 2.4V$ 

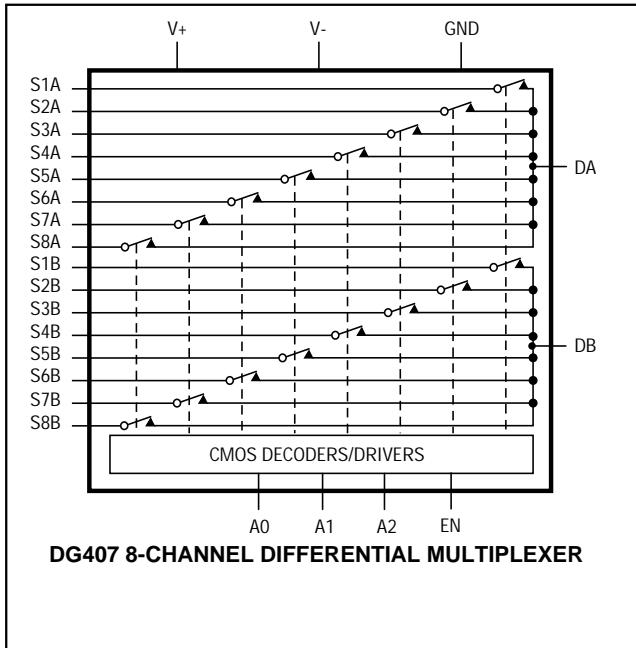
A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG407

LOGIC "0"  $V_{AL} \leq 0.8V$ , LOGIC "1" =  $V_{AH} \geq 2.4V$

## Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

### Functional Diagrams (continued)



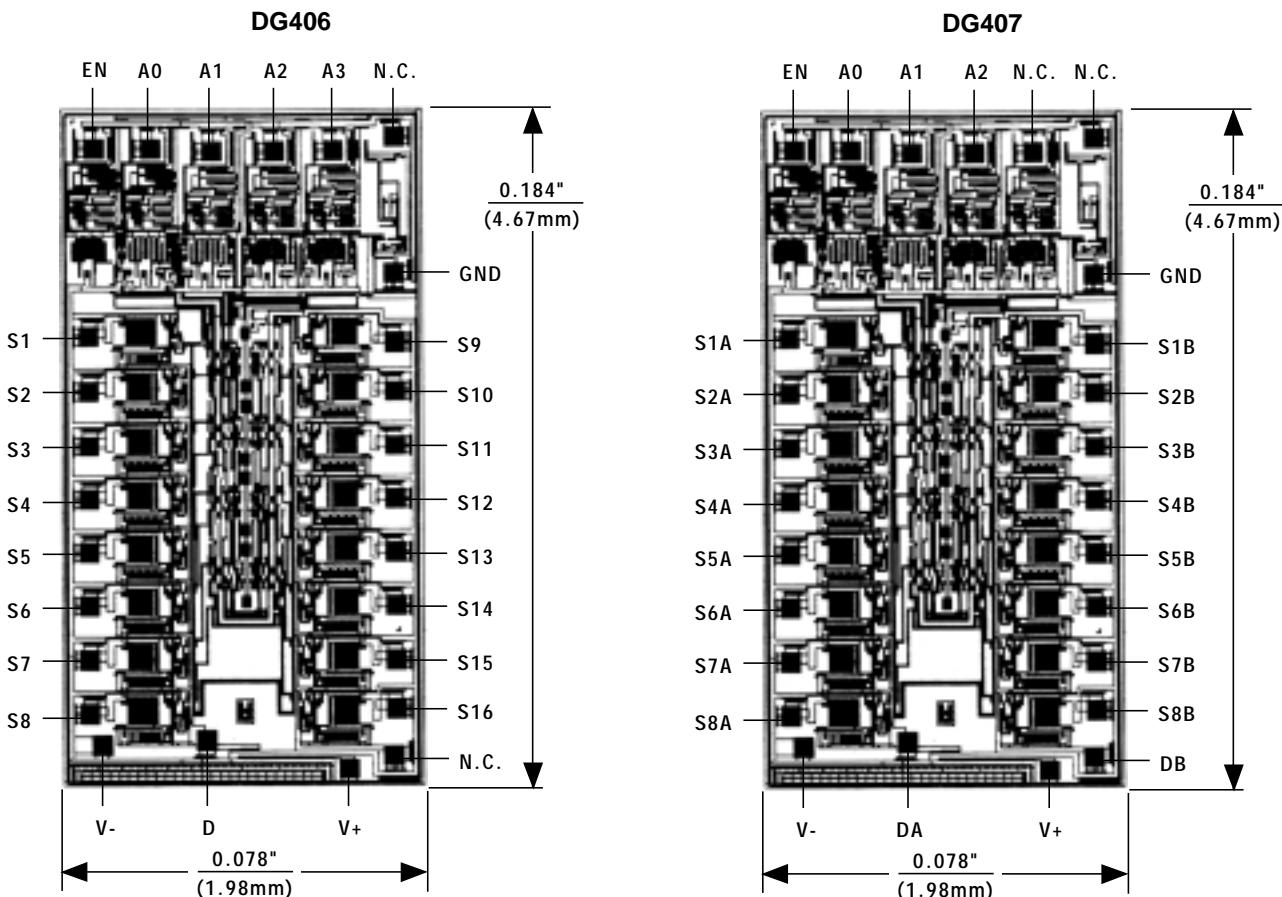
### Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
<b>DG407CJ</b>	0°C to +70°C	28 Plastic DIP
DG407CWI	0°C to +70°C	28 Wide SO
DG407C/D	0°C to +70°C	Dice*
DG407DJ	-40°C to +85°C	28 Plastic DIP
DG407DWI	-40°C to +85°C	28 Wide SO
DG407DN	-40°C to +85°C	28 PLCC
DG407AK	-55°C to +125°C	28 CERDIP

\* Contact factory for dice specifications.

# Improved, 16-Channel/Dual 8-Channel, CMOS Analog Multiplexers

## Chip Topographies



N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 269

SUBSTRATE IS INTERNALLY CONNECTED TO V+

TRANSISTOR COUNT: 269

SUBSTRATE IS INTERNALLY CONNECTED TO V+

*Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.*

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