Low Voltage, 1-Ω Single SPDT Analog Switch (1:2 Multiplexer) with Power Down Protection

DESCRIPTION

The DG4157 is a high performance single pole double throw analog switch designed for 1.8 V to 5.5 V operation with single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance as 1 Ω at 4.5 V power supply and fast switching speed. The - 3 dB bandwidth is typically 117 MHz.

The DG4157 features break before make switch performance, and guarantees logic HIGH control input threshold as low as 1.4 V over the range up to 5.5 V.

It can handle both analog and digital signals and permits signals with amplitudes of up to V_{CC} to be transmitted in either direction.

Power down protection circuit is built in to prevent abnormal current path through signal pins during power down condition.

Each output pin (A, B_0, or B_1) can withstand greater than 8 kV (human body model).

It is available in both SC-70-6 and miniQFN6 packages.

The features make it an ideal part for the switching of audio, video, and data stream.

FEATURES

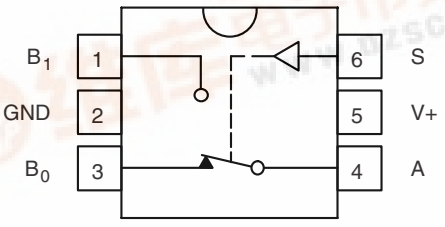
- Direct cross of industry standard xxx4157
- 1.8 V to 5.5 V operation voltage range
- Guaranteed 1.4 V logic high input threshold at V_{CC} = 5.5 V
- 117 MHz, - 3 dB bandwidth
- Low on-resistance
- Power down protection

Pb-free Available

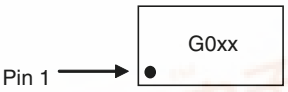
RoHS* COMPLIANT

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

SC-70-6L

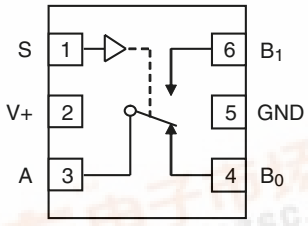


Top View

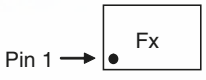


Device Marking: G0xx
xx = Date/Lot Traceability Code

miniQFN-6L



Top View



Device Marking: Fx
x = Date/Lot Traceability Code

TRUTH TABLE	
Logic Input (S)	**Function**
0	B_0 Connected to A
1	B_1 Connected to A

ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85 °C	SC-70-6L	DG4157DL-T1-E3
	miniQFN-6L	DG4157DN-T1-E4

* Pb containing terminations are not RoHS compliant, exemptions may apply.

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 6	V
S, A, B[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 200	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 400	
Storage Temperature	D Suffix	- 65 to 150	°C
Power Dissipation (Packages)[b]	SC-70-6L[c]	250	mW
	miniQFN-6L[d]	160	

Notes:
a. Signals on A, or B or S exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 3.1 mW/°C above 70 °C.
d. Derate 2.0 mW/°C above 70 °C.

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_{IN} = 0 V or V+[e]	Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
DC Characteristics							
On Resistance	R_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, I_O = 100 mA	Room		1.7	2.5	Ω
			Full			3	
		V+ = 4.5 V, B_0 or B_1 = 3.5 V, I_O = 100 mA	Room		0.95	1.2	
			Full			1.4	
On Resistance Flatness	$R_{FLATNESS}$	V+ = 2.7 V, B_0 or B_1 = 0.75 V, 1.5 V, I_O = 100 mA	Room		0.2		
		V+ = 4.5 V, B_0 or B_1 = 1 V, 3.5 V, I_O = 100 mA	Room		0.14	0.3	
			Full			0.4	
On Resistance Match	ΔR_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, I_O = 100 mA	Room		0.04		
		V+ = 4.5 V, B_0 or B_1 = 3.5 V, I_O = 100 mA	Room		0.05	0.12	
			Full			0.15	
Switch OFF Leakage Current	I_{OFF}	V+ = 5.5 V, A = 1 V, 4.5 V B_0 or B_1 = 4.5 V, 1 V or Floating	Room	- 2		2	nA
			Full	- 20		20	
Switch ON Leakage Current	I_{ON}		Room	- 4		4	
			Full	- 40		40	
Digital Control							
Input, High Voltage	V_{INH}	V+ = 2.7 V to 5.5 V	Full	1.4			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}, I_{INL}	V_{IN} = 0 or V+	Full	- 1		1	µA
Power Supply							
Power Supply Range	V+		Full	1.8		5.5	V
Quiescent Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 V, 5.5 V	Room		0.05	0.5	µA
			Full			1	

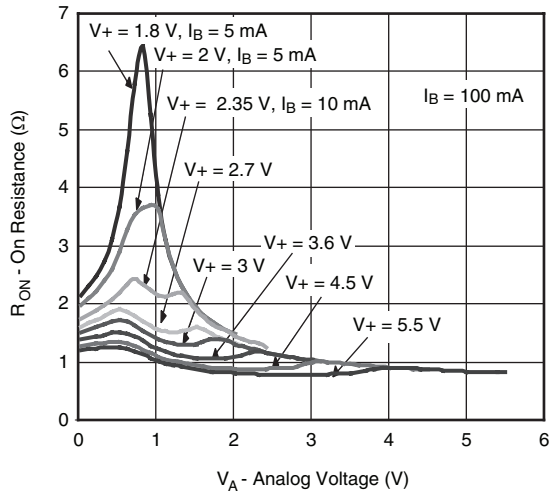
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 3.0 V, V_{IN} = 0 V or V+[e]	Temp.[a]	Limits - 40 °C to 85 °C Min.[b]	Typ.[c]	Max.[b]	Unit
AC Characteristics							
Turn-On Time[d]	t_{ON}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		40	55	ns
			Full			60	
		V+ = 4.5 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		22	37	
			Full			40	
Turn-Off Time[d]	t_{OFF}	V+ = 2.7 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		12	27	
			Full			30	
		V+ = 4.5 V, B_0 or B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room		8	23	
			Full			25	
Break-Before-Make Time[d]	t_{BBM}	V+ = 2.7 V, B_0 = B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF	Room	1	26		
		V+ = 4.5 V, B_0 = B_1 = 1.5 V, R_L = 50 Ω, C_L = 35 pF		1	15		
Charge Injection[d]	Q	C_L = 1 nF, R_{GEN} = 0 Ω, V_{GEN} = 0 V	Room		50		pC
Off Isolation[d]	OIRR	R_L = 50 Ω, f = 1 MHz	Room		- 58		dB
		R_L = 50 Ω, f = 10 MHz			- 31		
Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 63		
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz			- 36		
Bandwidth[d]	BW	R_L = 50 Ω	Room		117		MHz
Total Harmonic Distortion[d]	THD	R_L = 600 Ω, V_{IN} = 0.5 V, f = 20 to 20 kHz	Room		0.02		%
Capacitance							
BX Port Off Capacitance[d]	$C_{B(OFF)}$	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		20		pF
A Port On Capacitance[d]	$C_{A(ON)}$				57		
Control Pin Capacitance[d]	C_{IN}				5		

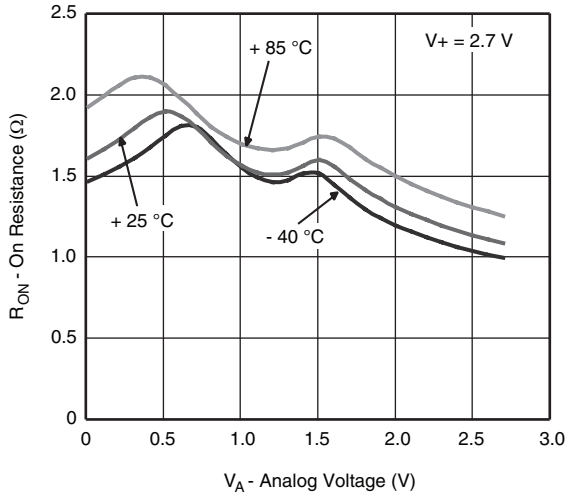
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

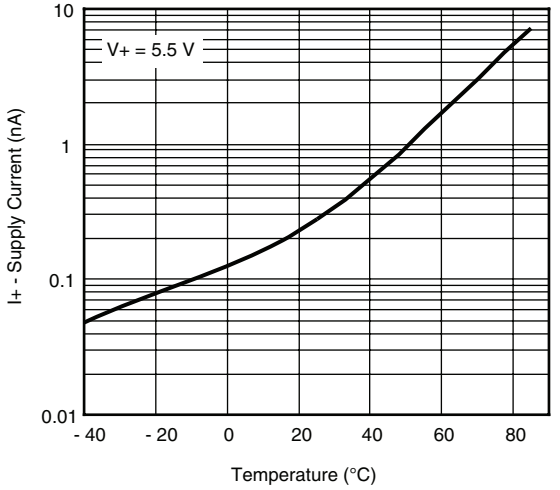
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



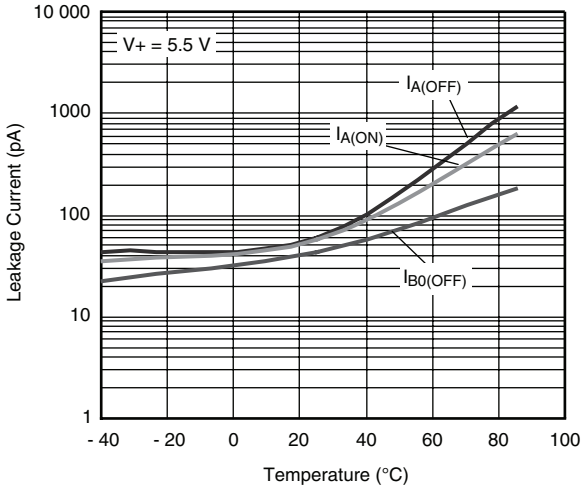
R_{ON} vs. V_A and Supply Voltage



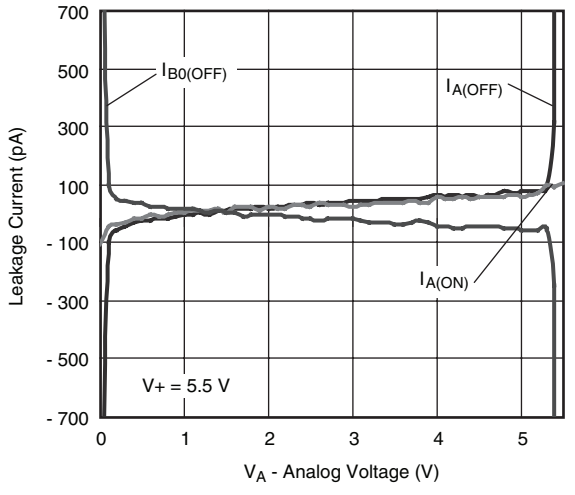
R_{ON} vs. V_D and Temperature



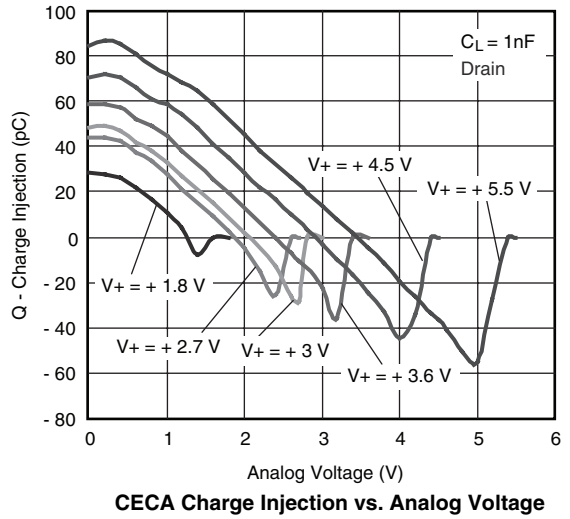
Supply Current vs. Temperature



Leakage Current vs. Temperature

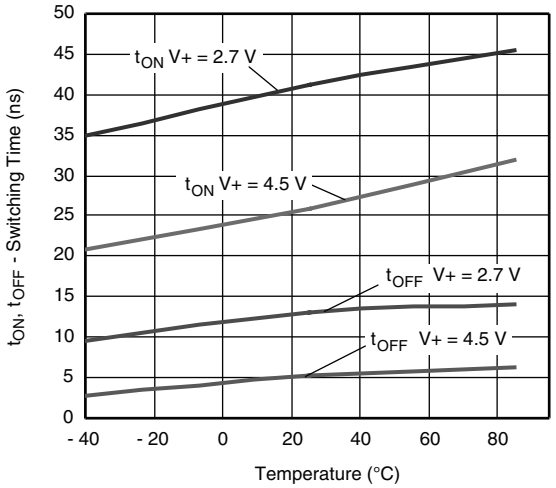


Leakage vs. Analog Voltage

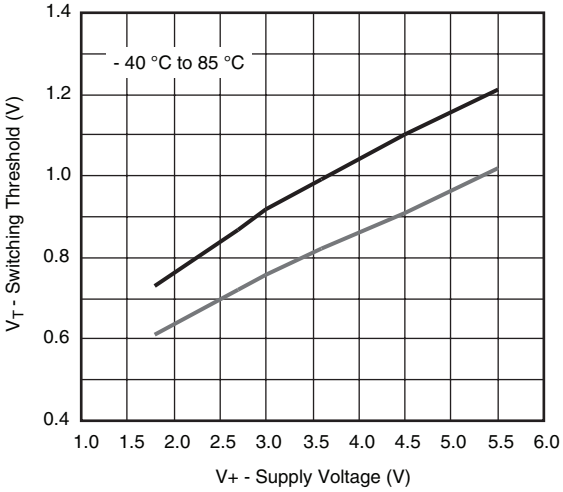


CECA Charge Injection vs. Analog Voltage

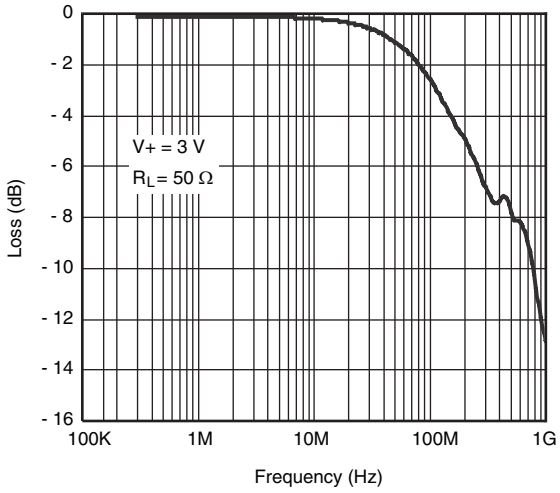
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



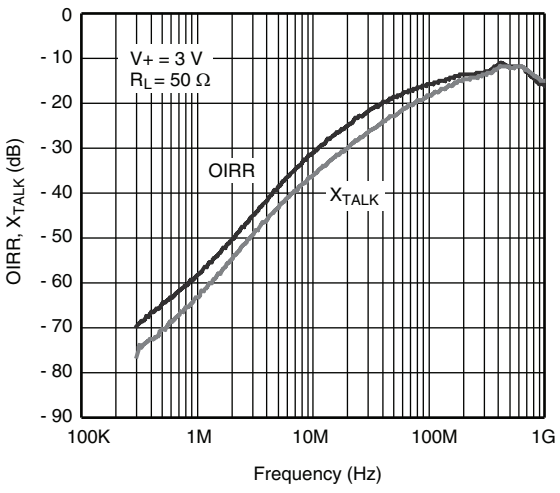
Switching Time vs. Temperature



Switching Threshold vs. Supply Voltage

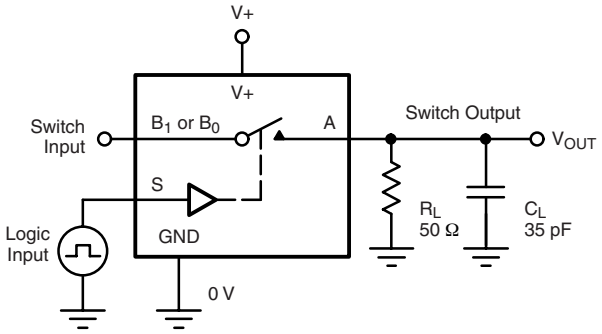


Insertion Loss vs. Frequency



Off-Isolation and Crosstalk vs. Frequency

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_A \left(\frac{R_L}{R_L + R_{ON}} \right)$$

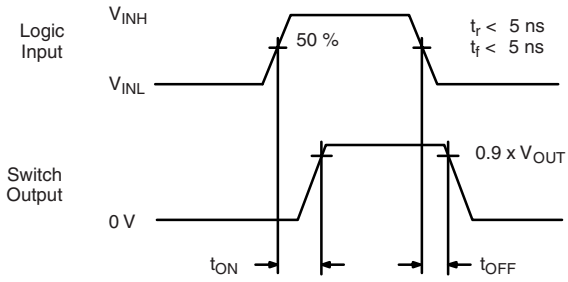
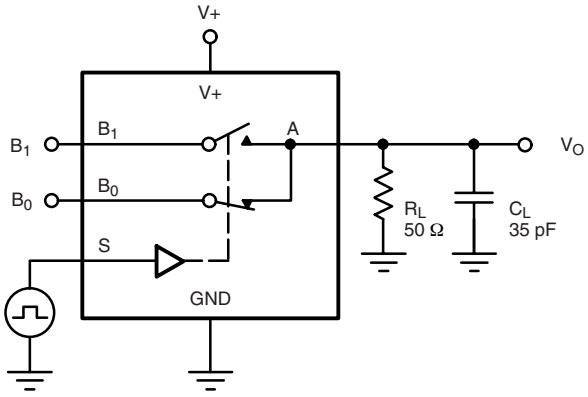


Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

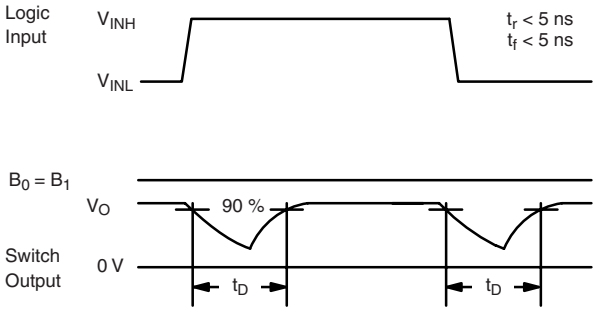
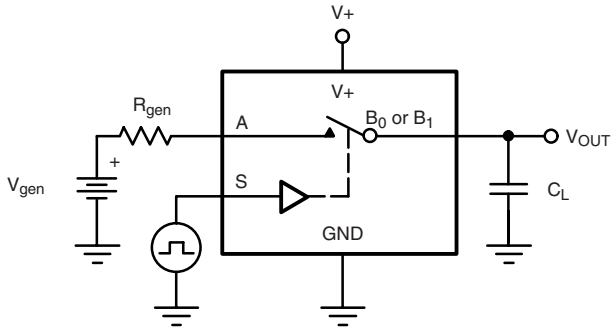
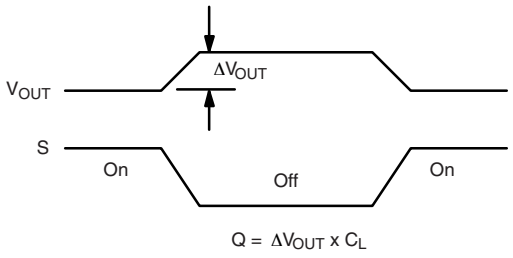


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

S depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

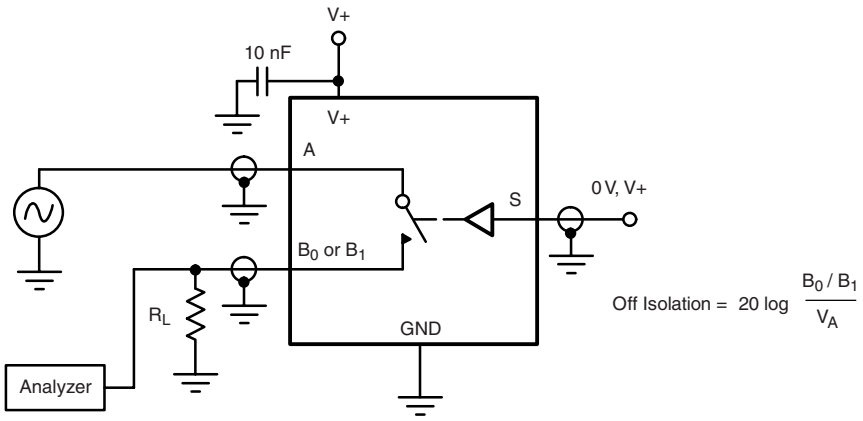


Figure 4. Off-Isolation

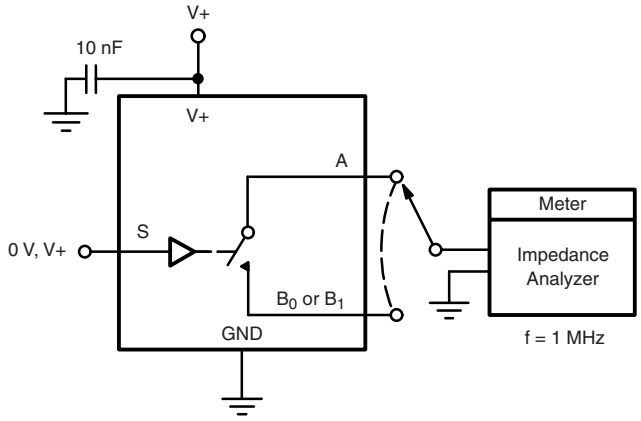


Figure 5. Channel Off/On Capacitance

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