



DG441L/442L

Vishay Siliconix

Precision Monolithic Quad SPST Low-Voltage CMOS Analog Switches

FEATURES

- 2.7- thru 12-V Single Supply or ± 3 - thru ± 6 -Dual Supply
- On-Resistance— $r_{DS(on)}$: 17 Ω
- Fast Switching— t_{ON} : 20 ns
— t_{OFF} : 12 ns
- TTL, CMOS Compatible
- Low Leakage: 0.25 nA
- 2000-V ESD Protection

BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals
- SDSL, DSLAM
- Audio and Video Signal Routing

DESCRIPTION

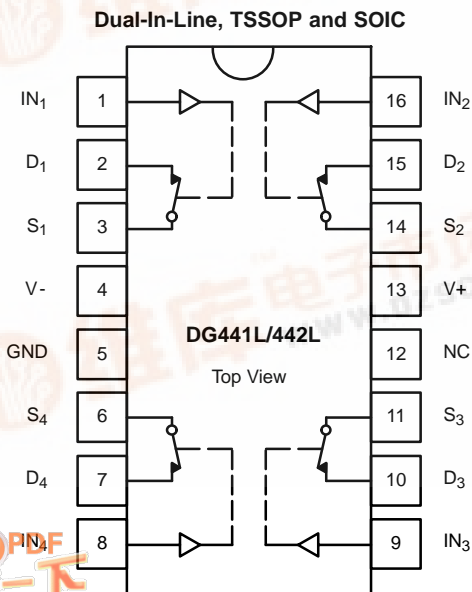
The DG441L/442L are low voltage pin-for-pin compatible companion devices to the industry standard DG441L/442L with improved performance

Using BiCMOS wafer fabrication technology allows the DG441L/442L to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

Combining high speed (t_{ON} : 20 ns), flat $r_{DS(on)}$ over the analog signal range (5 Ω), minimal insertion lose (-3 dB at 280 MHz), and excellent crosstalk and off-isolation performance (-50 dB at 50 MHz), the DG441L/442L are ideally suited for audio and video signal switching.

The DG441L/442L responds to opposite control logic as shown in the Truth Table. open and two normally closed switches.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG441L	DG442L
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin TSSOP	DG441LDQ
		DG442LDQ
	16-Pin Narrow SOIC	DG441LDY
		DG442LDY
-55 to 125°C	16-Pin CerDIP	DG441LAK, DG441LAK/883
		DG442LAK, DG442LAK/883
	LCC-20	DG441LAZ/883
		DG442LAZ/883



ABSOLUTE MAXIMUM RATINGS

V+ to V-	-0.3 to 13 V
GND to V-	7 V
Digital Inputs ^a V _S , V _D	GND -0.3 to (V+ + 0.3 V) or 30 mA, whichever occurs first
Continuous Current (Any Terminal)	30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle)	100 mA
Storage Temperature: (DQ, DY Suffix)	-65 to 125°C
(AK Suffix)	-65 to 150°C

Power Dissipation (Package) ^b	
16-Pin TSSOP ^c	450 mW
16-Pin Narrow Body SOIC ^d	650 mW
16-Pin CerDIP ^e	900 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 7 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C
- Derate 12 mW/°C above 75°C

SPECIFICATIONS ^a (SINGLE SUPPLY 12 V)									
Parameter	Symbol	Test Conditions Unless Specified V+ = 12 V, V- = 0 V V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	r _{DS(on)}	V+ = 10.8 V, V- = 0 V I _S = 10 mA, V _D = 2/9 V	Room Full	20		30 45		30 40	Ω
On-Resistance Match Between Channels ^e	Δr _{DS(on)}	I _S = 10 mA, V _D = 9 V	Room	0.1		0.5		0.5	
Switch Off Leakage Current	I _{S(off)}	V _D = 1/11 V, V _S = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	I _{D(off)}		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current	I _{D(on)}	V _S = V _D = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V _{IN} Low	I _{IL}	V _{IN} Under Test = 0.8 V	Full	0.01	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High	I _{IH}	V _{IN} Under Test = 2.4 V	Full		-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _S = 5 V See Figure 2	Room Full	20		60 80		60 70	ns
Turn-Off Time	t _{OFF}		Room Full	12		35 50		35 45	
Charge Injection ^e	Q	V _g = 0 V, R _g = 0 Ω, C _L = 10 nF	Room	5					pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room	71					dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room	95					
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room	5					pF
Drain Off Capacitance ^e	C _{D(off)}		Room	6					
Channel On Capacitance ^e	C _{D(on)}		Room	15					
Power Supplies									
Positive Supply Current	I+	V _{IN} = 0 or 12 V	Full	0.03		1.5		1	μA
Negative Supply Current	I-		Room Full	-0.002	-1 -7.5		-1 -5		
Ground Current	I _{GND}		Full	-0.002	-1.5		-1		



SPECIFICATIONS ^a (DUAL SUPPLY ± 5 V)									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		-5	5	-5	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	$V_+ = 5\text{ V}, V_- = -5\text{ V}$ $I_S = 10\text{ mA}, V_D = \pm 3.5\text{ V}$	Room Full	20		33 45		33 40	Ω
On-Resistance Match Between Channels ^e	$\Delta r_{DS(on)}$	$I_S = 10\text{ mA}, V_D = \pm 3.5\text{ V}$	Room	0.1		0.5		0.5	
Switch Off Leakage Current ^g	$I_{S(off)}$	$V_+ = 5.5\text{ V}, V_- = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}, V_S = \mp 4.5\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current ^g	$I_{D(on)}$	$V_+ = 5.5\text{ V}, V_- = -5.5\text{ V}$ $V_S = V_D = \pm 4.5\text{ V}$	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V_{IN} Low ^e	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.05	-1.5	1.5	-1	1	μA
Input Current, V_{IN} High ^e	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.05	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = \pm 3.5\text{ V}$ See Figure 2	Room Full	21		60 83		60 70	ns
Turn-Off Time	t_{OFF}		Room Full	16		35 55		35 45	
Charge Injection ^e	Q	$V_G = 0\text{ V}, R_G = 0\ \Omega, C_L = 10\text{ nF}$	Room	5					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF},$ $f = 1\text{ MHz}$	Room	68					dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room	85					
Source Off Capacitance ^e	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance ^e	$C_{D(off)}$		Room	9					
Channel On Capacitance ^e	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current ^e	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Full	0.002		1.5		1	μA
Negative Supply Current ^e	I-		Room Full	-0.002		-1 -7.5		-1 -5	
Ground Current ^e	I_{GND}		Full	-0.002		-1.5		-1	

SPECIFICATIONS ^a (SINGLE SUPPLY 5 V)									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		0	5	0	5	V
Drain-Source On-Resistance ^e	$r_{DS(on)}$	$V_+ = 4.5\text{ V}, I_S = 5\text{ mA}$ $V_D = 1\text{ V}, 3.5\text{ V}$	Room Full	35		50 88		50 75	Ω
On-Resistance Match Between Channels ^e	$\Delta r_{DS(on)}$	$I_S = 5\text{ mA}, V_D = 3.5\text{ V}$	Room	0.5		1.0		1.0	
Dynamic Characteristics									
Turn-On Time ^e	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = 3.5\text{ V}$, See Figure 2	Room Hot	27		50 90		50 60	ns
Turn-Off Time ^e	t_{OFF}		Room Hot	15		30 55		30 40	



SPECIFICATIONS ^a (SINGLE SUPPLY 5 V)									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Dynamic Characteristics									
Charge Injection ^e	Q	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$	Room	0.5					pC
Power Supplies									
Positive Supply Current ^e	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Full	10		200		100	μA
Negative Supply Current ^e	I-		Room	-0.002	-1		-1		
Ground Current ^e	I _{GND}		Full	-10	-200		-100		

SPECIFICATIONS ^a (SINGLE SUPPLY 3 V)									
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 3\text{ V}, V_- = 0\text{ V}$ $V_{IN} = 0.4\text{ V}^f$	Temp ^b	Typ ^c	A Suffix Limits -55 to 125°C		D Suffix Limits -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	r _{DS(on)}	$V_+ = 2.7\text{ V}, V_- = 0\text{ V}$ $I_S = 5\text{ mA}, V_D = 0.5, 2.2\text{ V}$	Room	65		80		80	Ω
On-Resistance Match Between Channels ^e	$\Delta r_{DS(on)}$	$I_S = 5\text{ mA}, V_D = 2.2\text{ V}$	Room	1.0		3.0		3.0	
Switch Off Leakage Current ^g	I _{S(off)}	$V_+ = 3.3\text{ V}, V_- = 0\text{ V}$ $V_D = 1, 2\text{ V}, V_S = 2, 1\text{ V}$	Room		-1	1	-1	1	nA
	I _{D(off)}		Full		-15	15	-10	10	
Channel On Leakage Current ^g	I _{D(on)}	$V_+ = 3.3\text{ V}, V_- = 0\text{ V}$ $V_S = V_D = 1, 2\text{ V}$	Room		-1	1	-1	1	
			Full		-15	15	-10	10	
Digital Control									
Input Current, V _{IN} Low ^e	I _{IL}	V _{IN} Under Test = 0.4 V	Full	0.005	-1.5	1.5	-1	1	μA
Input Current, V _{IN} High ^e	I _{IH}	V _{IN} Under Test = 2.4 V	Full	0.005	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t _{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$ See Figure 2	Room	50		136		136	ns
Turn-Off Time	t _{OFF}		Full	30		100		100	
Charge Injection ^e	Q	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 10\text{ nF}$	Room	1					pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF},$ $f = 1\text{ MHz}$	Room	68					dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room	85					
Source Off Capacitance ^e	C _{S(off)}		Room	6					
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz	Room	6					pF
Channel On Capacitance ^e	C _{D(on)}		Room	20					

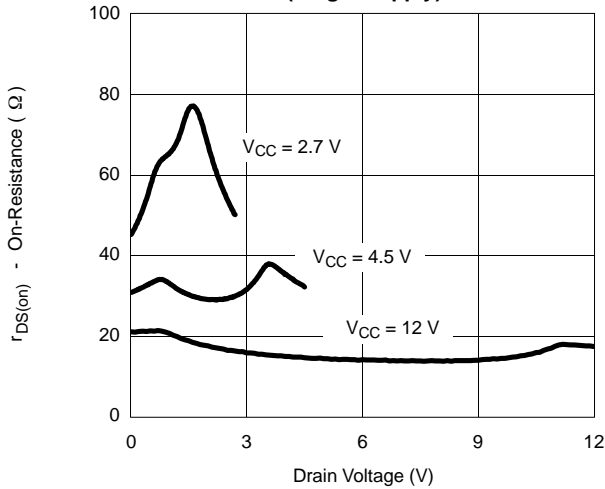
Notes:

- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.
- Leakage parameters are guaranteed by worst case test conditions and not subject to test.

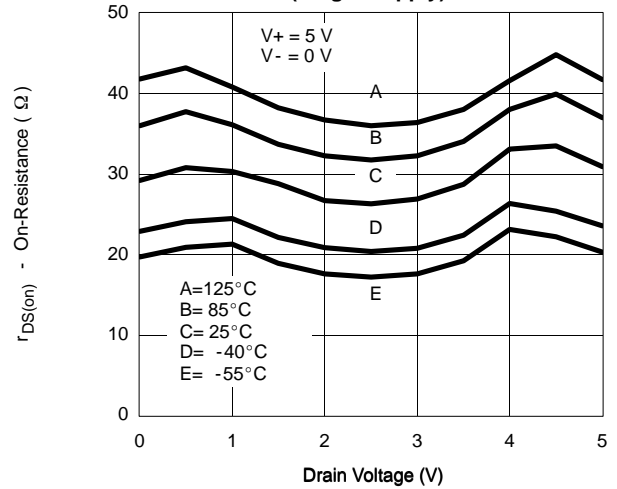


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

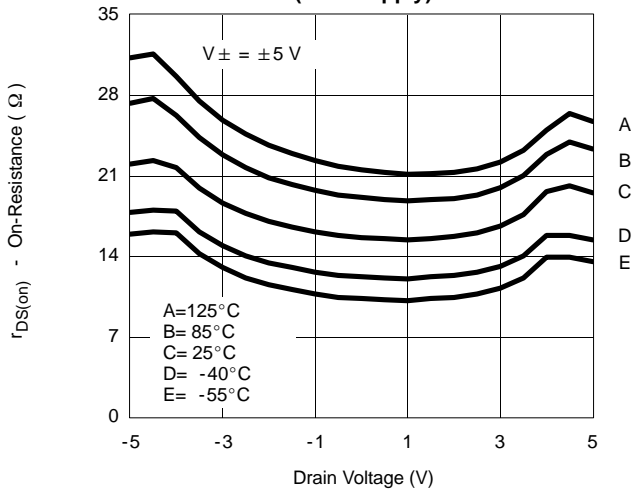
$r_{DS(on)}$ vs. Drain Voltage (Single Supply)



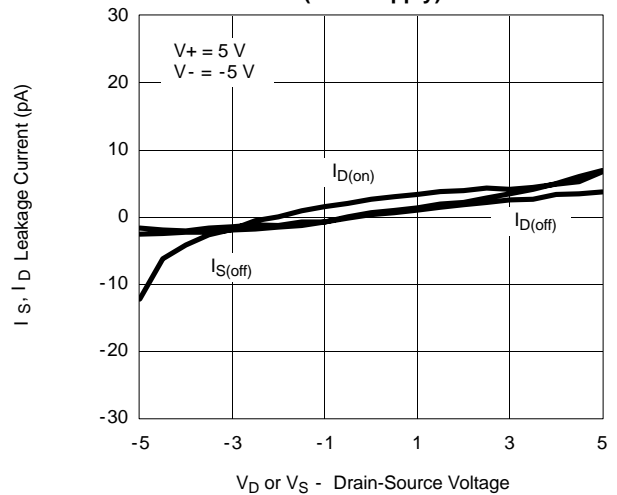
$r_{DS(on)}$ vs. Drain Voltage and Temperature (Single Supply)



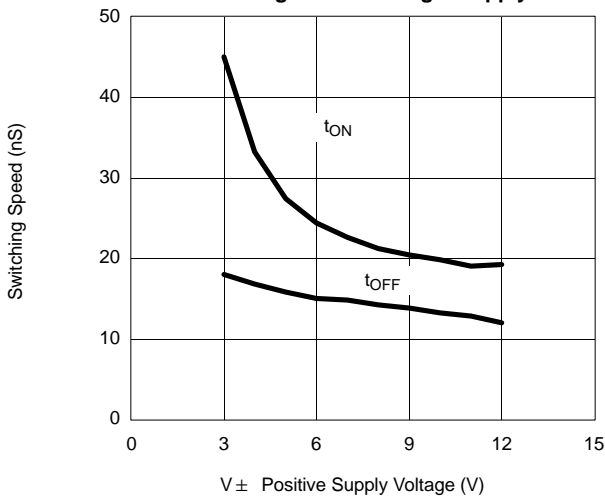
$r_{DS(on)}$ vs. Drain Voltage and Temperature (Dual Supply)



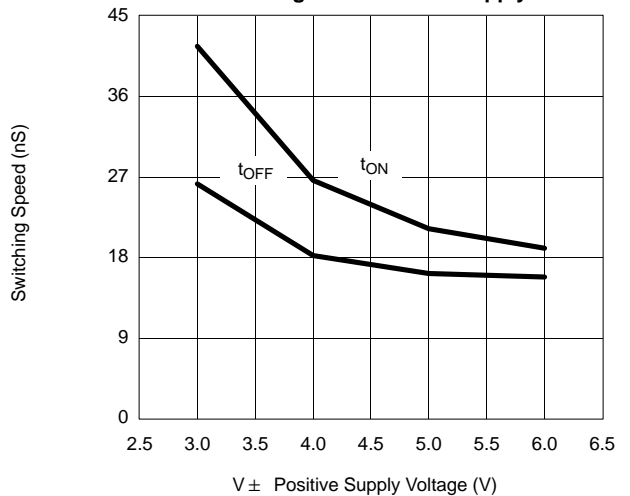
Leakage Current vs. Analog Voltage (Dual Supply)



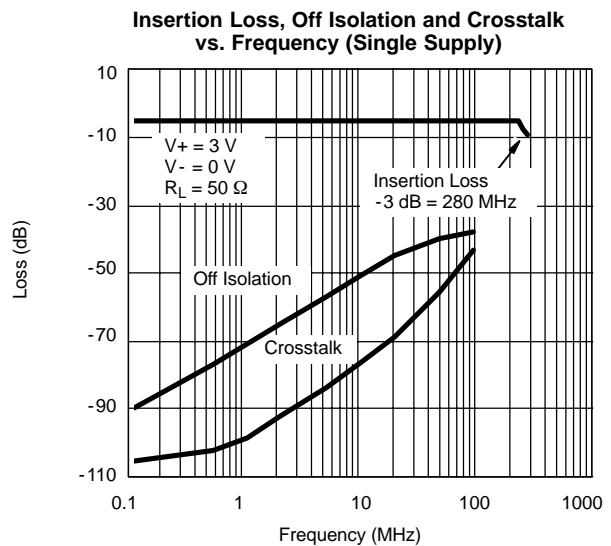
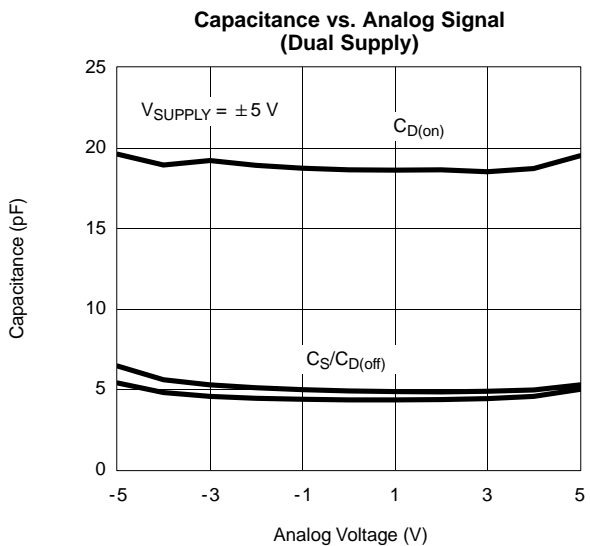
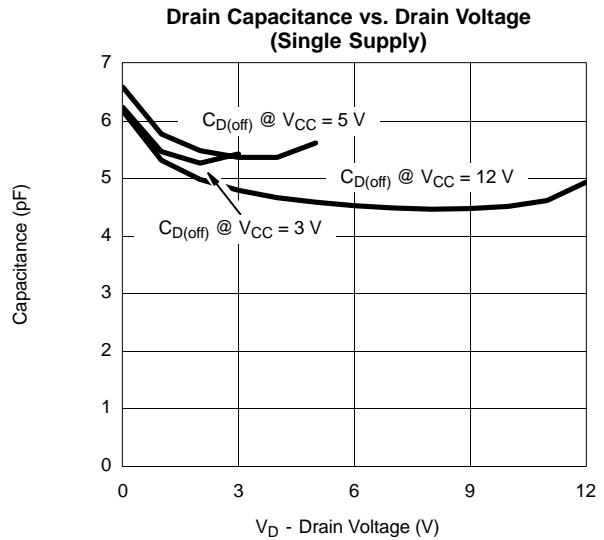
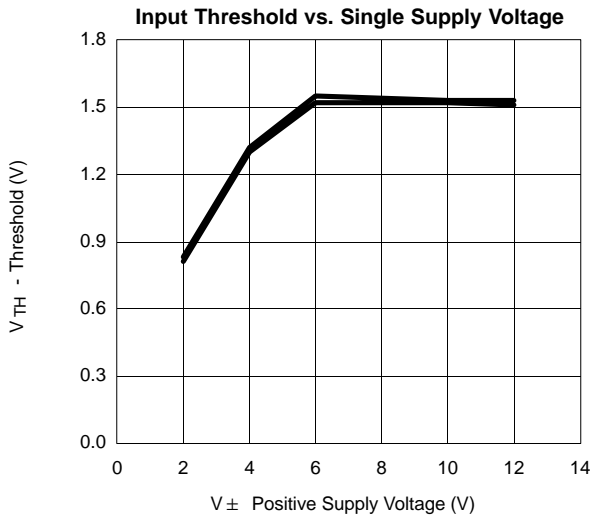
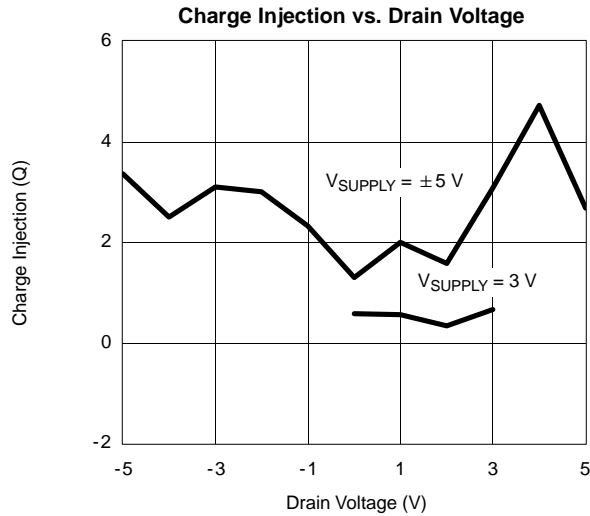
Switching Time vs. Single Supply



Switching Time vs. Dual Supply



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

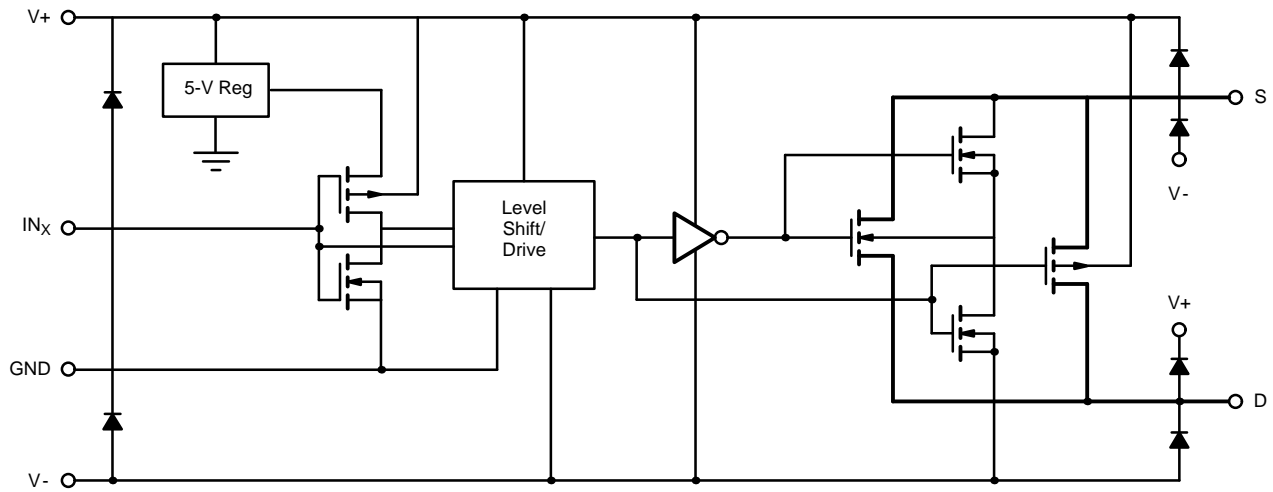
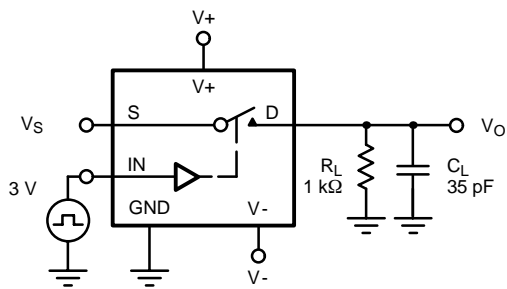
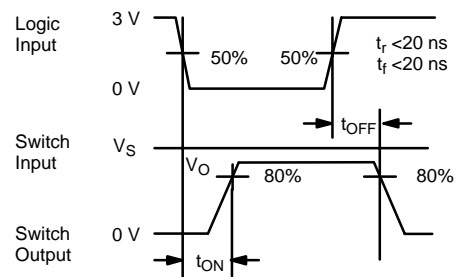


FIGURE 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)



Note: Logic input waveform is inverted for DG442.

FIGURE 2. Switching Time

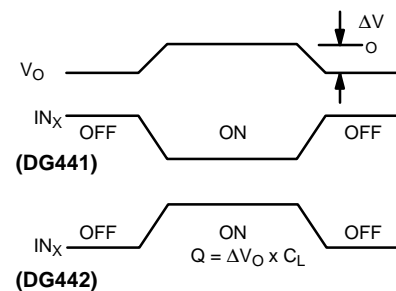
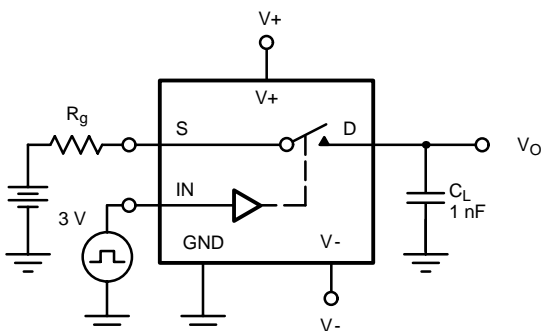


FIGURE 3. Charge Injection

TEST CIRCUITS

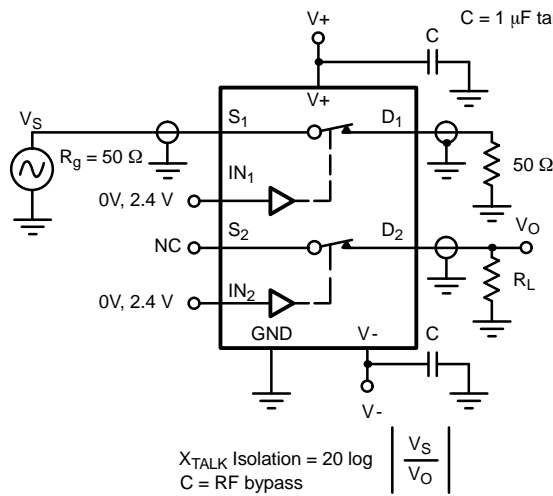


FIGURE 4. Crosstalk

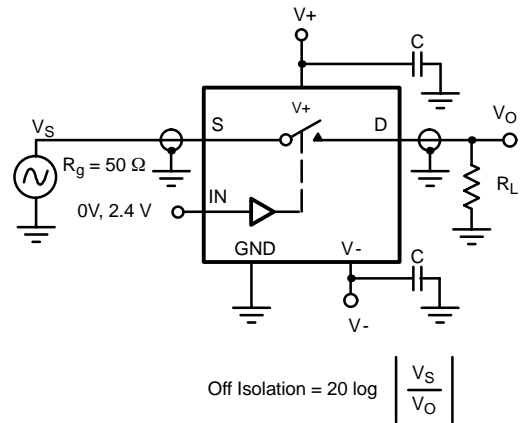


FIGURE 5. Off Isolation

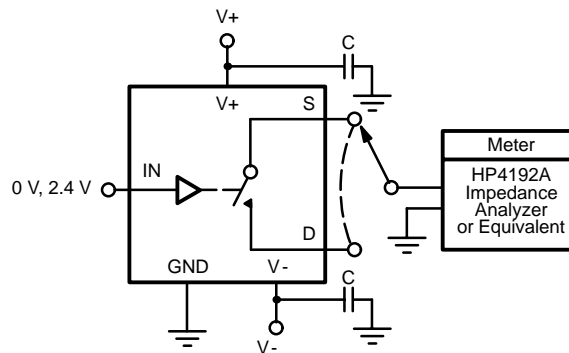


FIGURE 6. Source/Drain Capacitances

APPLICATIONS

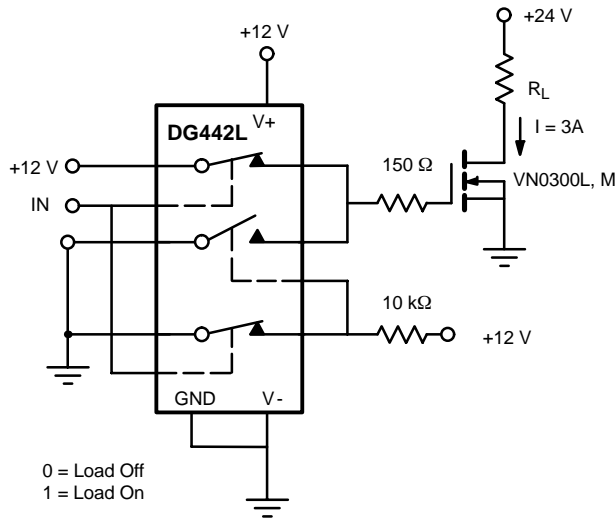


FIGURE 7. Power MOSFET Driver

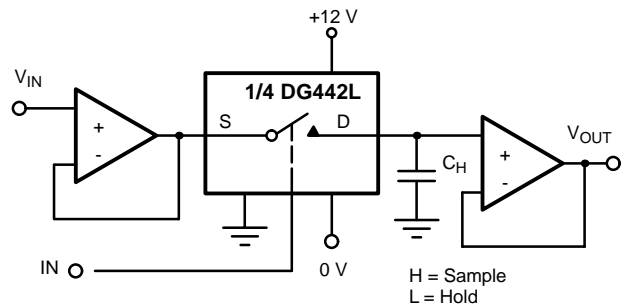
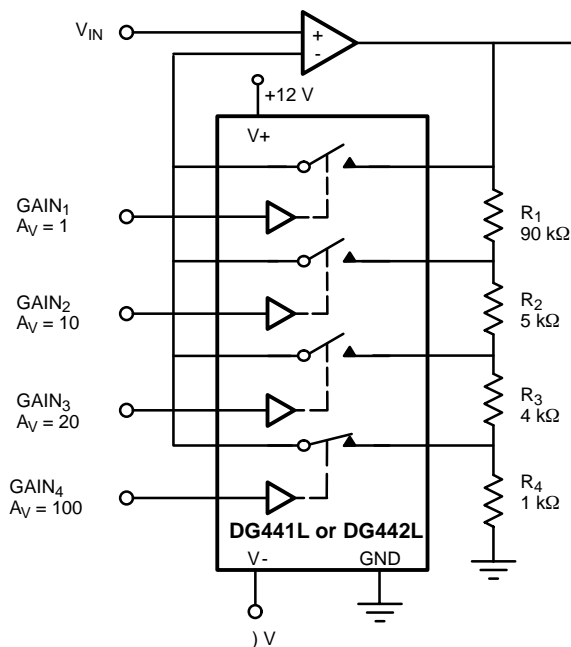


FIGURE 8. Open Loop Sample-and-Hold



Gain error is determined only by the resistor tolerance. Op amp offset and CMRR will limit accuracy of circuit.

With SW₄ Closed

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

FIGURE 9. Precision-Weighted Resistor Programmable-Gain Amplifier



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All product specifications and data are subject to change without notice.

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