Low-Voltage Dual SPST Analog Switch

DESCRIPTION

The DG9232/9233 is a single-pole/single-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 35 ns, t_{OFF}: 20 ns), low on-resistance ($r_{DS(on)}$: 20 Ω) and small physical size, the DG9232/9233 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9232/9233 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7 is 2000 V. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9232/9233.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

FEATURES

- Low Voltage Operation (+ 2.7 to + 5 V)
- Low On-Resistance - $r_{DS(on)}$: 20 Ω
- Fast Switching - t_{ON}: 35 ns, t_{OFF}: 20 ns
- Low Leakage - $I_{COM(on)}$: 200 pA max
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in MSOP-8 and SOIC-8

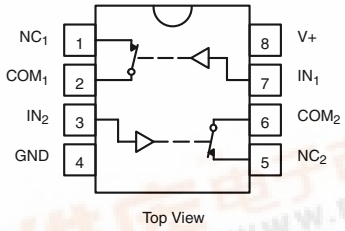
Pb-free Available

RoHS* COMPLIANT

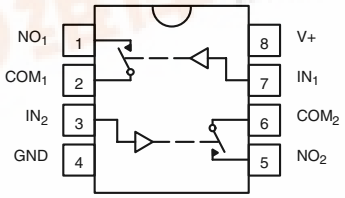
APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top View



Top View

TRUTH TABLE - DG9232

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

TRUTH TABLE - DG9233

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 to 85 °C	SOIC-8	DG9232DY DG9232DY-E3 DG9232DY-T1 DG9232DY-T1-E3
		DG9233DY DG9233DY-E3 DG9233DY-T1 DG9233DY-T1-E3
	MSOP-8	DG9232DQ-T1-E3
		DG9233DQ-T1-E3

* Pb containing terminations are not RoHS compliant, exemptions may apply

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
Reference V+ to GND		- 0.3 to + 13	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any terminal)		± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 40	
ESD (Method 3015.7)		> 2000	V
Storage Temperature	D Suffix	- 65 to 125	°C
Power Dissipation (Packages)[b]	8-Pin Narrow Body SOIC[c]	400	mW

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 70 °C.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	Temp[a]	D Suffix - 40 to 85 °C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V, V+ = 2.7 V, I_{COM} = 5 mA	Room Full		30	50 80	Ω
$r_{DS(on)}$ Match[d]	$\Delta r_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room		0.4	2	
$r_{DS(on)}$ Flatness[d]	$r_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1 and 2 V	Room		4	8	
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/2 V, V_{COM} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	pA
COM Off Leakage Current[g]	$I_{COM(off)}$	V_{COM} = 1 V/2 V, V_{NO} or V_{NC} = 2 V/1 V	Room Full	- 100 - 5000	5	100 5000	
Channel-On Leakage Current[g]	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/2 V	Room Full	- 200 - 10000	10	200 10000	
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 120	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X_{TALK}		Room		- 90		
NC and NO Capacitance	$C_{S(off)}$	f = 1 MHz	Room		7		pF
Channel-On Capacitance	$C_{COM(on)}$		Room		20		
COM-Off Capacitance	$C_{COM(off)}$		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V_{IN} = 0 or 3.3 V				1	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 5-V leakage tests, not production tested.

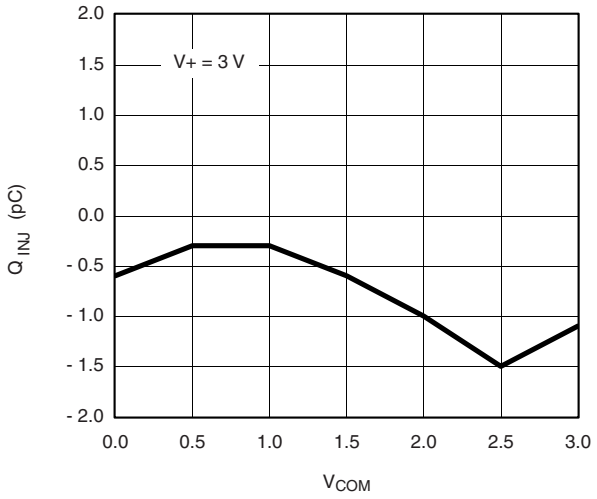
SPECIFICATIONS (V+ = 5 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]	Temp[a]	D Suffix - 40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V, V+ = 4.5 V I_{COM} = 5 mA	Room Full		20	30 50	Ω
$r_{DS(on)}$ Match[d]	$\Delta r_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V	Room		0.4	2	
$r_{DS(on)}$ Flatness[d]	$r_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1, 2 and 3 V	Room		2	6	
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V/4 V, V_{COM} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	pA
COM Off Leakage Current	$I_{COM(off)}$	V_{COM} = 1 V/4 V, V_{NO} or V_{NC} = 4 V/1 V	Room Full	- 100 - 5000	10	100 5000	
Channel-On Leakage Current	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V/4 V	Room Full	- 200 - 10000		200 10000	
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3.0 V	Room Full		35	75 150	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 100	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 74		dB
Crosstalk	X_{TALK}		Room		- 90		
NC and NO Capacitance	$C_{(off)}$	f = 1 MHz	Room		7		pF
Channel-On Capacitance	$C_{D(on)}$		Room		20		
COM-Off Capacitance	$C_{D(off)}$		Room		13		
Power Supply							
Positive Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 or 5.5 V				1	µA

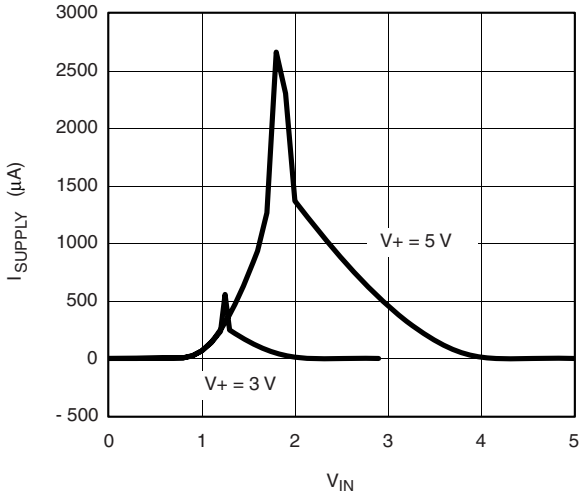
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

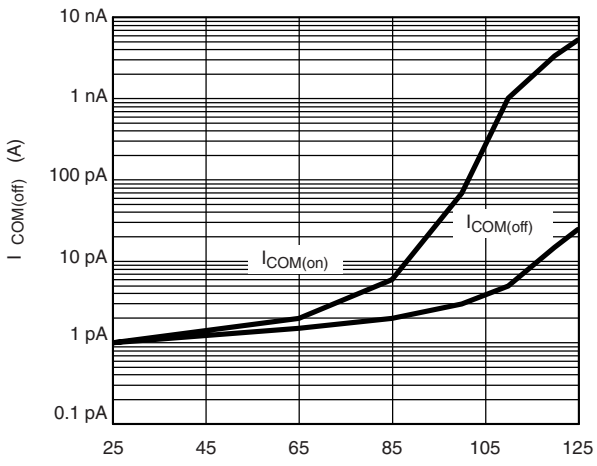
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



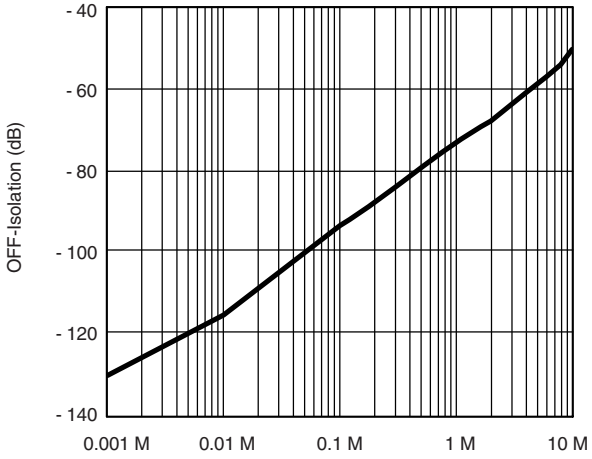
Charge Injection



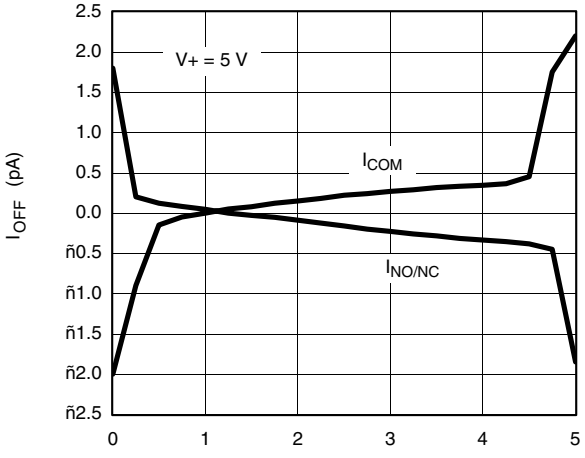
Supply Current vs. V_{IN}



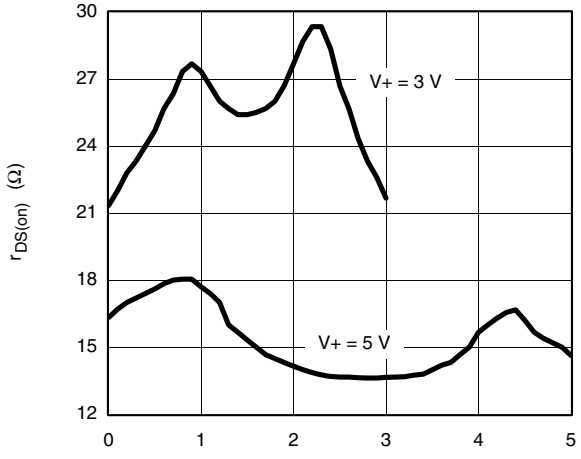
Leakage Current vs. Temperature



Off-Isolation vs. Frequency

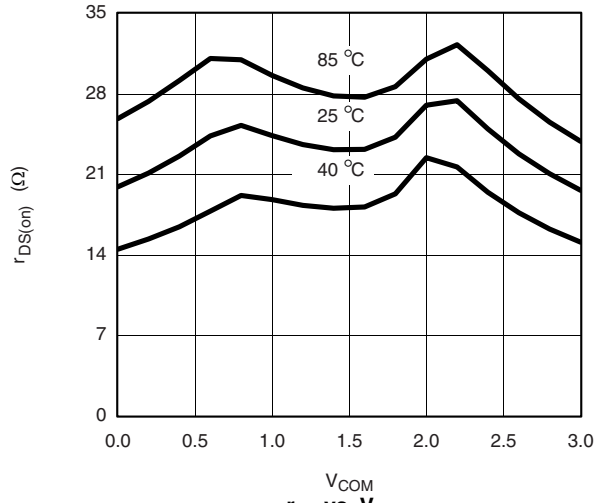


Off-Leakage vs. Voltage at 25 °C

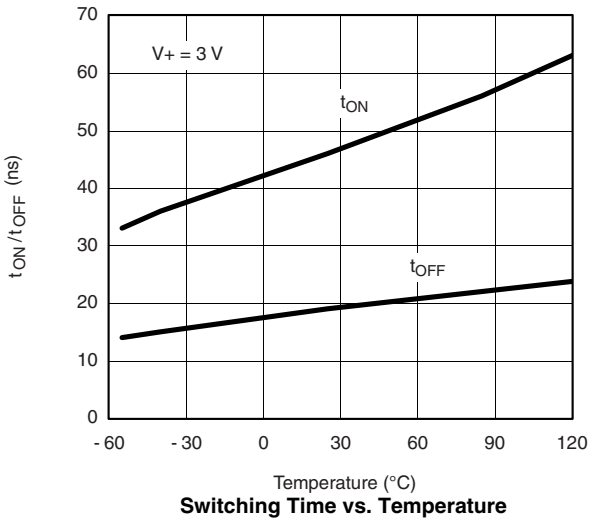


r_{DS} vs. V_{COM}

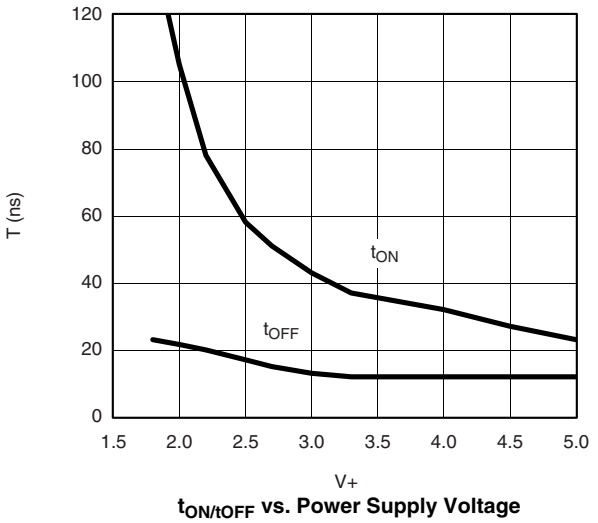
TYPICAL CHARACTERISTICS T_A = 25 °C, unless otherwise noted



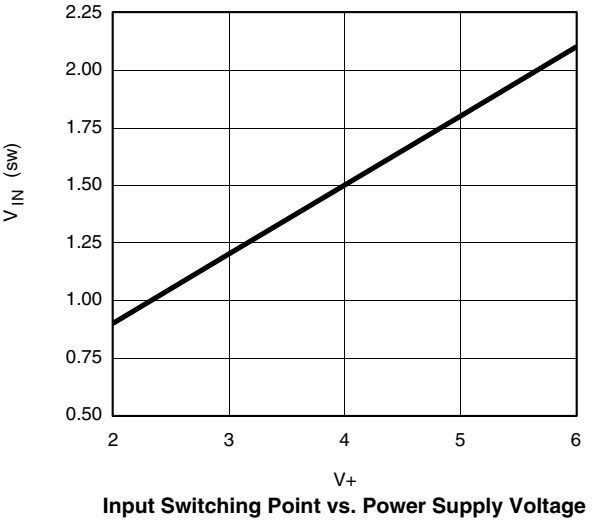
r_{DS} vs. V_{COM}



Switching Time vs. Temperature

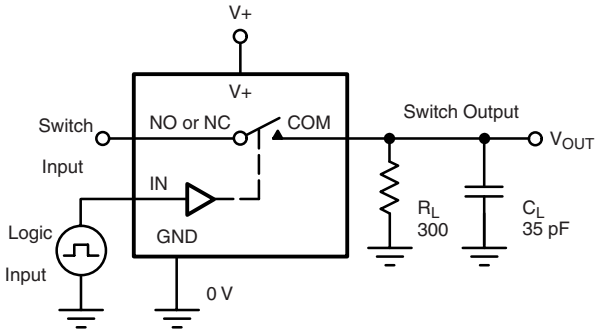


$t_{ON/tOFF}$ vs. Power Supply Voltage



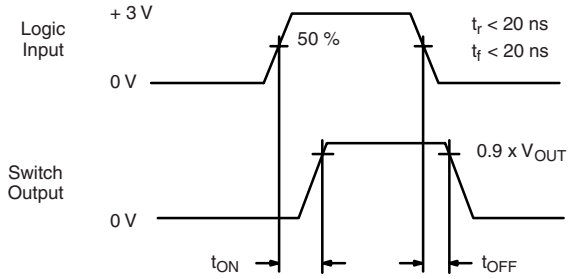
Input Switching Point vs. Power Supply Voltage

TEST CIRCUITS



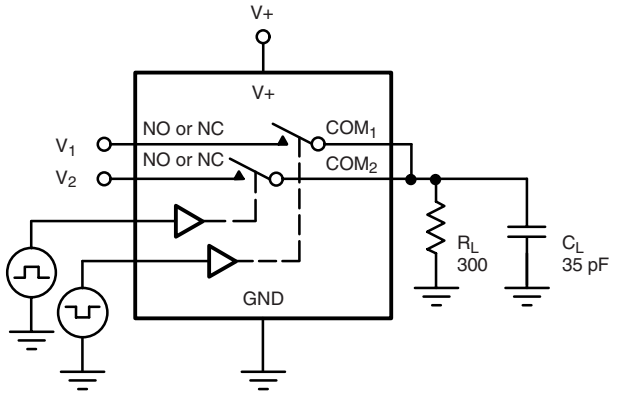
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

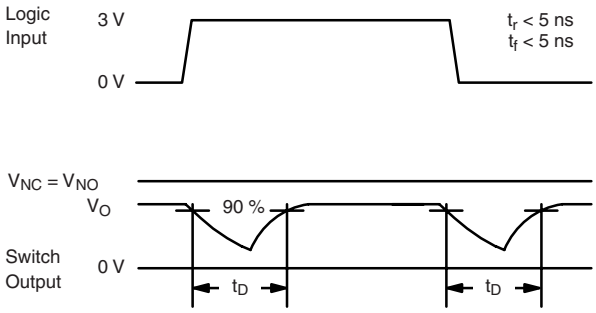
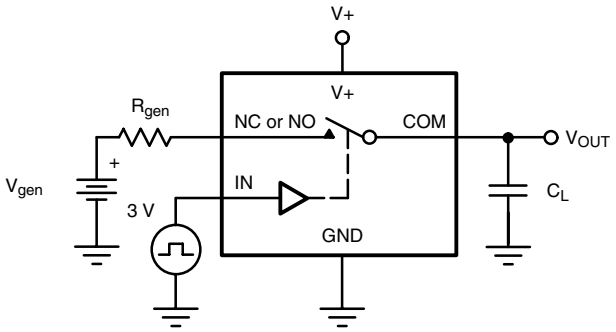
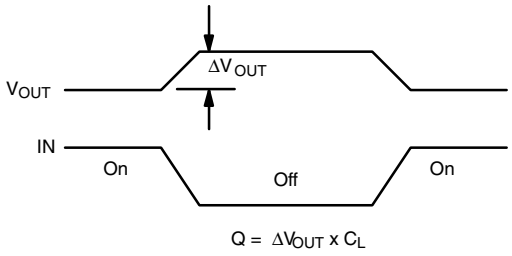


Figure 2. Break-Before-Make Interval





$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS

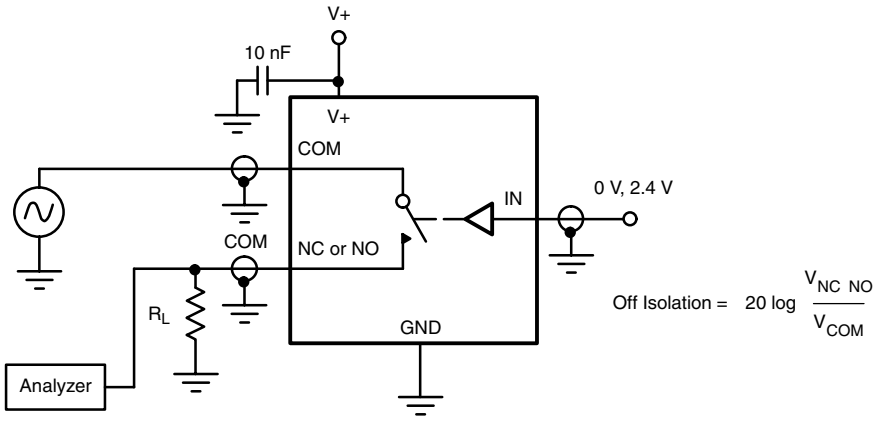


Figure 4. Off-Isolation

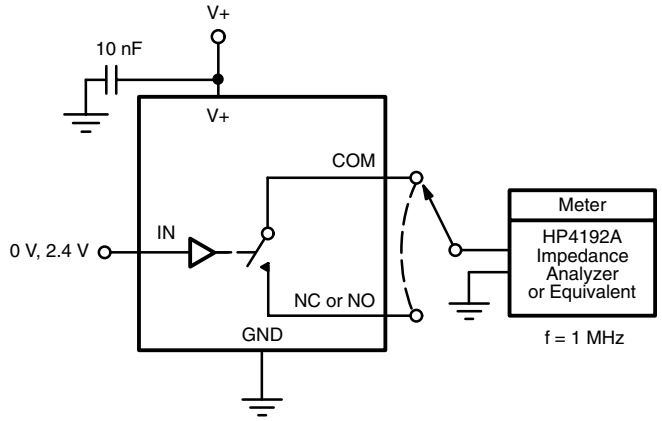


Figure 5. Channel Off/On Capacitance

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