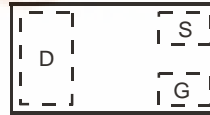


DMN2005LP4K

N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

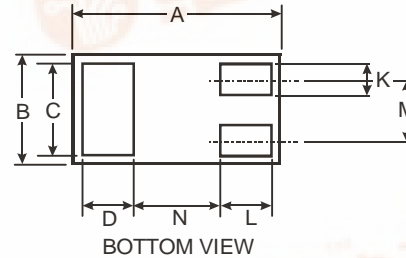
- Low On-Resistance
- Very Low Gate Threshold Voltage, 0.9V Max.
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Lead Free By Design/RoHS Compliant (Note 2)
- "Green" Device (Note 4)
- ESD Protected Gate
- Ultra Low Profile Package



TOP VIEW

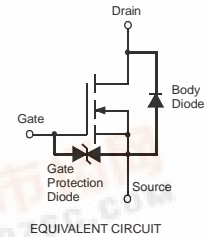


SIDE VIEW



BOTTOM VIEW

DFN1006H4-3			
Dim	Min	Max	Typ
A	0.95	1.075	1.00
B	0.55	0.675	0.60
C	0.45	0.55	0.50
D	0.20	0.30	0.25
G	—	0.40	—
H	0	0.05	0.02
K	0.10	0.20	0.15
L	0.20	0.30	0.25
M	—	—	0.35
N	—	—	0.40
All Dimensions in mm			



Mechanical Data

- Case: DFN1006H4-3
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020C
- Terminal Connections: See Diagram
- Terminals: Finish — NiPdAu annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Marking: See Page 4
- Ordering & Date Code Information: See Page 4
- Weight: 0.001 grams

Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate-Source Voltage	V_{GSS}	± 10	V
Drain Current per element (Note 1)	I_D	Continuous	mA
		Pulsed (Note 3)	
Total Power Dissipation (Note 1)	P_d	200	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	625	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_j, T_{STG}	-65 to +150	$^\circ\text{C}$

- Notes:
1. Device mounted on FR-4 PCB.
 2. No purposefully added lead.
 3. Pulse width $\leq 10\mu\text{s}$, Duty Cycle $\leq 1\%$.
 4. Diodes Inc.'s "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (per element) (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	$V_{GS} = 0V, I_D = 100\mu A$
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	$V_{DS} = 17V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$
ON CHARACTERISTICS (per element) (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	0.53	—	0.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	—	0.9	1.5	Ω	$V_{GS} = 4V, I_D = 10mA$
		—	0.85	1.7		$V_{GS} = 2.7V, I_D = 200mA$
		—	1.2	1.7		$V_{GS} = 2.5V, I_D = 10mA$
		—	2.4	3.5		$V_{GS} = 1.8V, I_D = 200mA$
		—	2.5	3.5		$V_{GS} = 1.5V, I_D = 1mA$
Forward Transfer Admittance	$ Y_{fs} $	40	—	—	mS	$V_{DS} = 3V, I_D = 10mA$

Notes: 5. Short duration test pulse used to minimize self-heating effect.

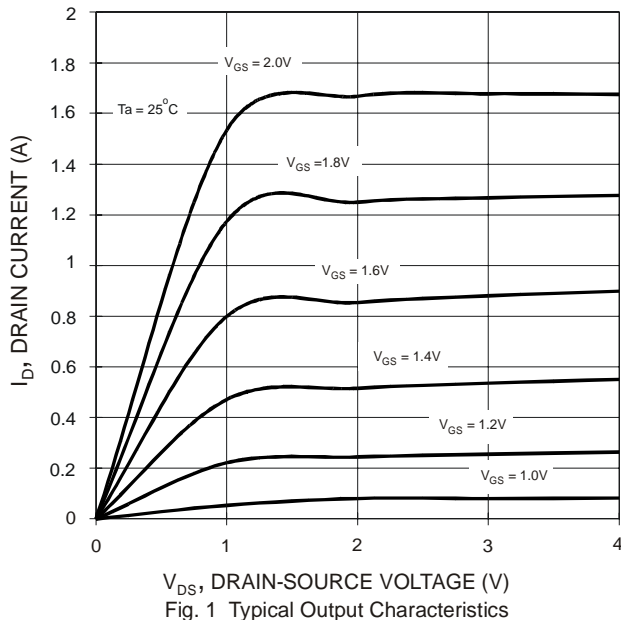


Fig. 1 Typical Output Characteristics

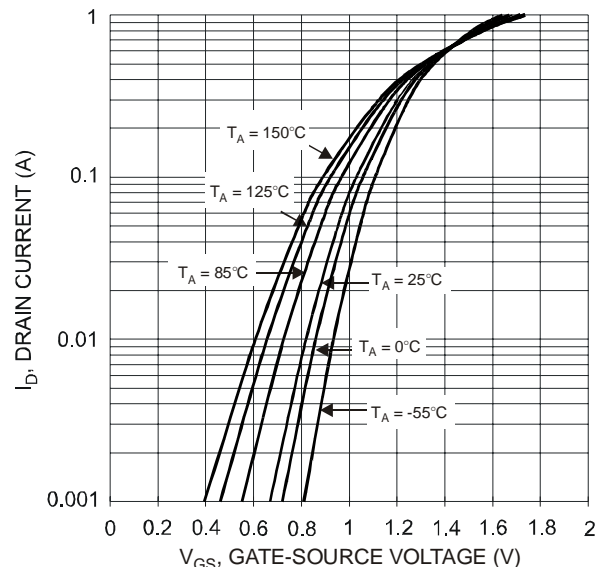


Fig. 2 Reverse Drain Current vs. Source-Drain Voltage

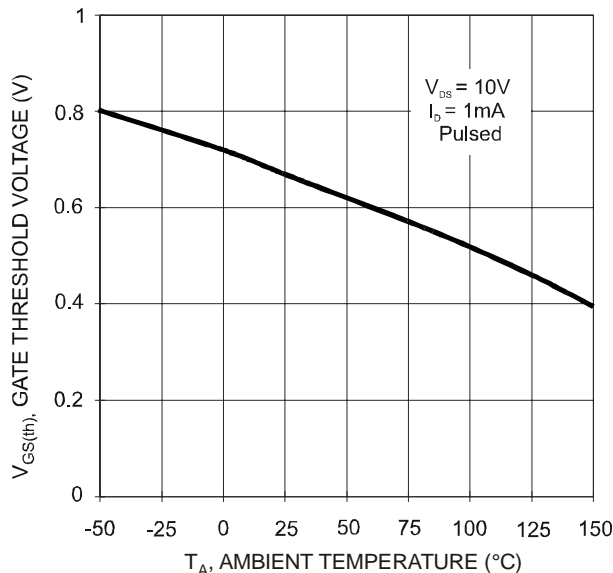


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

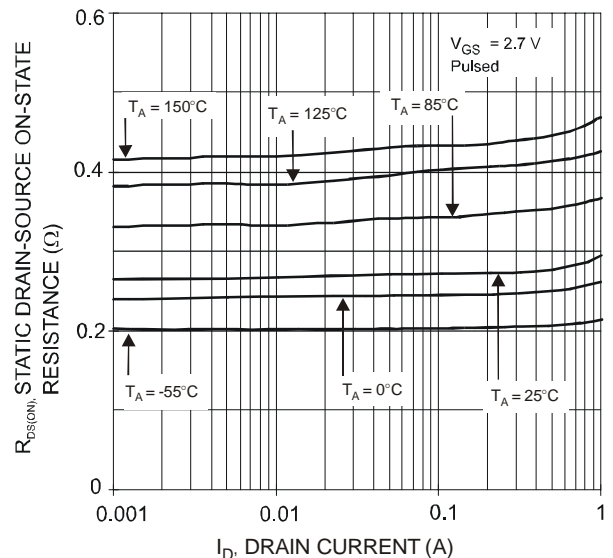


Fig. 4 Static Drain-Source On-State Resistance vs. Drain Current

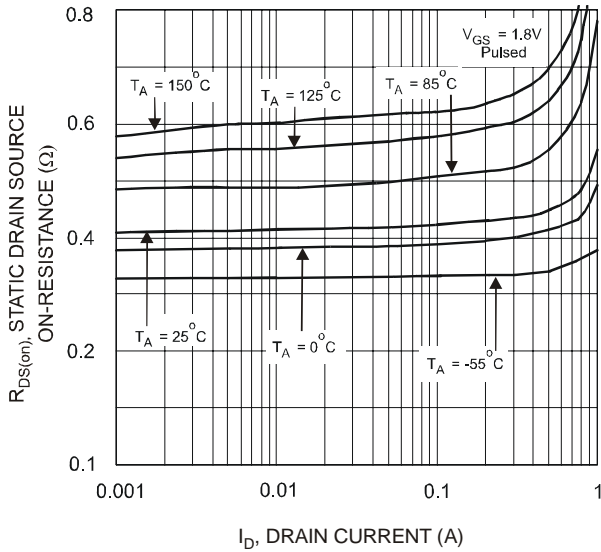


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

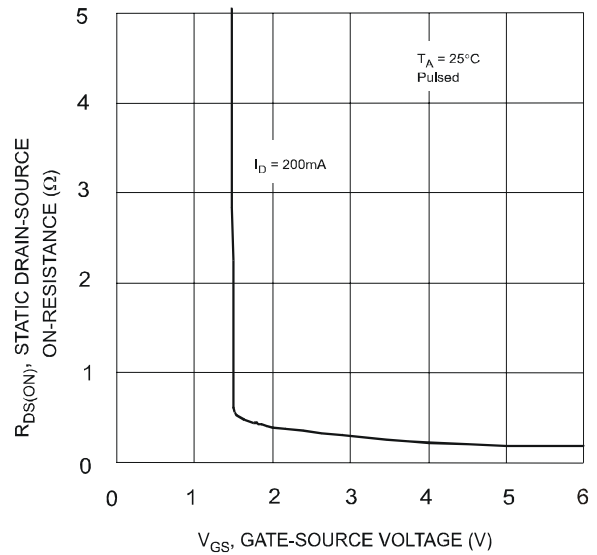


Fig. 6 Static Drain-Source, On-Resistance vs. Gate-Source Voltage

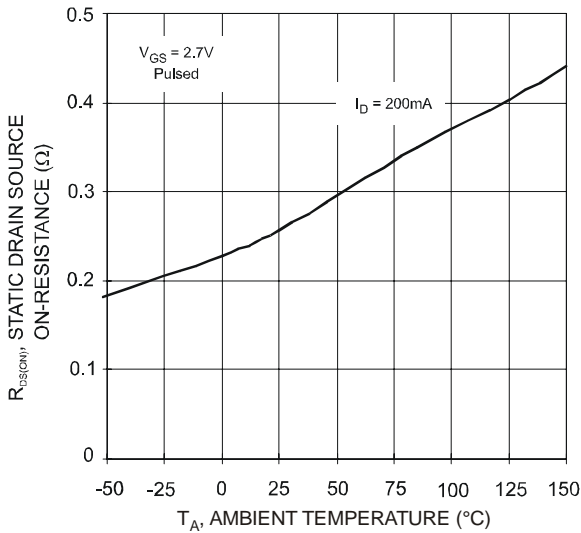


Fig. 7 Static Drain-Source, On-Resistance vs. Ambient Temperature

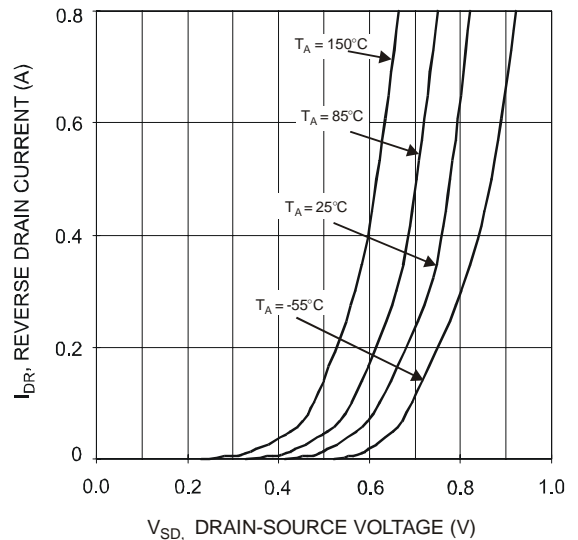


Fig. 8 Reverse Drain Current vs. Source-Drain Voltage

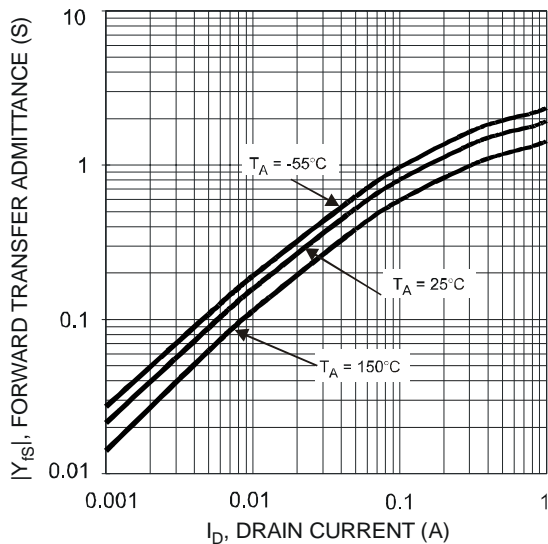


Fig. 9 Forward Transfer Admittance vs. Drain Current

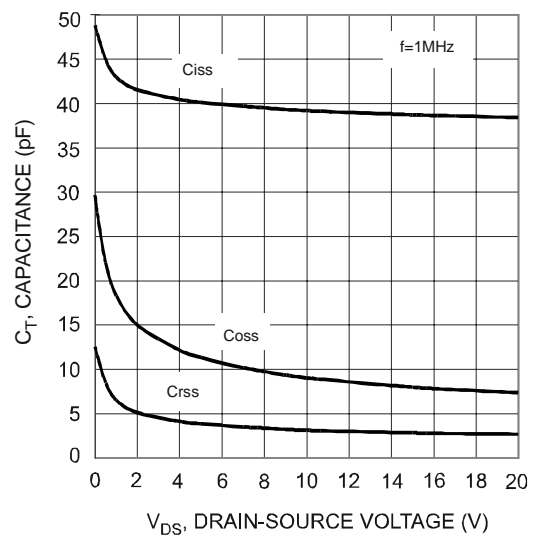


Fig. 10 Typical Capacitance



Ordering Information (Note 6)

Device	Packaging	Shipping
DMN2005LP4K-7	DFN1006H4-3	3000/Tape & Reel

Notes: For packaging details, please go to our website at <http://www.diodes.com/ap02007.pdf>.

Marking Information



DN = Product Type Marking Code
Dot Denotes Drain Side

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